PROGRESS AND APPLICATION OF THROUGH GLASS VIA (TGV) TECHNOLOGY

Aric B. Shorey and Rachel Lu
Corning, Incorporated
Corning, NY USA
shoreyab@corning.com

ABSTRACT
Glass provides many opportunities for advanced packaging. The most obvious advantage is given by the material properties. As an insulator, glass has low electrical loss, particularly at high frequencies. The relatively high stiffness and ability to adjust the coefficient of thermal expansion gives advantages to manage warp in glass core substrates and bonded stacks for both through glass vias (TGV) and carrier applications. Glass also gives advantages for developing cost effective solutions. Glass forming processes allow the potential to form both in panel format as well as at thicknesses as low as 100 um, giving opportunities to optimize or eliminate current manufacturing methods.

As the industry adopts glass solutions, significant advancements have been made in downstream processes such as glass handling and via/surface metallization. Of particular interest is the ability to leverage tool sets and processes for panel fabrication to enable cost structures desired by the industry. By utilizing the stiffness and adjustable CTE of glass substrates, as well as continuously reducing via size that can be made in a panel format, opportunities to manufacture glass TGV substrates in a panel format increase. We will provide an update on advancements in these areas as well as handling techniques to achieve desired process flows. We will also provide the latest demonstrations of electrical, thermal and mechanical reliability.

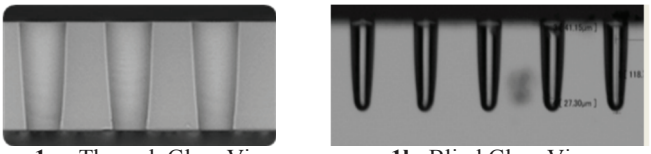
Key words: Through glass via (TGV); glass; panel

INTRODUCTION
New initiatives in semiconductor packaging have created needs for new materials solutions. There has been substantial effort to extend interposer technology for 3D-IC stacking. Multiple solutions are being developed to address some of these needs including traditional interposers utilizing various materials as well as Fan-Out Wafer Level Packaging (FO-WLP), which has become a popular consideration in attempt to achieve lower cost.[1] Furthermore, the proliferation of mobile devices and the Internet of Things (IoT), leads to increasingly difficult requirements in RF communications. These include such requirements as the introduction of more frequency bands, smaller/thinner package size and need to conserve power to increase battery life as new functionality is introduced. Glass has proven to be an excellent solution to these challenges [2].

Glass has many properties that support the initiatives described above. These include high resistivity and low electrical loss, low or adjustable dielectric constant, and adjustable coefficient of thermal expansion (CTE). There has been much work in recent years as researchers demonstrate leveraging glass properties to achieve these objectives [3]-[6].

In order to leverage glass for many RF and interposer applications, it is often necessary to have precision vias for electrical interconnect and other functional purposes. The ability to put precision holes in glass and downstream metallization to create these vias continues to mature towards volume manufacture. Work in recent years has also demonstrated the reliability of these structures in glass [7]-[9].

Over the past several years, there have been significant advances in the ability to provide high quality vias in glass substrates of various formats. Examples are shown in Fig.1. The process employed provides the opportunity to leverage both through and blind vias in both wafer and panel format. The glass substrates with holes have been shown to give strength on par with bare glass, and filled vias have been shown to have excellent mechanical and electrical reliability after thermal cycle tests [9]-[11]. The approximate current best practice capabilities are summarized in Table 1 below. These represent guidance for the current TGV process, but in many cases the capabilities can be extended.



1a: Through Glass Vias **1b**: Blind Glass Vias

Figure 1: Examples of both through glass vias (TGV) and blind glass via (BGV).

In addition to enhanced technical performance, packaging solutions must also be cost effective. Glass forming processes give the ability to form high quality substrates in large formats (>> 1 m in size). Processes can be scaled to deliver ultra-slim flexible glass to thicknesses down to ~100 µm. Providing large substrates in wafer or panel format at

100 µm thickness gives significant opportunities to reduce manufacturing costs. The advantages given by fusion forming process, for example, to supply substrates for electronics applications, has been previously reported [7], [8].

Table 1: TGV specification

Attribute	Current Capability*
Outer Diameter (OD)	25 – 100 um
Minimum Pitch	~2x OD
Type	Through and Blind
Wafer Size	Up to 300 mm
Panel Size	Up to 515 x 515 mm
Thickness (mm)	0.1 – 0.7

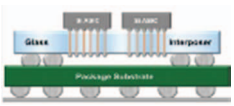
*Approximate.

Glass Material Properties

A. Adjusting the CTE for Carrier and Interposer Applications

Glass material properties are determined by the specific constituents, making it possible to tailor glass composition to achieve a targeted CTE; thus enabling management of stack warp. Previously, we have shown examples of the material properties of two fusion formed glass types, in which it is possible to achieve very different CTE values while maintaining similar mechanical properties [7].

One of the important challenges in 3DIC stacking is reliability due to CTE mis-match and glass provides an excellent opportunity to manage warp of 3D-IC stacks by optimizing CTE. [6] Figure 2 gives an illustration of the challenge of stacking substrates with multiple CTEs in an interposer application. Figure 2a schematically shows Si chips mounted on a Si interposer, which is then mounted on an organic substrate. The CTE mismatch causes failures when the substrates go through temperature cycles. However, if instead of a Si interposer, a glass interposer with CTE in between glass and organic is used, this warp can be better managed and increased reliability realized as demonstrated in work at Georgia Tech's Packaging Research Center (PRC) and illustrated Fig. 2b [6].



2a: CTE mis-match creates reliability challenges.

2b: Utilizing the ability to adjust the CTE of glass helps to manage warp and improve reliability.

Figure 2: Illustration of CTE mismatch in 3DIC stacking.

Another interesting example is to consider carrier applications. One of the driving forces to introduce glass carriers was that one could obtain glass with a very close CTE match to Si for thinning Si interposers. The transparency of glass allows features such as visual bond inspection and laser de-bonding that improves throughput. [13]-[14].

As this approach matures into high volume manufacturing, the ability to adjust the CTE of the glass carrier has become increasingly important. Consider for example the FO-WLP process. A reconstituted wafer is formed by encapsulating Si chips in high CTE molding compound. This structure will have a CTE much greater than Si in most cases and will depend on the materials and details of the layout of the package (size, thickness etc.). The CTE mismatch from the carrier and the fan-out structure will result in excessive warp and make lithography steps extremely challenging. By utilizing glass carriers, the CTE can be optimized to minimize warp of the stack during FO-WLP processing resulting in higher quality fan-out packages. Glass with CTE in the range of ~3-9 ppm/°C is available [15] and other CTEs are also possible depending on requirements.

B. Electrical Performance

As new, higher frequencies used in RF applications are released, the electrical properties of the substrates become increasing important. As a semiconducting material, standard silicon tends to have increased loss at higher frequencies. Work done in collaboration with the Industrial Technology Research Institute (ITRI) in Taiwan illustrates this well. [16] In this work, co-planar waveguides (CPW), micro-strip lines (MS) and co-planar waveguides with 2 vias were constructed on glass and silicon substrates, and impedance matched to ~50 ohm. The structures where then tested up to 20 GHz and insertion loss was characterized. The results are shown in Fig. 2. Since glass is an insulator, there is much less loss as frequency is increased beyond a few 100's of MHz. Given the importance of minimizing power loss at these higher frequencies coupled with the need to continue to reduce package size, glass provides valuable material for all applications working in the GHz range.

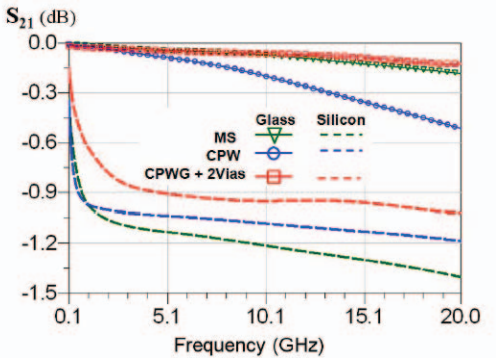


Figure 3: The insertion loss (S_{21}) from transmission lines on glass and standard silicon substrates showing much less loss in glass at higher frequencies.

A good example of leveraging the insulating properties of glass is to provide high-Q inductors and capacitors in a glass-based LC network as recently described [17]. In this work, the high-Q inductors were created by utilizing solenoid inductors shown schematically in Fig. 4a. The top and cross sectional view of the fabricated inductors is shown in Figs. 4b and 4c respectively. High-Q capacitance was achieved by utilizing a metal-insulator-metal construction. Fig. 5 shows the MIM capacitor formed on the same TGV glass substrate.

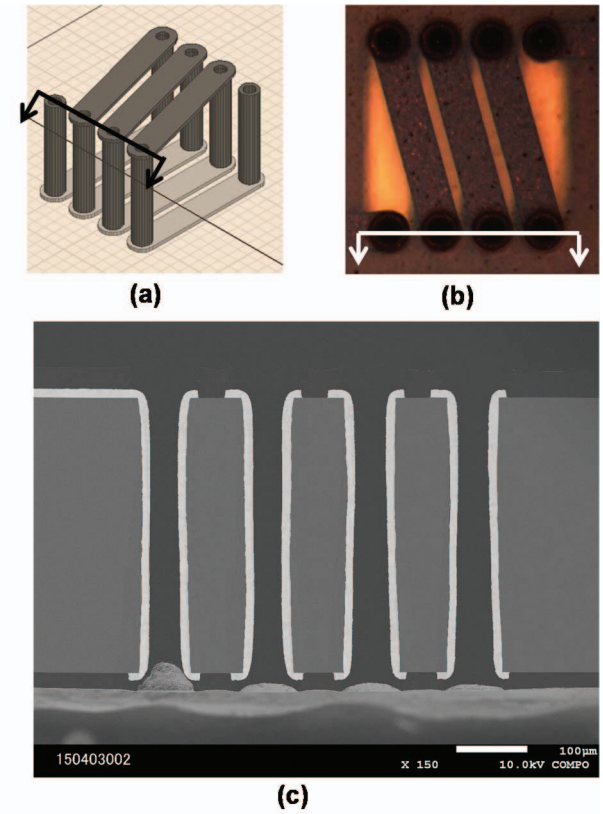


Figure 4: 3D TGV inductor formation. (a) 3D rendering, (b) top-down photograph, (c) cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor

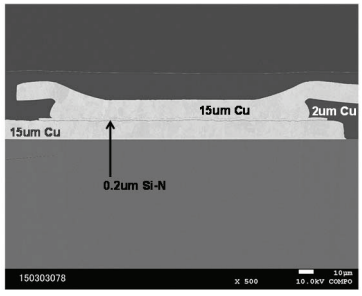


Figure 5: Cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor.

Figure 6 shows a complete die of RF multi-band filters in a single chip with WLCSP solder balls attached and completely singulated using laser dicing.

The TGV IPD parts were mounted on evaluation boards and further tested for both electrical functionality and thermal and mechanical reliability, showing no performance degradation or any board-level reliability issues. The insulating properties of glass provide very high-Q performance.

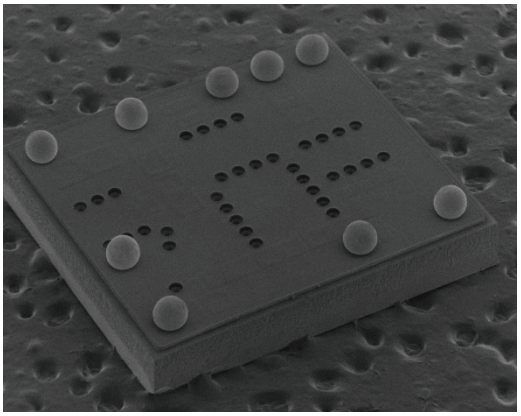


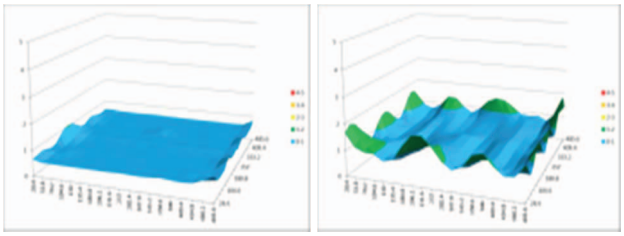
Figure 6: SEM bird's eye view of completed LC networks device.

Form Factor

Another valuable aspect of leveraging glass as a semiconductor packaging substrate is that the forming processes lend themselves to providing large form factors.[7], [8] This is important as the IoT will require billions and even trillions of devices and sensors. Being able to utilize economies of scale given by panel processing is very important.

Recent work has shown significant progress in the ability to process glass panels > 500 mm in size [18]. An important outcome of this work demonstrated one advantage of using glass in this application. Specifically, that the increased stiffness and thermal stability of glass relative to current solutions results in improved flatness (See Fig. 7).

In Fig. 7a, the profile of a 508mm × 508mm panel size glass substrate with two layers build-up after pre-cure processes is shown. Figure 7b shows the profile of organic substrate after same processes. There is ~3x better warpage performance for the glass based substrate. This has important implications in that the improved flatness of the glass based substrate enables finer lines and spacing for redistribution layers relative to organic substrates. This allows high performance devices to be fabricated in a panel format, which provides substantial opportunity for both cost effective and high quality solutions.



7a 7b

Figure 7: (a) Warpage measurement result of glass substrate after two layers build-up (b) Warpage measurement result of organic substrate after build-up

In addition to scaling glass substrate size, it is possible to scale the process to deliver ultra-slim flexible glass to thicknesses down to ~100 um (see Fig. 8). Providing large substrates in wafer or panel format at 100 um thickness gives significant opportunities to reduce manufacturing costs because there is likely to be no need for grinding and polishing operations.

Figure 8: Manufacture of high quality ultra-slim flexible Corning® Willow® Glass provides substantial opportunities to deliver substrates for TGV that do not require post processing.

Handling of ultra-thin glass in standard wafer or panel processing operations can be a challenge. However, solutions are being developed. The Advanced Lift-off Technology (ALoT) is a carrier based solution that is designed to be compatible with high temperatures (> 450 C) without outgas, as well as maintaining compatibility with important process chemistries such as cleaning (SC1, SC2, etc.) and metallization. The process is shown schematically in Figure 9.

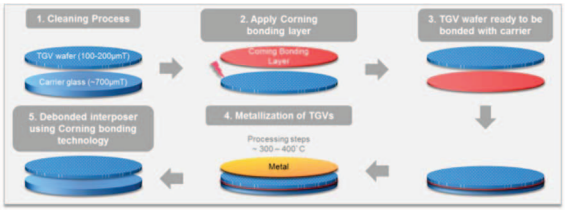


Figure 9: Schematic showing an approach for handling thin glass through metallization.

The approach is to apply a surface treatment on a glass carrier wafer to prevent permanent bond at high temperatures, while maintaining enough adhesion strength to enable via and surface metallization. The thin metallized glass TGV wafer will then be mechanically de-bonded and processed further. This approach is relevant for wafers and panels.

Work recently at RTI International in Research Triangle, NC has been done to demonstrate feasibility of utilizing the ALoT structure to perform metallization of the vias. Glass with 100um thickness and ~30um diameter through vias was provided on a carrier. RTI then applied the seed layer and via fill using a process consistent with the method used to fill blind vias.[9] However, instead of backgrinding to expose the bottom of the vias, with ALoT the thin glass is peeled off mechanically as shown schematically in Fig. 10. Figure 11 shoes the 150 mm bonded wafers.

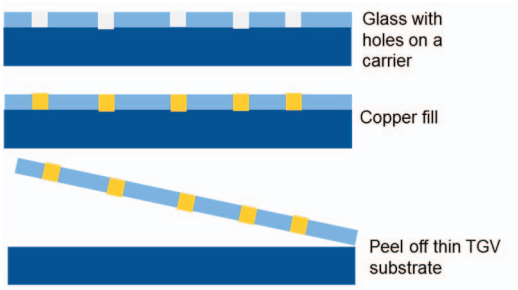


Figure 10: Cartoon of leveraging ALoT technology to metallize through vias in 100 um thick glass.

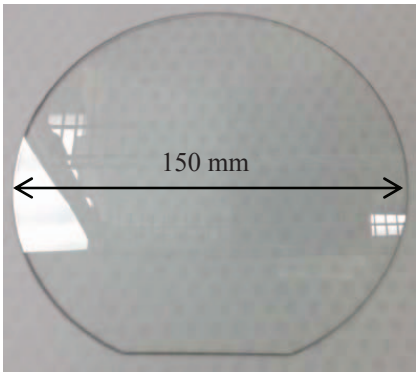


Figure 11: Image 100 um thick glass with 30 um diameter vias temporarily bonded onto a glass carrier using ALoT technology.

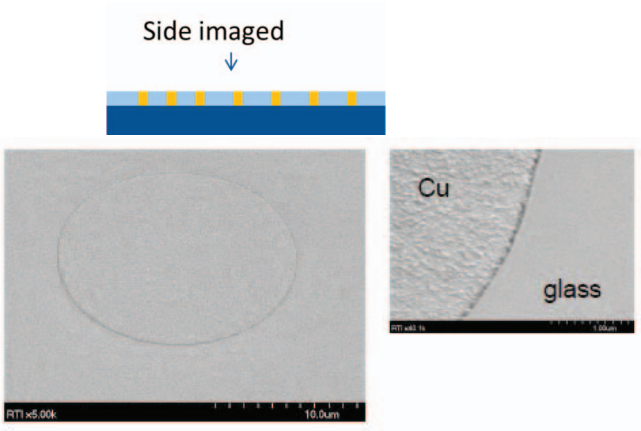


Figure 12: SEM of vias on top surface after planarization.

Figure 12 shows the result after via metallization and overburden removal from the top surface. The thin glass completed processes for via metallization, overburden removal and Chemo-Mechanical Planarization (CMP) and very good planarity of the Cu and glass surface was achieved. After completion of top surface CMP, the wafers were mechanically de-bonded and an SEM image of the TGV on the back surface was collected to evaluate the ability to achieve good planarity without any post-processing (e.g. there was no planarization of the back surface). Figure 13 shows an SEM image of the back surface TGV after de-bond. There is work to be done to achieve perfect bond and planarity, but the result shows the feasibility of using this approach to effectively fill TGV in thin glass. Optimization of this method provides exciting opportunities to dramatically enhance cost effectiveness of providing thin glass solutions by eliminating back-grinding operations and enabling further downstream process optimization. Furthermore, while this demonstration was completed in 150 mm wafer format, it is scalable to 300 mm wafer and even panel formats.

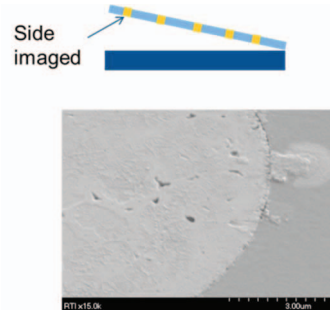


Figure 13: SEM image of bottom of metallized via after de-bond (no polishing).

CONCLUSION

Glass has a number of properties that make it an exciting material for various packaging applications. The electrical performance of glass gives reduced electrical loss relative to silicon. This becomes even more important at high frequencies, which will be used for next generation mobile networks. The important implication would be the ability to increase smart phone functionality while maintaining or extending battery life.

Adjusting material properties like CTE generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications in multiple forms. Furthermore, the ability to form high-quality glass in thin, large sheets enables a number of opportunities to reduce cost. Handling technologies that provide means to effectively process ultra-thin glass are being demonstrated.

Well-formed through and blind vias have been demonstrated and existing metallization technology can be leveraged to generate very good Cu filling performance in glass in both wafer and panel formats. Reliable performance of Cu-filled vias in glass has been demonstrated. These developments make glass an exciting material for next generation packaging applications.

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