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WHERE THE CHIP MEETS THE BOARD

High-Speed Loopback Applications by Utilizing a Differential DPDT MEMS Switch

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Abstract

Ever increased electronic system performance are forcing faster communications between chipsets and memories. Precision high-speed testing of chipsets on design-in-boards is forcing test engineers to Utilizing higher precision components on loopback paths with switches to route the signals back into the DUT becomes widely adopted on design-in-boards method for precision high-speed testing of chipsets. Many of these paths include PCIe 4.0/5.0, Serdes, Ethernet, USB3.x/4, and HDMI.

One of the limiting factors with increasing data rates, such as for PCIe 5.0 specifications, is the switch performance at higher frequencies., The MEMS switch has switching speed of 10μs due to its tiny dimension versus milli seconds range for a bulky EM relays. This allows for a significant increase in test speed and DUT throughput. The small size of the device enables higher test site density so again increasing DUT throughput. The lifespan of the MEMS switch is 3 billion cycles, compared to up to 10 million life cycles for EM relays could help reduce the test system down time.

Design for Signal integrity is critical for optimized PCB layout and fabrication. The session will present details of 2x Through fixture design, PCB design parameters, and how to minimize e impedance discontinuity.

The session will cover the differential signaling scheme, microwave de-embedding techniques, eye diagram test setup and test conditions, and present measured eye-diagram performance.

The eye-diagram performance of the PCIe 5.0 loopback using differential DPDT MEMS switches is optimal both for its eye height and eye width without enabling any pre-emphasis and equalization.

Author(s) Biography

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As part of Menlo's Application Engineering team, Stewart has played an integral role in supporting leading customer designs and assisting them with their product development. Stewart has extensive engineering experience working in the semiconductor industry supporting major global accounts, with expertise at the device level supporting xDSL, 802.11, microwave backhaul, and satellite front-end. Stewart has a Bachelor’s Degree in Electrical Engineering from Hanyang University in South Korea.

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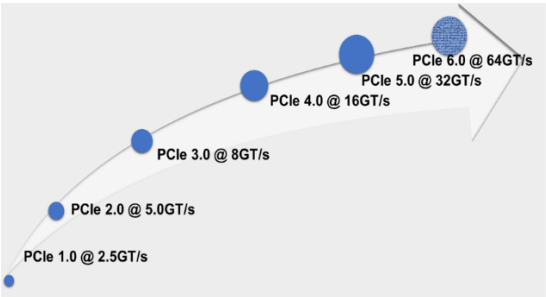
Jangwoo is in charge of SoC Device Interface Board development at Advantest KOREA R&D Center. The main role is Design & PCB electrical stimulation of front-end / back-end interface boards of various applications such as high-speed digital interface, microwave RF, mm Wave RF used in V93K and T2000 SoC ATE Test. Jangwoo has a bachelor's degree in electrical engineering and VLSI design from Hallym University in South Korea.

Introduction

PCI Express (Peripheral Component Interconnect Express) is a common high-speed serial bus; as data consumption increases its required supported speed goes faster and faster. PCIe 5.0 is twice as fast as PCIe 4.0, PCIe 5.0 has a 32 Gbps data rate, compared to 16 Gbps with PCIe 4.0.

Historically Electromechanical relays (EMR) have been used to implement an external loopback test for automated test equipment (ATE) applications, but it become very difficult to use EMR to support testing above PCIe 4.0 specification.

A differential DPDT MEMS switch is designed for use in applications up to PCIe 5.0, two devices are needed to implement the external loopback test. The differential DPDT MEMS switch provides many advantages over existing EM relay solutions.



PCIe Specification	Data Rate(Gb/s) (Encoding)	x16 B/W per dirn*	Year
1.0	2.5 (8b/10b)	32 Gb/s	2003
2.0	5.0 (8b/10b)	64 Gb/s	2007
3.0	8.0 (128b/130b)	126 Gb/s	2010
4.0	16.0 (128b/130b)	252 Gb/s	2017
5.0	32.0 (128b/130b)	504 Gb/s	2019
6.0	64.0 (PAM-4, Flit)	1024 Gb/s (~1Tb/s)	2021

* - bandwidth after encoding overhead

Figure 1: PCIe specification- Data rate has doubled roughly every three years.

The first section of this paper is a quick overview of s-parameters including single-ended and balanced 4-port differential S-parameters, followed by de-embedding concept and the 2X-Through de-embedding method.

The second section is an introduction of an ohmic RF MEMS switch technology and its control methods.

The third section details the PCIe 5.0/PCIe 6.0 loopback board design utilizing differential DPDT MEMS switch and related measurements.

The last section shows measured eye-diagram performance.

An overview of 2-port S-parameters

S-parameters are complex matrix that show reflection and transmission characteristics (amplitude and phase) in the frequency domain.

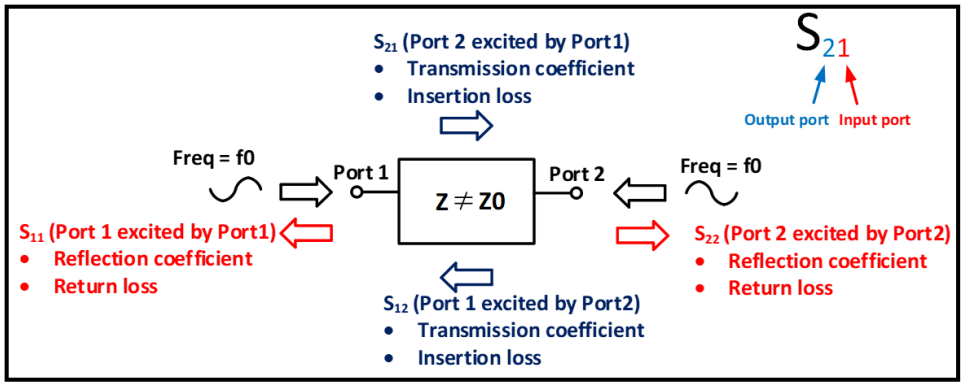


Figure 2. Simple 2-port S-parameters for a reciprocal passive device

A two-port device, with port one on the left and port two on the right, will be represented by S-parameter, a 2x2 matrix: S_{11}, S_{21}, S_{22}, and S_{12}. The numbering convention for S-parameters is that the first number following the "S" is the port where the signal comes out, and the second number is the port where the signal is applied.

For example, S_{21} is a measure of the signal coming out port 2 relative to the RF stimulus entering port 1. When the numbers are the same (for example S_{11} and S_{22}), it indicates a reflection measurement, as the input and output ports are the same.

Transmission parameters S_{21}/S_{12} show insertion loss, phase, and group delay. Reflection parameters S_{11}/S_{22} indicate return loss impedance, admittance, and VSWR.

These measured S-parameters can be transformed into the time domain. With S-parameters, it's easy to simulate waveform under various conditions on simulation software.

Using S-parameters with signal integrity specialist software, for example, Physical Layer Test System (PLTS) from Keysight enables critical multi-domain analysis to observe frequency domain, time domain, eye diagram domain, multi-channel simulation, and crosstalk.

Balanced Devices

Standard Single-ended devices generally have one input port and one output port. Signals on the input and output ports are referenced to ground. On the other hand, balanced devices have two pins on either the input, the output, or both. The signal of interest is the difference and average of the two input or output lines, not referenced to ground.

Differential mode responses can be obtained by balanced measurements and are represented by differential S-parameters.

The format of the parameter notation "S_{abxy}", where "S" stands for S-parameter, "a" is the device output mode, "b" is the device input mode, "x" is the device output logical port number, and "y" is the device input logical port number.

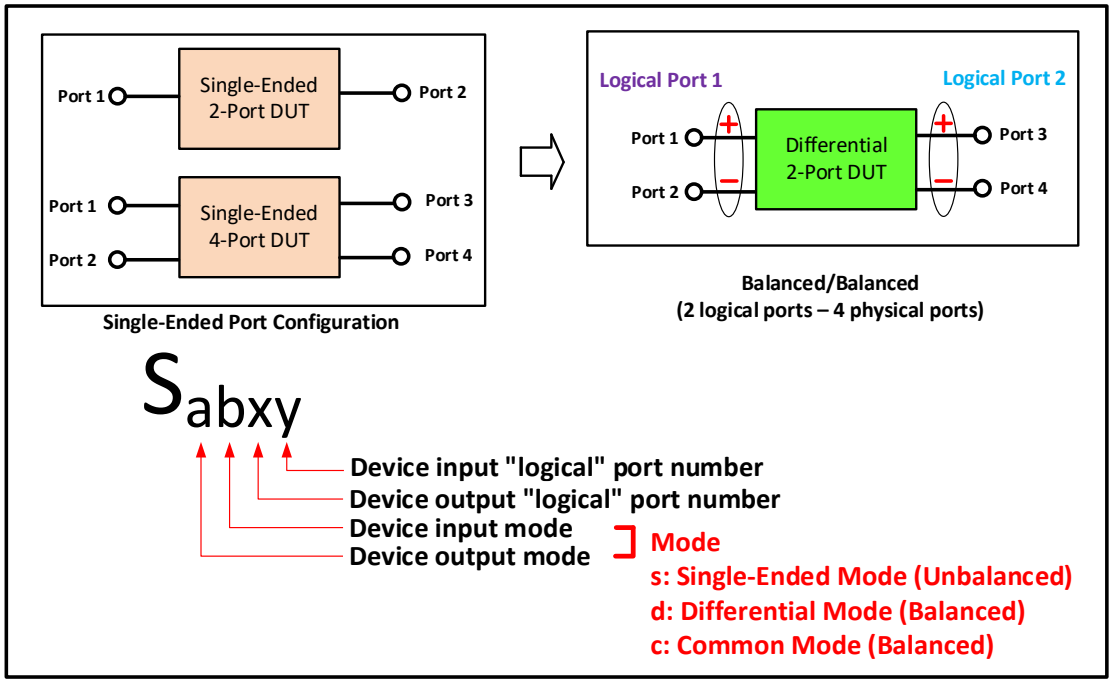


Figure 3. Differential mode responses are represented by Differential S-parameters

Mixed Mode (Balanced) S-Parameters: 4-port Differential S-parameters

Figure 4 describes the possible responses of a differential pair using the mixed mode S-parameter matrix. They are:
S_{ddxy} - A differential signal enters the differential pair and a differential signal comes out
S_{cdxy} - A differential signal enters the differential pair and a common signal comes out
S_{dcxy} - A common signal enters the differential pair and a differential signal comes out
S_{ccxy} - A common signal enters the differential pair and a common signal comes out

The focus is mostly on these 4 S-parameters, S_{DD11}, S_{DD12}, S_{DD21}, and S_{DD22}.
For S_{DD11}, it refers to the differential response at logical port one, excited by differential logical input at port one. The S_{DD11} and S_{DD21} are related to the differential return loss and insertion loss. The S_{CD21} refers to mode conversion and EM generation, and S_{DC21} is EM susceptibility.

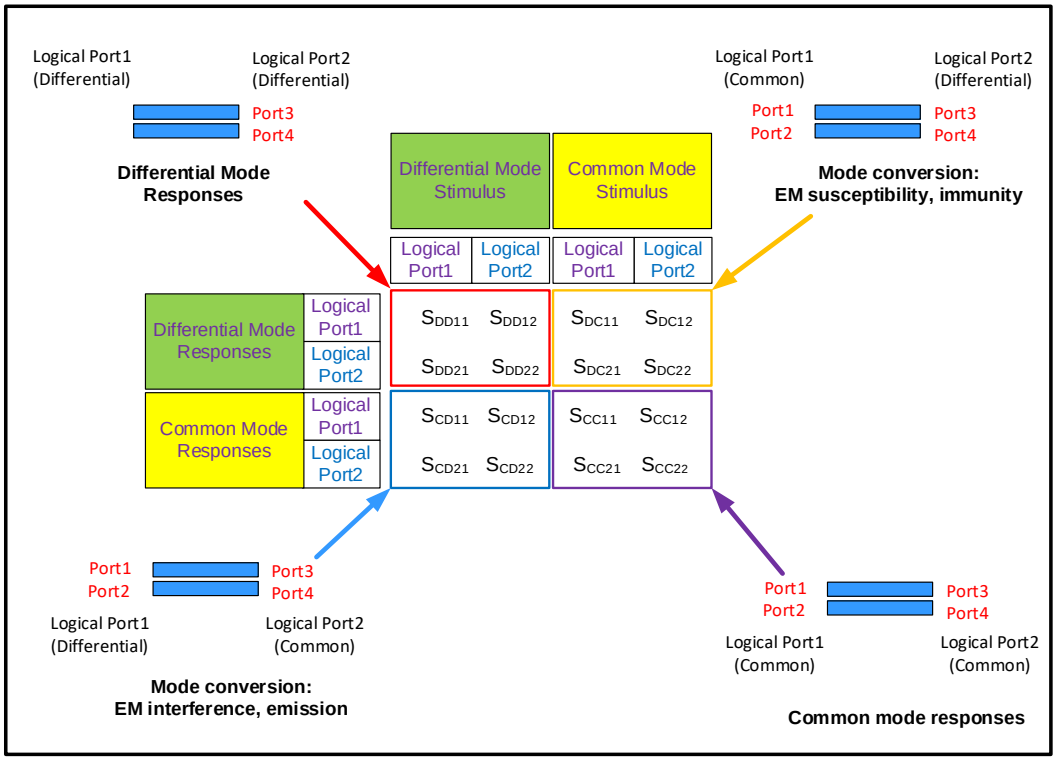


Figure 4. 4-port Differential S-parameters

Signal Integrity Measurements using a VNA

A modern VNA can be used for S-parameter measurement and fixture de-embedding in the frequency domain and signal integrity measurements such as TDR measurement and Eye-Diagram performance. Time domain analysis is useful for measuring impedance values along a transmission line and for evaluating a device problem (discontinuity) in time or distance.

For accurate TDR measurements, the analyzer should be calibrated. The measurement start and step frequencies should be equal. This is necessary for TDR measurements.

For example, if the start frequency is 10MHz and stop frequency is 50GHz, then the number of measurement points would be five thousand.

Balanced measurements are calibrated in the same manner as single-ended (standard) measurements. However, for highest accuracy, you must choose Thru paths so that each transmission path of the balanced measurement is represented. For a Balanced input/Balanced output topology, this means that FOUR Thru connections should be made.

For example:

Balanced Port 1 is ports 1 and 2
Balanced Port 2 is ports 3 and 4
Thru paths to be calibrated should be: Ports1-3, 1-4, 2-3, and 2-4.

De-embedding technique: 2x-thru de-embedding

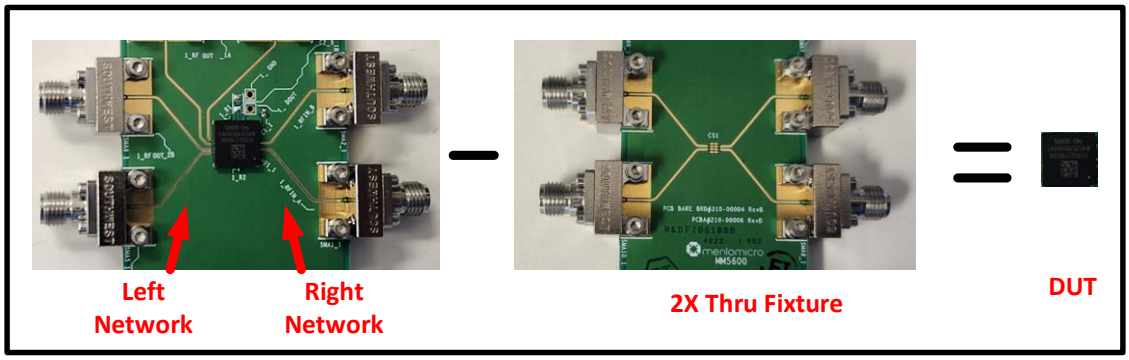
As the device under test (DUT) is typically mounted on a board with input/output RF traces and connectors, it is desired to de-embed impact of the RF trace and connectors from measurement to obtain the true DUT (device under test) performance. So, it is required to model the fixture as additional “networks” as left and/or right as shown in Figure 5.

Various mathematical algorithms can be used for modeling and 2X -thru typically is the most accurate method of fixture compensation.

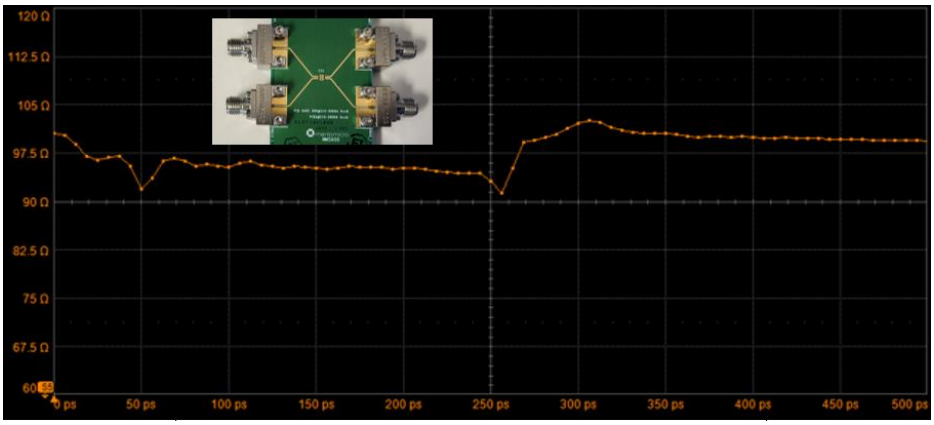
The 2X-thru fixture has same structure for the DUT and for the 2X-thru alone. First, measure the 2X-thru with VNA after coaxial calibration. Then, mathematically divide the 2X-thru to two halves to acquire the S-parameters of just the left or right network.

De-embed the fixtures from the DUT measurement to achieve the real DUT characteristics.

In order to ensure an accurate de-embedding, the return loss and insertion loss of the 2X-Thru Test Fixture should not cross each other within DUT measurement frequency range of interest, in fact there should be greater than 5 dB separation.



(a)



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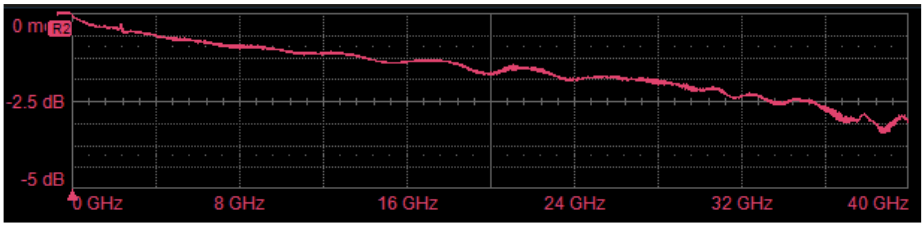


Figure 5. (a) 2x-thru de-embedding concept (b) TDR measurement (c) S_{DD21} measurement

Introduction of a RF MEMS Switch

The loopback board uses two of the differential DPDT MEMS switches, MM5600 devices, utilizing the Ideal Switch technology from Menlo Microsystems Inc. Every switch is individually controllable and can be daisy-chained for multiple switches. The test board includes a control interface and a 90 VDC driver for actuating the switches.

The unit cell architecture of the MEMS switch is illustrated in Fig 6 (a) and (b) and SEM images of the unit cell Fig 6 (c) and Through Glass Vias Fig 6 (d).

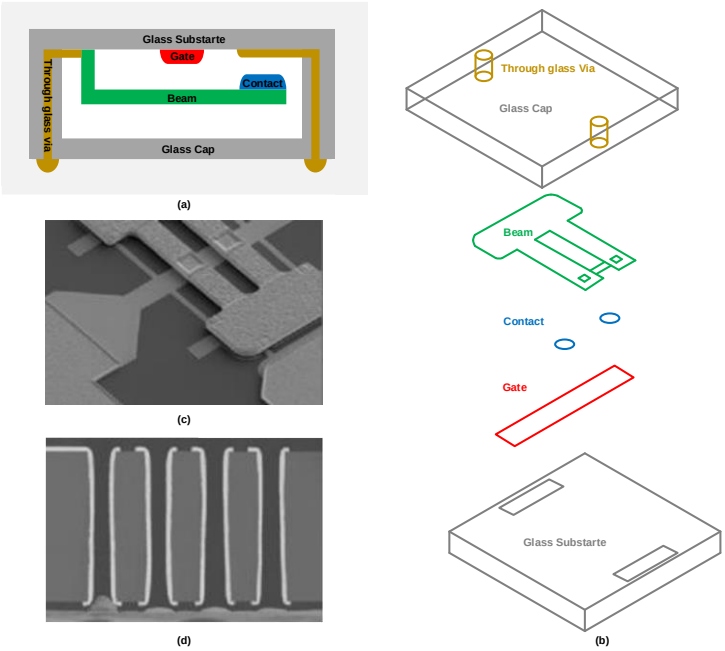


Fig 6. (a) (b) The Ideal Switch consists of glass substrate, glass cap, through glass via, beam, contact, and gate. (c) The unit cell - only 50µm x 50µm.(d) Through Glass Vias, miniaturized packaging with highest performance.

The MEMS switches are activated via electrostatic force, and thus require a high voltage source for switching operation. The gate of the switch is set for a bias of 0 VDC, which places the metal cantilever beam in a non-deflected (off) state. Thus, the path between RF input and output is isolated with an air gap, like a traditional mechanical relay. When the gate is set to its required actuation voltage of +89V, the electrostatic force that exists between the gate and cantilever beam is strong enough to cause it to deflect downward, forming a connection with the contact and closing the switch (on state).

The MM5600 device has a built-in high voltage driver with external high voltage supply , the MM5620 device even has a built-in charge pump as shown in Figure 7.

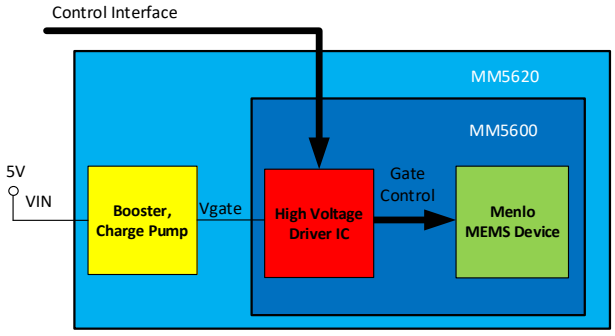


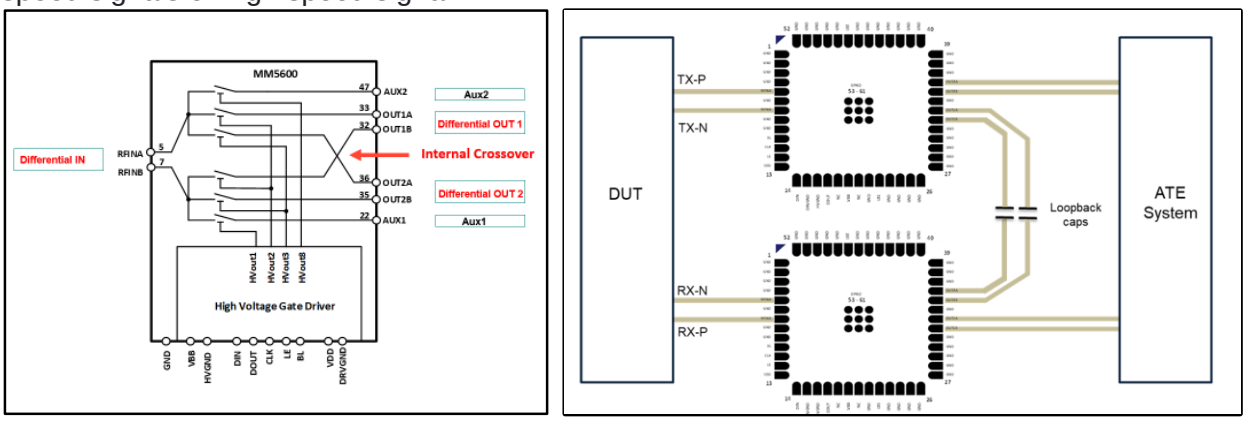
Figure 7. Control of the Ideal Switch

As mentioned, the Electromechanical Relays (EMR) have been used for loopback tests up to PCIe Gen4, but it has performance limitations for PCIe Gen 5 applications. There are many significant advantages to using the MM5600 and MM5620 switches over existing EM relay products:

- Fast switching: The MM5600/MM5620's ultra-fast switching speed (< 10 µs operation time and < 2 µs release time) is 1000x faster than EM relays, enabling reduced test time and lower cost-of-test.
- Reliability: The MM5600/MM5620 provides unmatched reliability and can operate with more than three billion switching cycles, resulting in reduced downtime, maintenance and cost and a 1000x longer lifetime compared to conventional EM relays.
- Stability: The MEMS switch is extremely stable over hold down time, cycling and temperature.
- Compact design: The MM5600's small-footprint/low-profile design (8 mm x 8 mm x 1.6mm QFN package) provides a 90 percent reduction in size over conventional EM relay solutions. This significant reduction enables more parallel tests and easier top and/or bottom routing.
- Power efficiency: The MM5600 operates at less than 0.08 mW, a 99 percent reduction in power consumption compared to EM relays, making it the most energy-efficient high-speed DPDT switching solution available.
- Leading IP3 linearity: The MM5600 achieves an IP3 linearity of more than +90 dBm, enabling large reductions in distortion and delivering up to a 10,000x improvement over existing EM relays.

PCIe Gen 5.0 – External Differential Loopback using Two MM5600 Devices

For high-speed path (32 Gbps), the differential output signals from the DUT are going through the AC coupling capacitors (200nF) and then coming out to the differential inputs of the DUT. The other differential path can be used for DC measurement or low-speed signals or high speed signal



(a) (b)

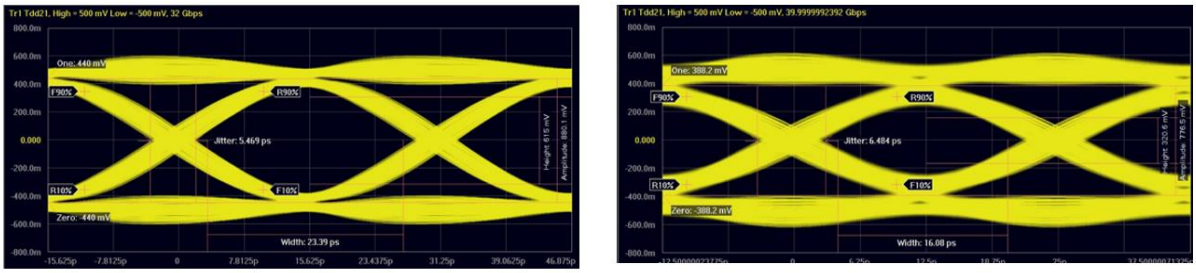
Figure 8. (a) MM5600 Functional Block Diagram. (b) 2 x MM5600 (8mm x 8 mm LGA) in a test system (Top View).

MM5600 High-Speed Eye-Diagram Performance

The Figure 9 and Table 1 show measured eye-diagram performance at 32 Gbps and 40Gbps. Test conditions for measurements are as below:

- 2^{15}-1 PRBS signal.
- PRBS output is 1000mVp-p NRZ at RF connectors.
- RF connector and RF traces are de-embedded.

- Measured differentially on the MM5600 EVK board.



(a) (b)

Figure 9. Eye-Diagram Performance (a) 32Gbps (b) 40 Gbps

Test Cases	Bit rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Jitter (P-P, ps)	Rise Time (10-90, ps)	Fall Time (90-10,ps)
Out 2 ON	32.000	615.0	23.4	5.47	21.3	21.3
Out 2 ON	40.000	320.6	16.1	6.48	19.9	19.9

Table 1. MM5600 Eye-Diagram Performance

PCIe Gen 6.0 – External Differential Loopback using the MM5620 Device

The MM5620 device is a Dual SP3T MEMS switch supporting the high-speed differential signal switching required in PCIe Gen 6 and SerDes applications. The MM5620 is based on Menlo's Ideal Switch® technology and can operate up to 64 GT/s or 20 GHz for high-performance applications.

The MM5620 has low insertion loss, fast switching speed, and can operate with greater than 3 billion switching cycles. The MM5620's integrated charge pump and driver can be controlled through SPI or GPIO interfaces by a host processor. The design fully integrates the loopback capacitors and offers a considerable 90% reduction in size when compared with comparable high speed relay solutions.

Figure 10 shows a simplified functional block diagram and pinout of the MM5620 device.

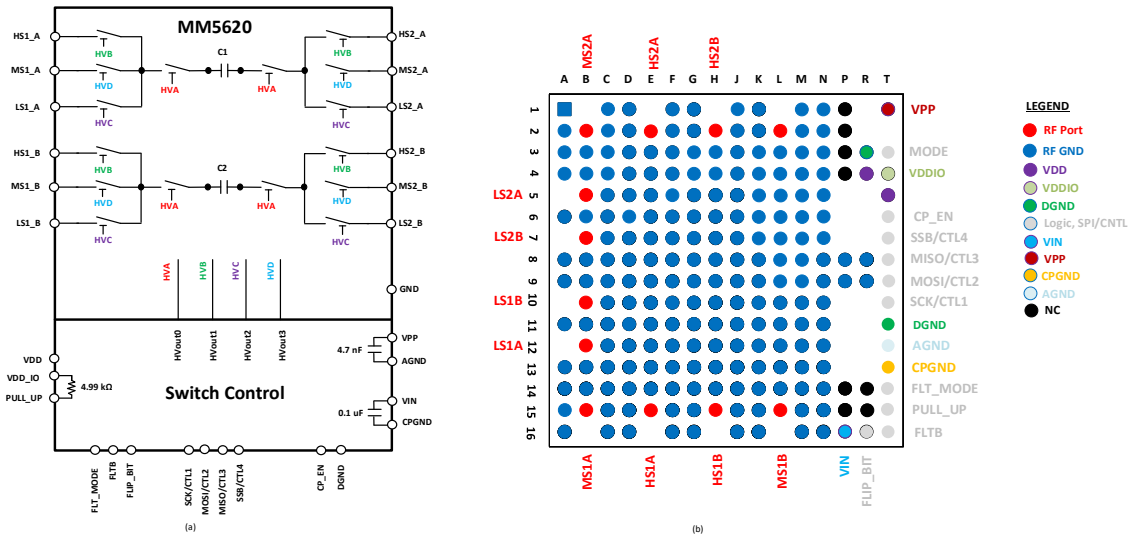
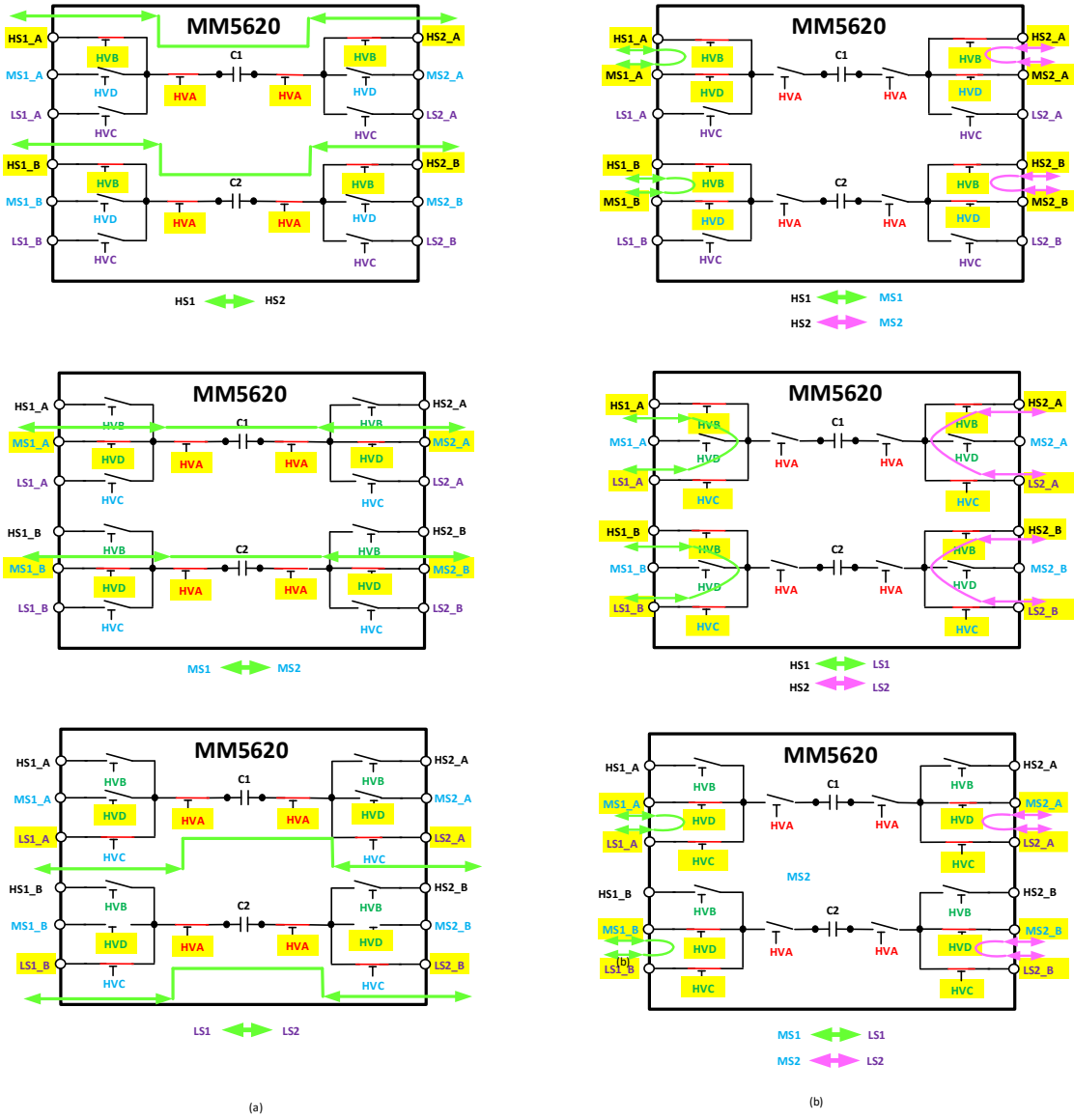


Figure 10. (a) Functional Block Diagram (b) MM5620 (8.2mm x 8.2 mm LGA) Top View

There are six possible controls as shown in the Figure 11. Three are the loopback signal paths through AC coupling capacitors and the other three are the loopback signal paths without AC coupling capacitors.

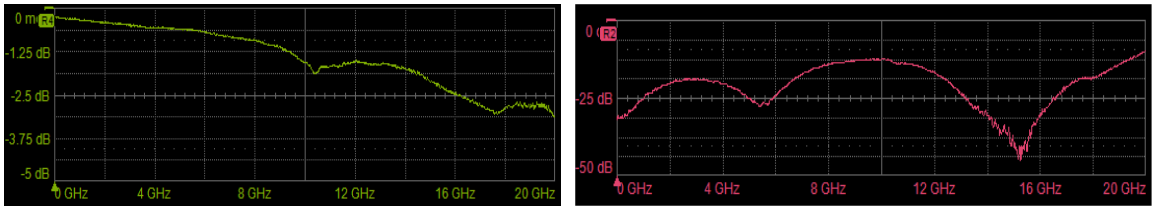


Input (Output)	Output (Input)	HVA	HVB	HVC	HVD
HS1	HS2	HIGH	HIGH	LOW	LOW
HS1	MS1	LOW	HIGH	LOW	HIGH
HS1	LS1	LOW	HIGH	HIGH	LOW
MS2	HS2	LOW	HIGH	LOW	HIGH
MS2	LS2	LOW	LOW	HIGH	HIGH
MS1	MS2	HIGH	LOW	LOW	HIGH
LS2	HS2	LOW	HIGH	HIGH	LOW
LS1	MS1	LOW	LOW	HIGH	HIGH
LS1	LS2	HIGH	LOW	HIGH	LOW

(c)

Figure 11. (a) Loopback signal paths through AC coupling capacitors. (b) Loopback signal paths without AC coupling capacitors (c) Signal Path Control- Truth table

Figure 12 shows differential insertion loss (S_{DD21}) and return loss (S_{DD11}) for the high-speed loopback path



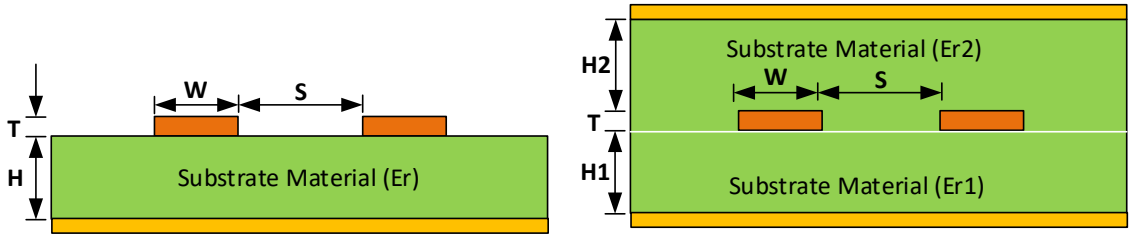
(a) (b)

Figure 12. (a) Measured insertion loss performance. (b) Measured return loss performance.

High-Speed Digital PCB Design

To achieve a good high-speed PCB design to meet the specific design target, it is very important to get deep understanding of your fabrication houses' capability and details of their design rules in advance, then work very closely together with them.

Most high-speed differential lines use either an edge-coupled microstrip or an edge-coupled stripline. A differential pair can be implemented as loosely or tightly coupled. Figure 13 shows differential Microstrip vs. differential Stripline construction, and Table 2 describes pros and cons between the two routing options.



(a) (b)

Figure 13. T(Copper Thickness), W(Trace Width), S (Spacing), H (Substrate Height), and B (Substrate height) (a) edge-coupled microstrip (b) edge-coupled stripline

Routing	Advantage	Disadvantage
Loosely Coupled	• Thinner dielectrics required for the same trace width • Less sensitivity to trace-to-trace variations provides better impedance control	Consumes more PCB area
Tightly Coupled	• Higher routing density • Smaller trace width for the same trace impedance • Better common mode noise rejection	Impedance control highly sensitive to trace-to-trace variations

Table 2. Loosely vs. Tightly Coupled Trace Routing

The signal attenuation is from the substrate material include dielectric loss, conductor loss, reflections due to mismatched impedance, and radiation loss. Losses due to radiation are usually very small and negligible. The remaining losses can be attributed to the various properties of the substrate material choice. Material properties that directly affect the link performance include:

- Loss tangent (tan(δ)/Df)
- Dielectric constant (Er/Dk)
- Fiberglass weave composition
- Copper surface roughness

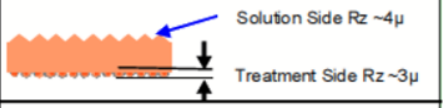
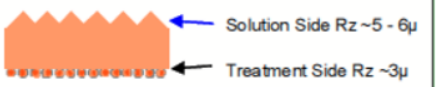
Oz	Generic Name	OM Product Name	Description
0.5oz	RTF or DSTF	MLS	
1oz	RTF or DSTF	MLS	
2oz	RTF or DSTF	MLS	

Table 3. Surface Roughness

The skin depth also needs to be considered; at RF and microwave frequencies the current is conducted at the surface of transmission line and that depth of current flow is called skin depth. For low loss designs it is best to avoid Nickel in the plating (ENIG/ENEPIG), as Figure 14 shows even a very thin layer of Nickel will cause high loss due to it's low skin depth and the majority of the current being carried in the high loss Nickel layer.

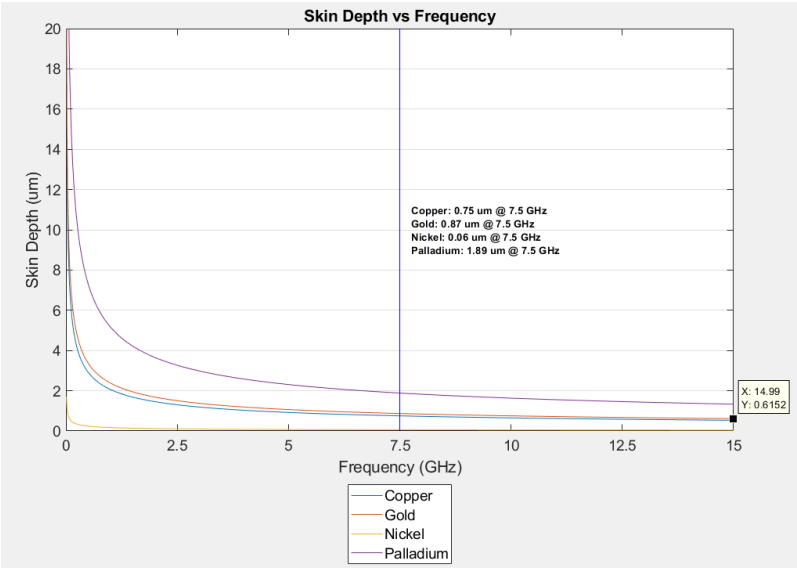


Figure 14. Skin Depth vs Frequency – 0 – 15 GHz

It is important to choose better dielectric material with low dielectric constant, low-loss tangent, better surface roughness, Reverse Treated Copper Foil, and better PCB finish (plating method) such as EPIG, ISIG, EPAG, etc. if the design has high-speed routing on top/bottom layer.

There are two MM5600 devices used for the loopback functionality. These need to be placed as close as possible to each other. To optimize transmission line design, wider and shorter traces are better to minimize the insertion loss.

For the differential signals, Routing should be smooth with minimum bends and tight length matching is required.

Stitching vias are required to be placed along all the high-speed routing from DUT to Connectors. If space allows, it is ideal to implement two rows of stitching vias along the RF signals routing as operating frequency approaches 20 GHz.

To provide a proper de-embedding, the 2x-through needs to be implemented with symmetrical routing and placement. The calibration structures should have a symmetric placement and routing similar to the one done in high-speed routing connected to the DUT but have 2 times the trace length and with a connector at the end of each trace.

Optimizing via transitions is necessary to minimize the impedance mismatch. A TDR simulation using 3D EM tools is a good method to check the impedance of vias and optimize it.

Soldermask needs to be removed on high-speed traces.

Although it takes additional time, confirmation by running post-layout full 3D EM simulation, to obtain s-parameter, TDR, and eye diagram results, is a must to ensure that the board layout can meet the requirements.

There are some considerations while designing high-speed PCBs and measuring RF performance as below:

Connector assembly issues (Edge Launch Connector)

Connector pin misalignment was found as pictured below.

Figure 15. (a) Bad, misaligned (b) Good, aligned

There is gap between the connector and the edge of the board when the connector is installed due to the board edge issue as shown in Figure 16. There is no copper underneath, this will cause impedance to be inductive and it will affect return loss performance.

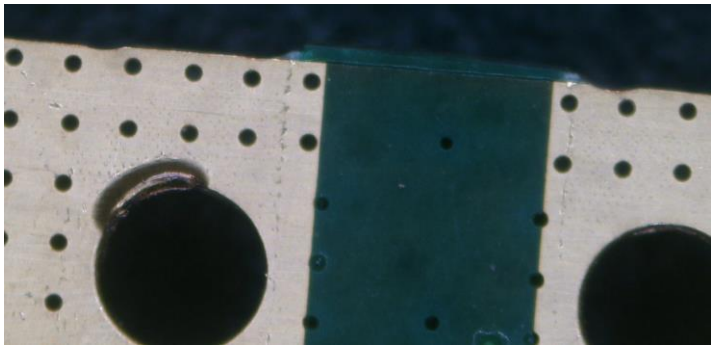


Figure 16. Not enough material removed from edge

Ensure connector pins are centered on transmission line and there is no gap between the connector and the edge of the board as shown in Figure 17.

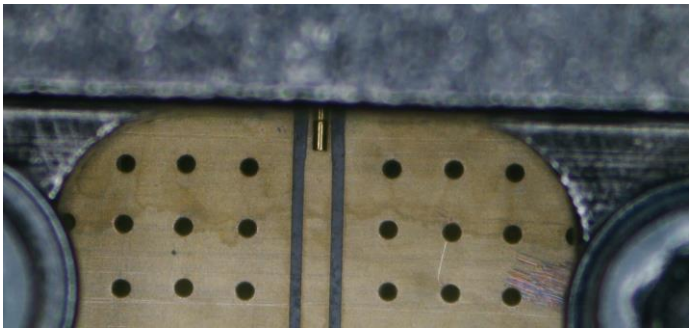


Figure 17. Corrected connector installation

Plots below show differences before and after rework (red/green is before, blue/orange is after)

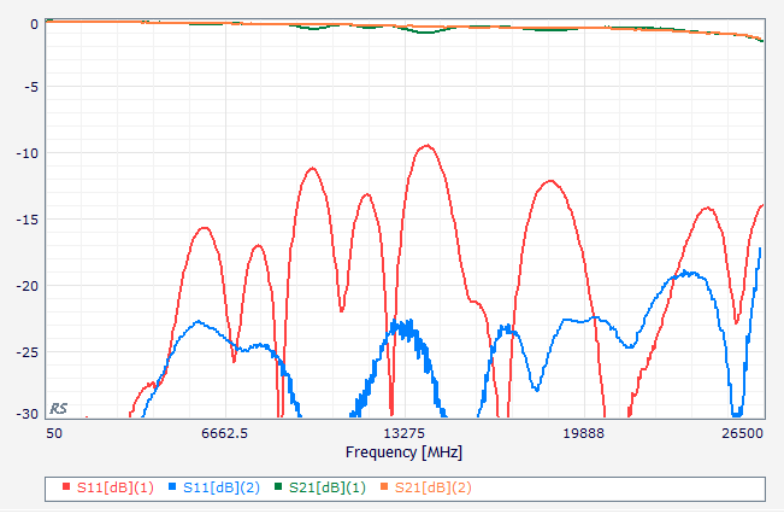


Figure 18. Plots showing differences before and after rework

Selecting an RF Connector for an evaluation board

The Nyquist frequency is 16GHz for both PCIe Gen5 and Gen6; for digital signal, need to use at least K connector (2.92mm, up to 40GHz) or V connector (1.85mm, up to 67GHz).

For high-speed, high performance RF board, it is recommended to use a solderless PCB connector as shown example in Figure 19.

For the edge launch connector, copper underneath of the connector should be flushed with the board edge, otherwise the signal will lose reference and will get an inductive spike from that area which will affect performance.

(a) (b)

Figure 19. (a) Edge Launch Connector(2.92mm/2.4mm) (b) solderless PCB connectors – 45 degree (2.92mm/1.85mm)

VNA Coaxial Cable Assemblies

For accurate RF measurements it is important to use high quality coax cables, RF connectors, calibration kit, and 50-ohm terminators to terminate the unused ports. The distance between connectors should be reviewed to make sure it can be plugged without unnecessary additional cables and adaptors.

(a) (b)

Figure 20. (a) Cable cannot be plugged (b) Cable can be plugged directly

2X-thru Fixture Simulation

Digital signal is a very broadband signal and simulation of the 2x-thru needs to cover the 3rd harmonics of its fundamental frequency, i.e. 16GHz x 3 is 48GHz. The insertion loss notch was noticed while measuring the on-board 2x-thru fixture Fig (a) and (c), because the simulation was performed up to 30GHz. The notch impacts the de-embedding process. The Fig (b) and (d) show newly designed 2x-thru, its insertion loss is monotonic up to 50 GHz and good separation between insertion loss and return loss.

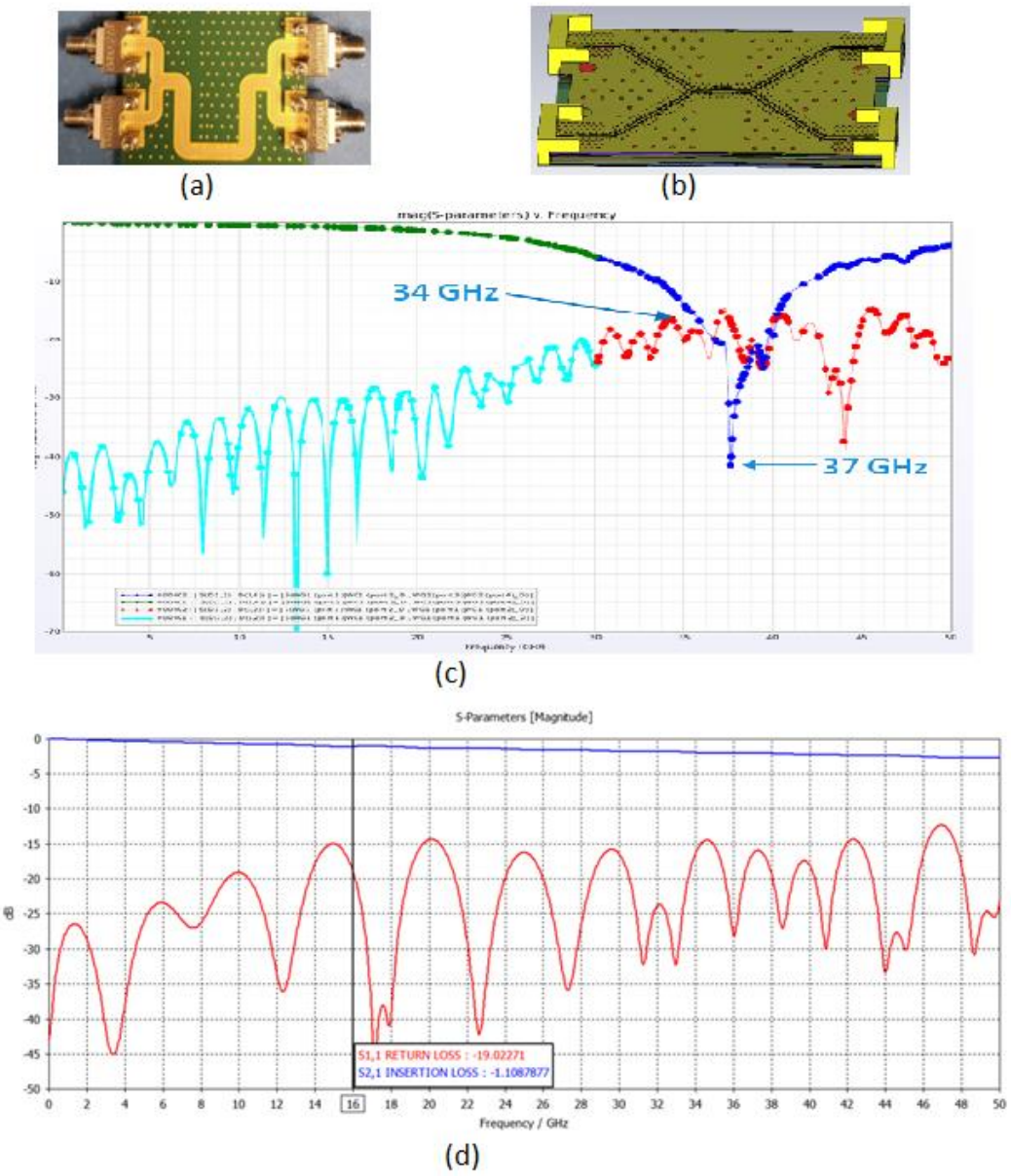


Figure 21. (a) old 2x-thru fixture (b) new 2x-thru fixture (c) Sim result from the old fixture , IL found at 37GHz (d)Sim result up to 50GHz, IL is monotonic and no IL notch observed

MM5600 Loopback Circuit with Evaluation Board

Deomstrated here is a test coupon board to evaluate the high-speed loopback circuit to make sure the load board design can meet the PCIe Gen5.0 requirements.

Figure 22 (a) shows the sideview of the load board structure and (b) for its topview. This is the first topology, which is the full path case including a charge pump circuit, control interface, and two MM5600 devices, AC coupling caps and four 1.85mm RF connectors.

Figure 23 shows evaluation board design with two different topologies. Case 1 Tx-Rx loopback using 2 x MM5600. Case 2 MM5600 replaced by transmission lines that simulate the MM5600 connection.

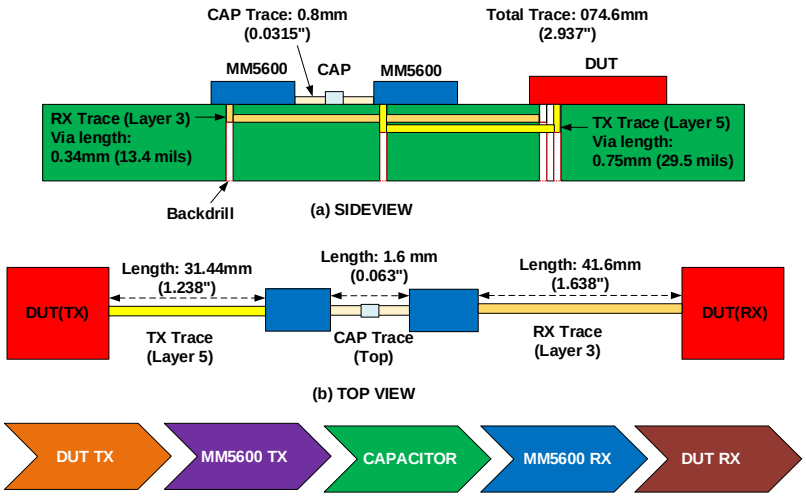
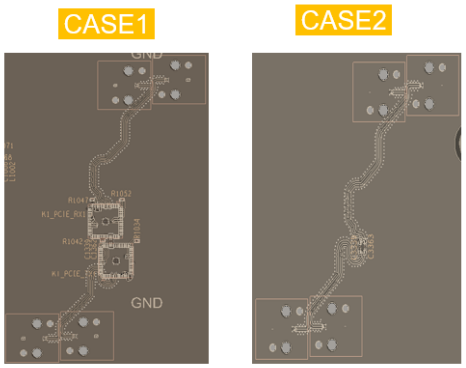


Figure 22. (a) Load Board Structure (Sideview) (b) Load Board Structure (Topview)



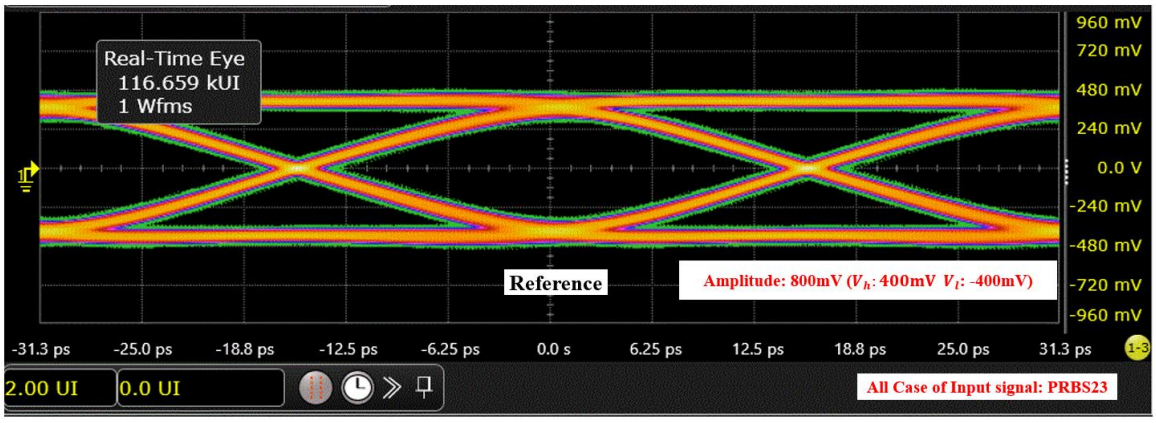
CASE	TOPOLOGY	DETAIL
1	TX-RX Loopback with MM5600	MM5600 mounted and full path case.
2	TX-RX Loopback without MM5600 (Connected to Trace)	MM5600 is not mounted, and the internal circuit of MM5600 is mounted as a trace

Figure 23. Evaluation board design with two different topologies

Eye-Diagram Performance of the Evaluation Board

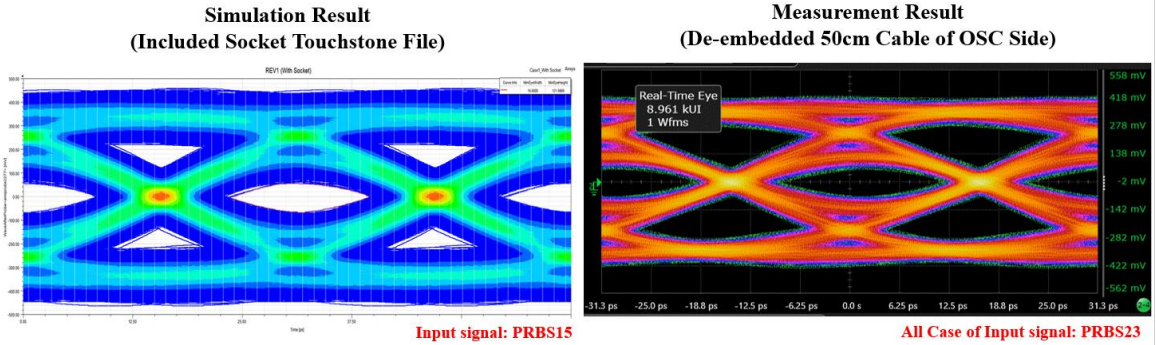
The eye-diagram performance of the evaluation board has been measured and compared with the simulation result for the case 1.

Figure 24 shows a baseline of 32Gbps with an eye height of 510mV. Figure 25 is a measured 32Gbps signal with an eye height of 108mV without pre-emphasis or equalization enabled, and both RF connectors and transmission lines are not de-embedded.



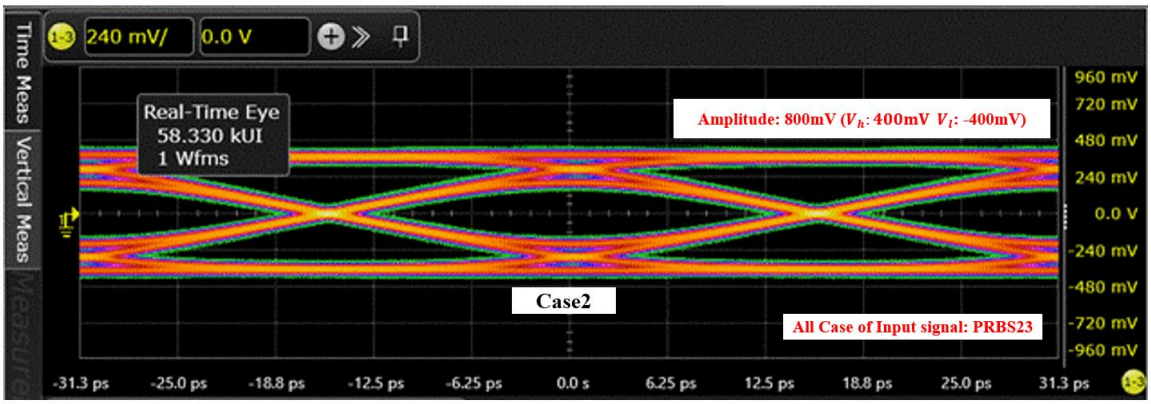
Reference Result	
Min. Eye Width	Min. Eye Height
26.46ps	510.0mV

Figure 24. Baseline measurement: Reference result without the eval board



Reference Result (Measurement)		Simulation Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	15.5ps	121.0mV	20.21ps (76%)	108.0mV (22%)

Figure 25. Case 1, PCIe Gen5 - 32Gbps Evaluation Result. NRZ, 800mVpp
(a) Simulation Result, PRBS 2^{15}-1, (b) Measured result, PRBS 2^{23}-1



Reference Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	25.00ps (95%)	270.0mV (53%)

Figure 26. Case 2, 32Gbps Loopback without MM5600 (Connected to Trace), Measured result, NRZ, 800mVpp, PRBS 2^{23}-1

MM5620 Eye-Diagram Performance – High Speed Loopback Path

The Figure 28 and Table 2 show measured eye-diagram performance at 32 GBaud. Test conditions for measurements are as below:

- 2^{23}-1 PRBS signal.
- PRBS output is 800mVp-p NRZ and 1200mVp-p PAM4 at RF connectors.
- RF connector and RF traces are de-embedded.
- Measured differentially on the MM5620 Evaluation board.

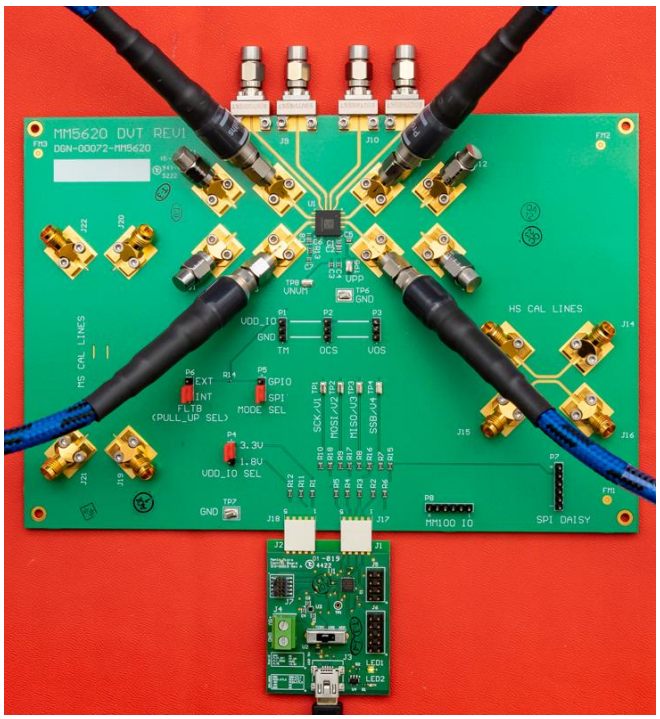


Figure 27. MM5620 Evaluation Board

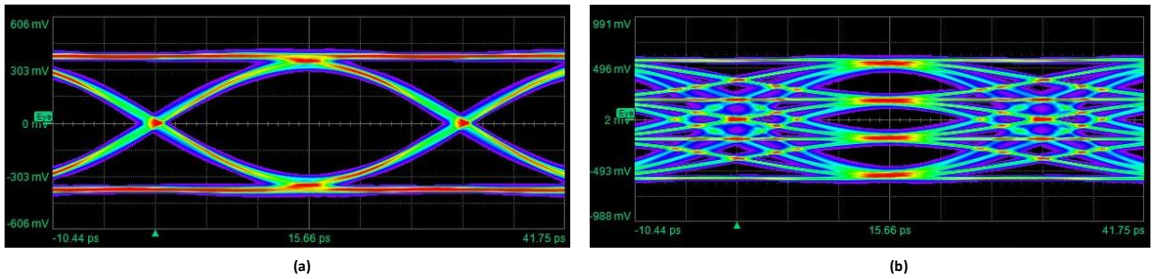


Figure 27. Eye-Diagram Performance (a) PCIe Gen5, 32Gbps, NRZ, 800mVpp, Measured Result, PRBS 2^{23}-1 (b) PCIe Gen6, 32GBaud, PAM4, 1200mVpp, Measured Result, PRBS 2^{23}-1

Conclusion

The MM5600 device, Menlo's first differential DPDT switch, is introduced. This device can support PCIe Gen5.0 loopback test and can be used for PCIe Gen4.0 applications for improved performance and reliability by replacing EMR relays on the existing load boards.

We have presented simulated and measured eye-diagram performance of the PCIe Gen 5.0 loopback board utilizing two MM5600 devices to ensure that the load board design can meet the PCIe Gen5.0 requirements. An excellent eye-diagram performance is achieved at 32Gbps signal with an eye height of 108mV without pre-emphasis or equalization enabled, and both RF connectors and transmission lines are not de-embedded.

Then the MM5620 device, differential dual SP3T switch, is introduced; it can support PCIe Gen6.0 loopback test.

We have also presented simulated and measured eye-diagram performance of the PCIe Gen 6.0 loopback board utilizing only a single MM5620 device. An excellent eye-diagram performance is achieved at 64GT/s PAM4 signal with an eye height of 154 mV without pre-emphasis or equalization enabled.

Test engineers requiring an RF switch that meets the requirements for PCIe 4.0/5.0/6.0 performance while saving crucial space in the load board and improving reliability, will appreciate a MEMS-based approach solution that is also cost competitive to EM and solid-state solutions.

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