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Santa Clara Convention Center

High-Speed Loopback Applications by Utilizing a Differential DPDT MEMS Switch

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SPEAKERS

Stewart Yang

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As part of Menlo's Application Engineering Team, Stewart has played an integral role in supporting leading customer designs and assisting them with their product development. Stewart has extensive engineering experience working in the semiconductor industry supporting major global accounts, with expertise at the device level supporting xDSL, 802.11, microwave backhaul, and satellite front-end. Stewart has a Bachelor's degree in Electrical Engineering from Hanyang University in South Korea.

Jangwoo Lee

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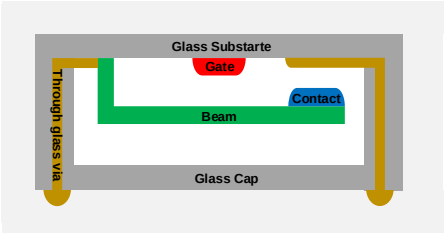
In charge of SoC Device Interface Board development at ADVANTEST KOREA R&D Center. The main role is Design & PCB electrical simulation of front-end / back-end interface boards of various applications such as high-speed digital interface, microwave RF, mmWave RF used in V93K and T2000 SoC ATE Test. Jangwoo has a bachelor's degree in electrical engineering and VLSI design from Hallym University in South Korea.

Agenda:

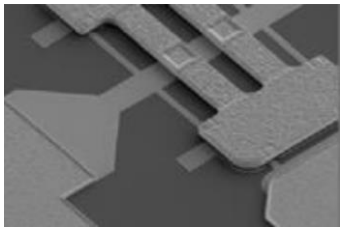
- Introduction of an RF MEMS Switch
- MM5600 Differential DPDT Switch, Switch Control
- PCI Express Speed – Gen4/5/6
- S-Parameter Overview, Signal Integrity Measurements using a VNA
- De-embedding Technique: 2x-thru De-embedding
- MM5600: DPDT Differential Switch – Signal Integrity Measurements
- High-Speed Digital PCB Design
- MM5600/MM5620 Loopback Circuit with Evaluation Board
- Eye-Diagram Performance of the Evaluation Board
- Summary and Conclusion

Introduction of an RF MEMS Switch

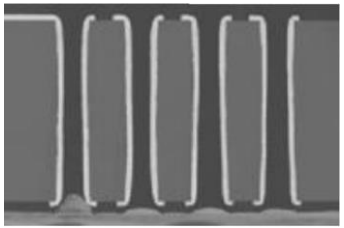
- The unit cell architecture.
- The Ideal Switch consists of glass substrate, glass cap, through glass via, beam, contact, and gate, (a) & (b).
- The unit cell - only 50μm x 50μm, (c). Through Glass Vias, miniaturized packaging with highest performance, (d).



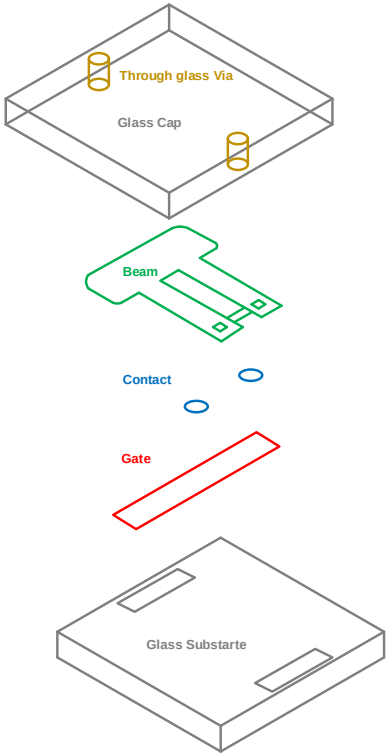
(a)



(c)

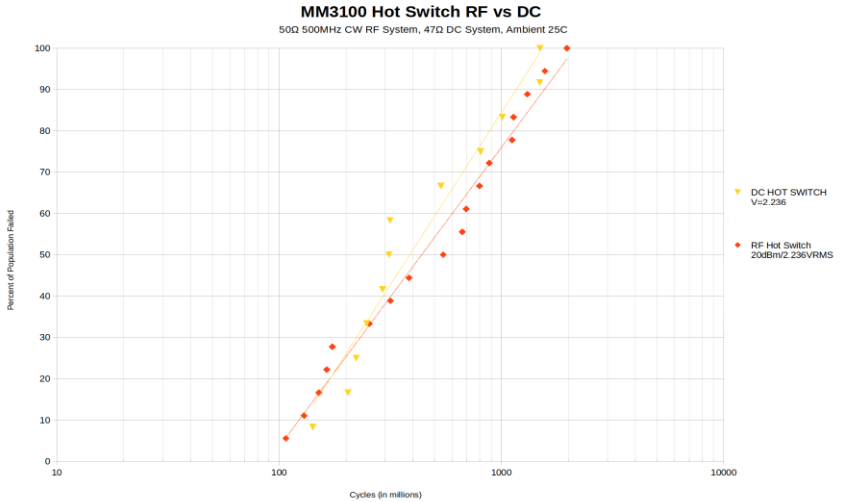


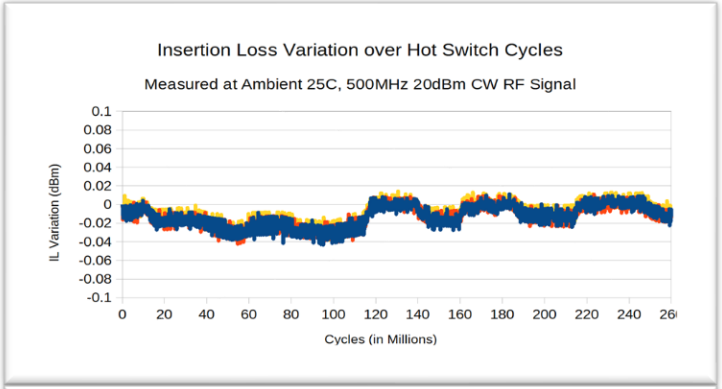
(d)

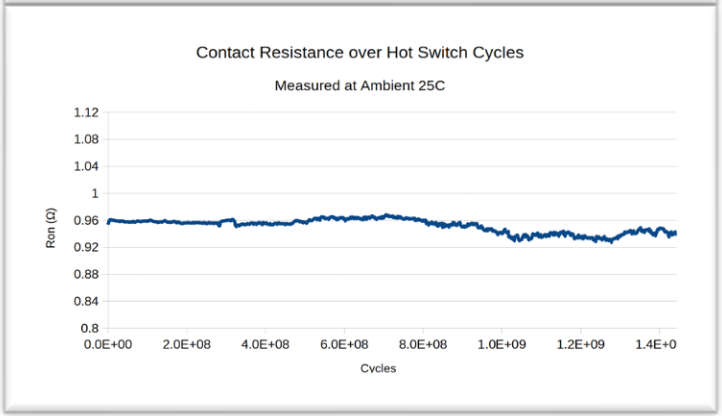


(b)

RF Hot Switch vs DC Hot Switch Test Performance



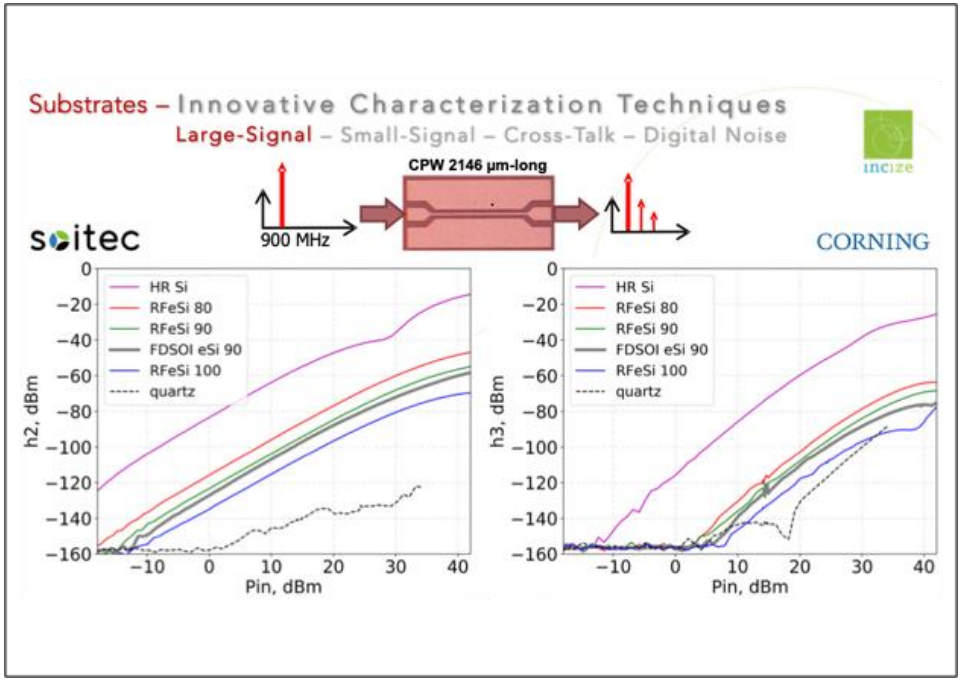


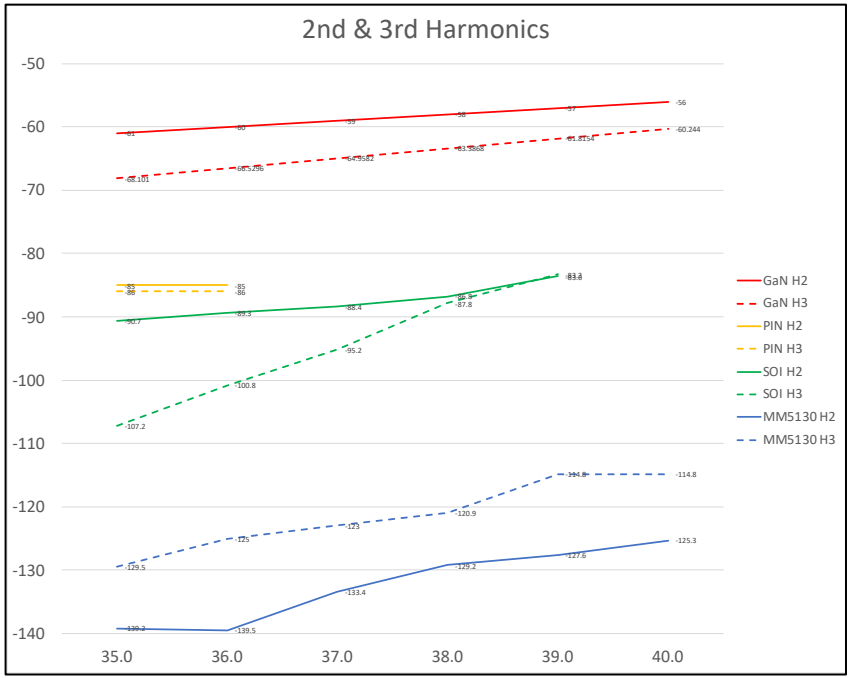


DC system run at 2.236V with 47Ω load

- Contact resistance remains stable during test
- Varied by <0.05Ω over test

Linearity





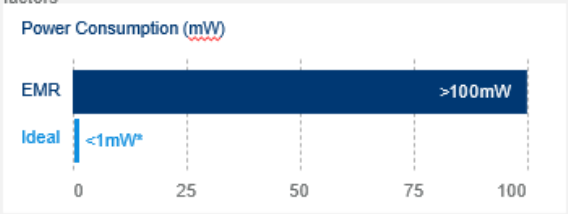
Moving from silicon to glass and removing the transistor from the RF signal chain helps reduce many sources of non-linearity.

Ideal Switch™ vs. Electromechanical Relay.

PERFORMANCE

100X LESS POWER

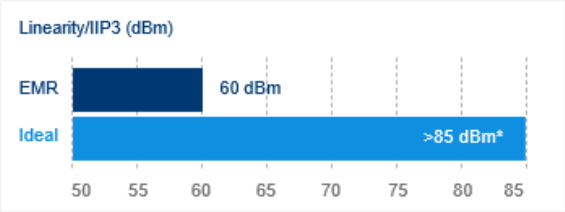
Longer battery life, less heat, new form factors



*Power needed to actuate a single switch

100X HIGHER LINEARITY

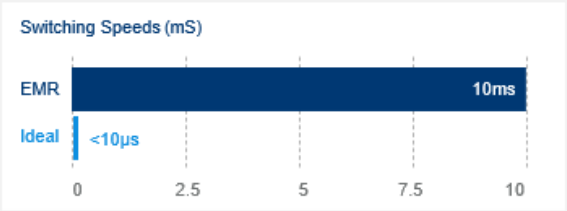
Distortion-free RF signal



*Menlo RF switch compared to typical RF coax switch performance.

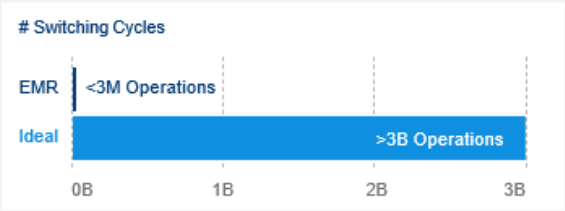
SWITCHES 1000X FASTER

New capabilities, New applications

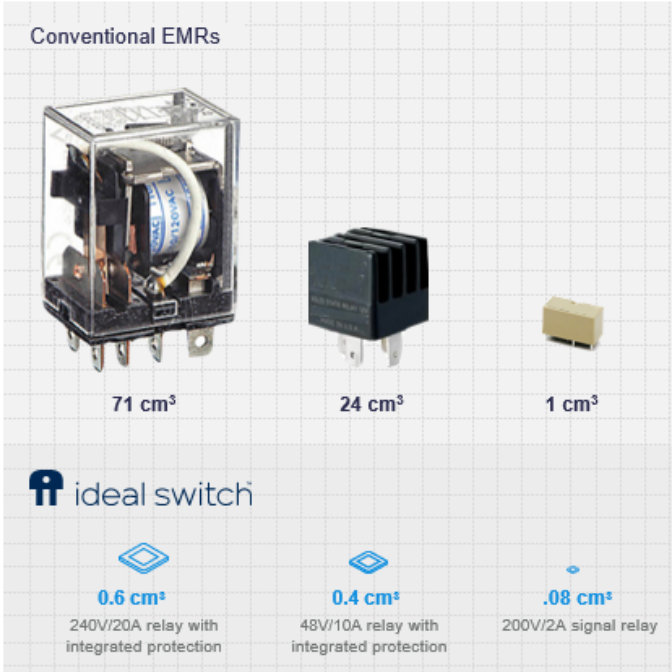


1000X LONGER LIFE

Massive reliability gain

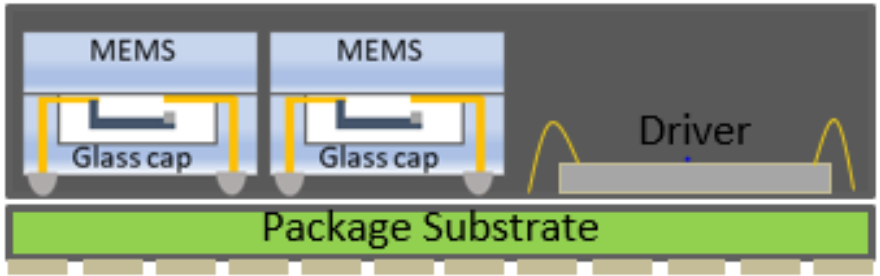


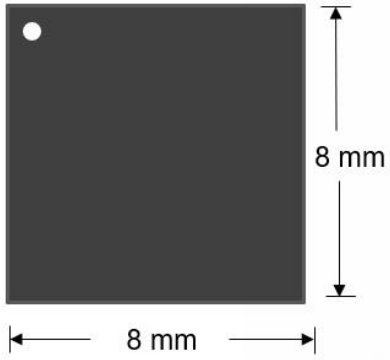
SIZE

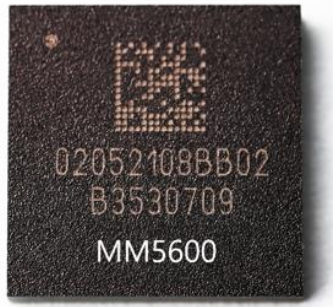


MM5600: High-Speed 40 Gbps DPDT Differential Switch

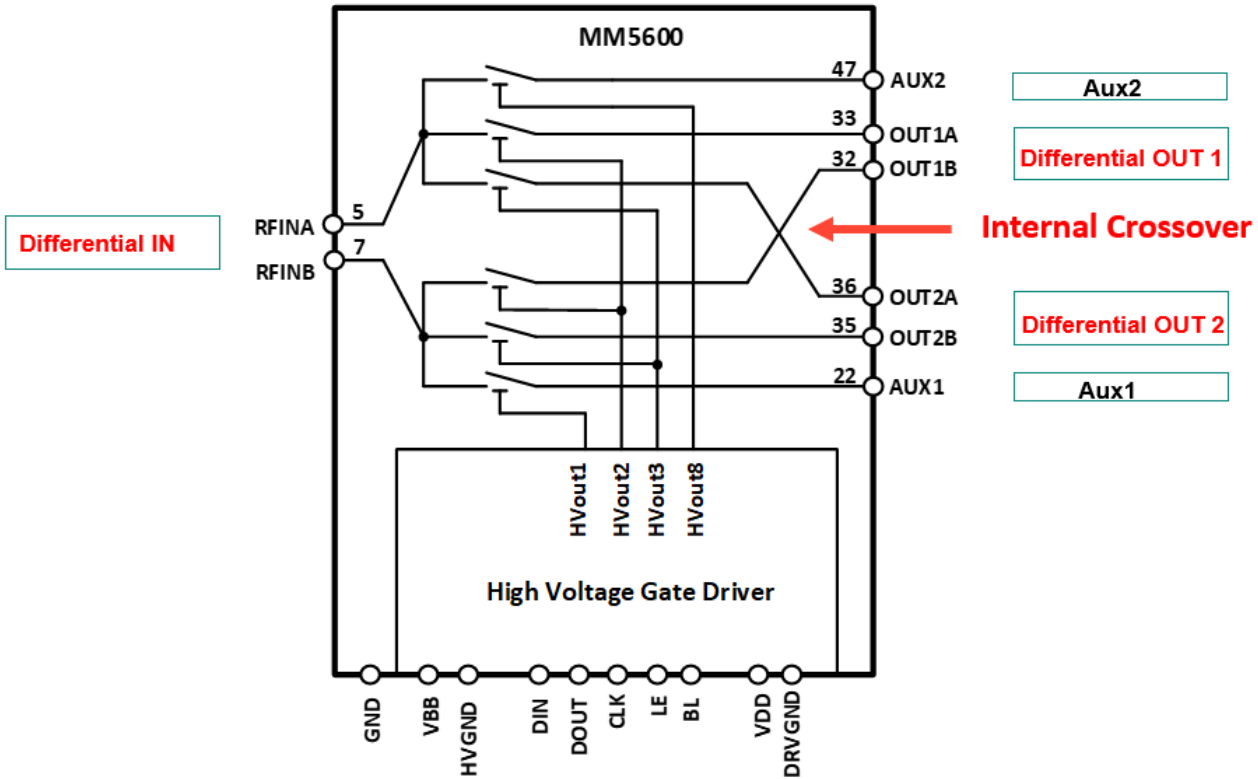
- Built on Menlo Micro's breakthrough Ideal Switch™ technology
- Targets "high-speed" differential signal devices up to 40
- Low insertion loss, fast switching speed, internal ESD diodes on all RF I/O pins
- Utilizes an internal high-voltage serial-to-parallel driver for control of the switch gate lines



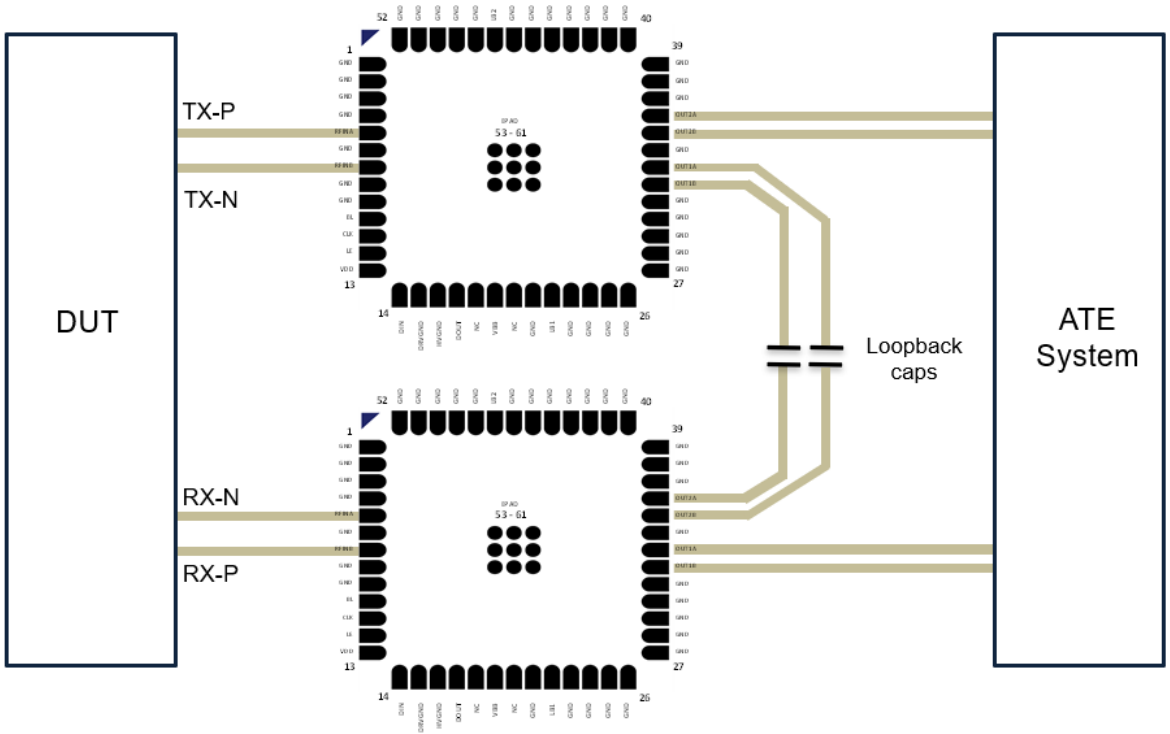




MM5600: DPDT Differential Switch – Block Diagram



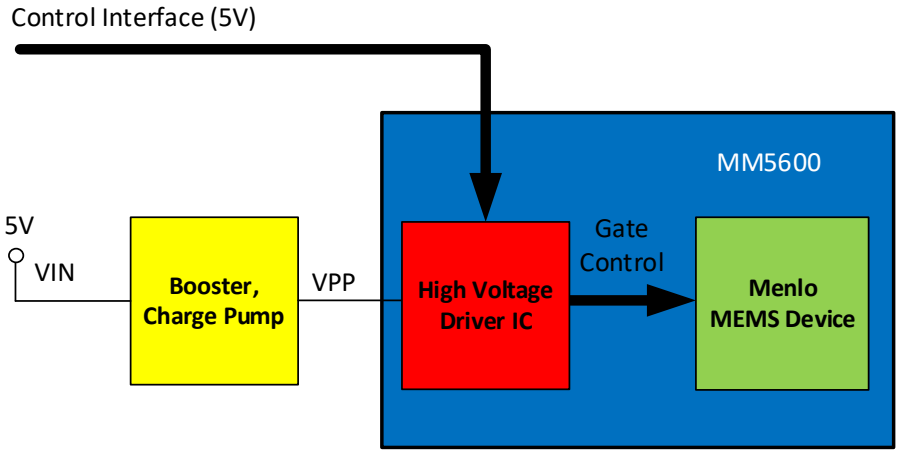
MM5600: Dual DPDT Configuration with Loopback

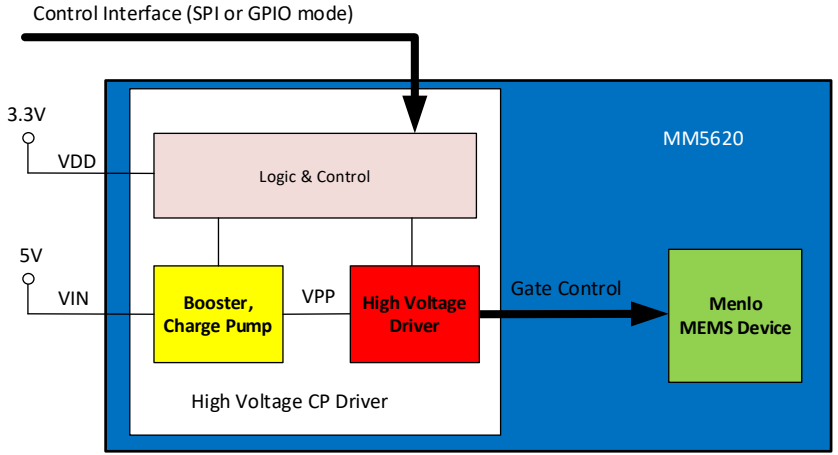


2 x MM5600 Menlo concept board for PCIe Gen 5 test

MM5600/MM5620 Switch Control

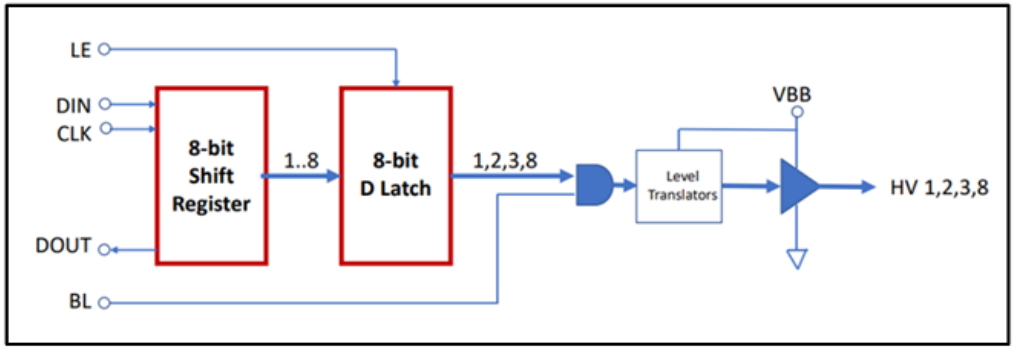
- The MEMS switches are activated via electrostatic force, and thus require a high voltage source for switching operation.
- The MM5600 device has a built-in high voltage driver, the upcoming MM5620 device even has a built-in charge pump.

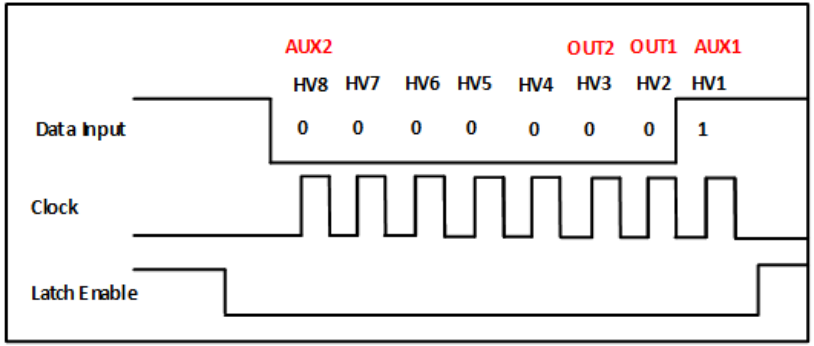




MM5600 High Voltage Gate Driver Control

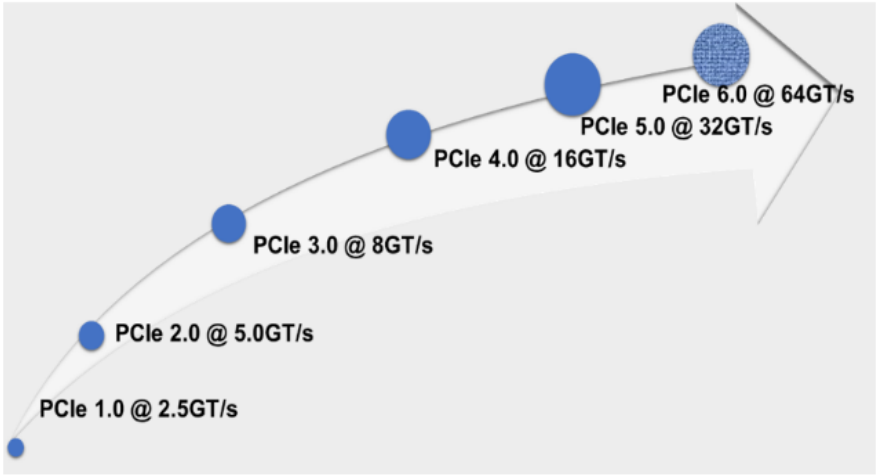
- The MM5600 uses only four of the eight data bits latched for switch control. Bits 1, 2, and 3 and 8 correspond to high voltage gate lines HV1, HV2, HV3, and HV8 respectively.
- BL (Blank input,pin 10) is always high.
- HV1 is “1” at the rising edge of the CLK, so RFINB(Pin7) will be connected to AUX1(Pin22) after the data is latched.





PCI Express

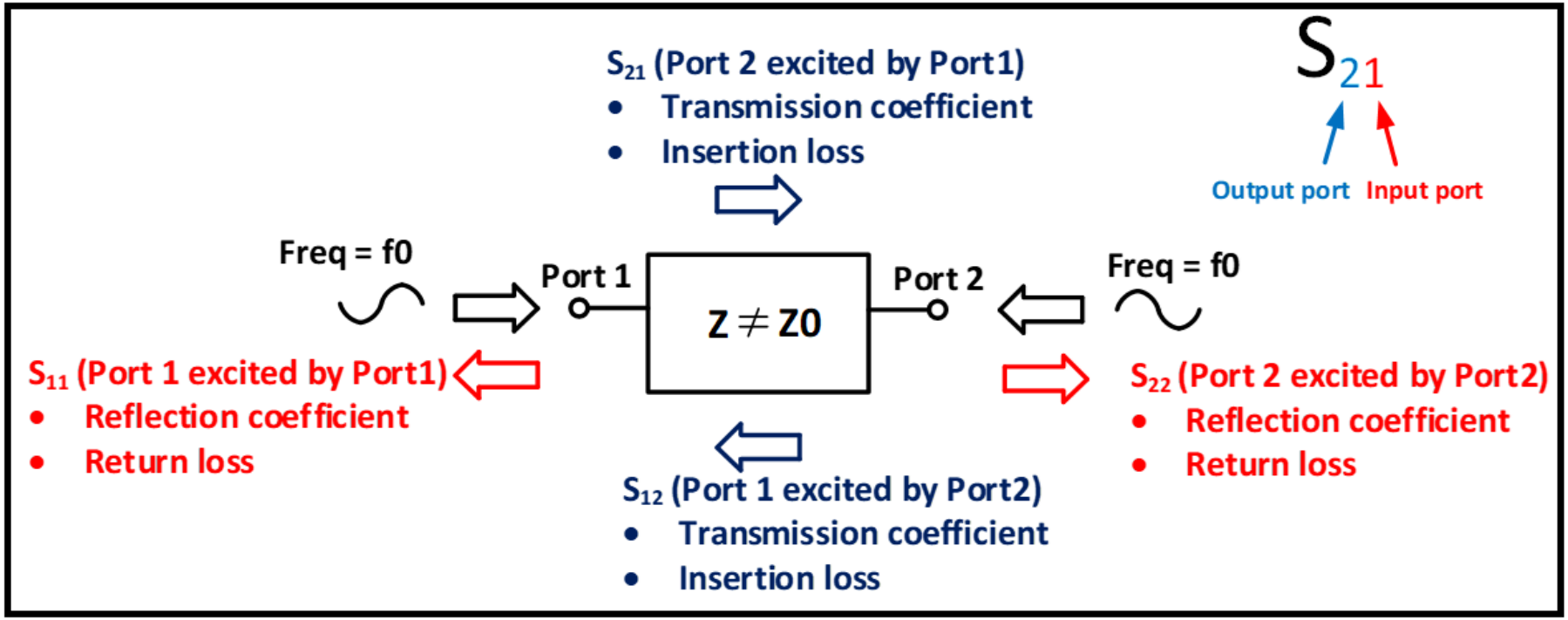
- PCIe 5.0 is twice as fast as PCIe 4.0, PCIe 5.0 has a 32 Gbps data rate, compared to 16 Gbps with PCIe 4.0.



PCIe Specification	Data Rate(Gb/s) (Encoding)	x16 B/W per dirn*	Year
1.0	2.5 (8b/10b)	32 Gb/s	2003
2.0	5.0 (8b/10b)	64 Gb/s	2007
3.0	8.0 (128b/130b)	126 Gb/s	2010
4.0	16.0 (128b/130b)	252 Gb/s	2017
5.0	32.0 (128b/130b)	504 Gb/s	2019
6.0	64.0 (PAM-4, Flit)	1024 Gb/s (~1Tb/s)	2021

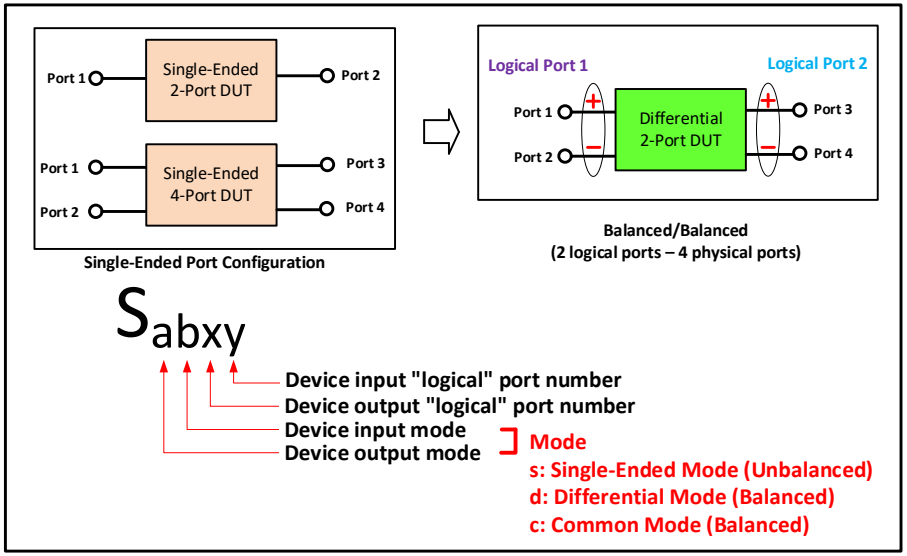
* - bandwidth after encoding overhead

An overview of 2-port S-parameters

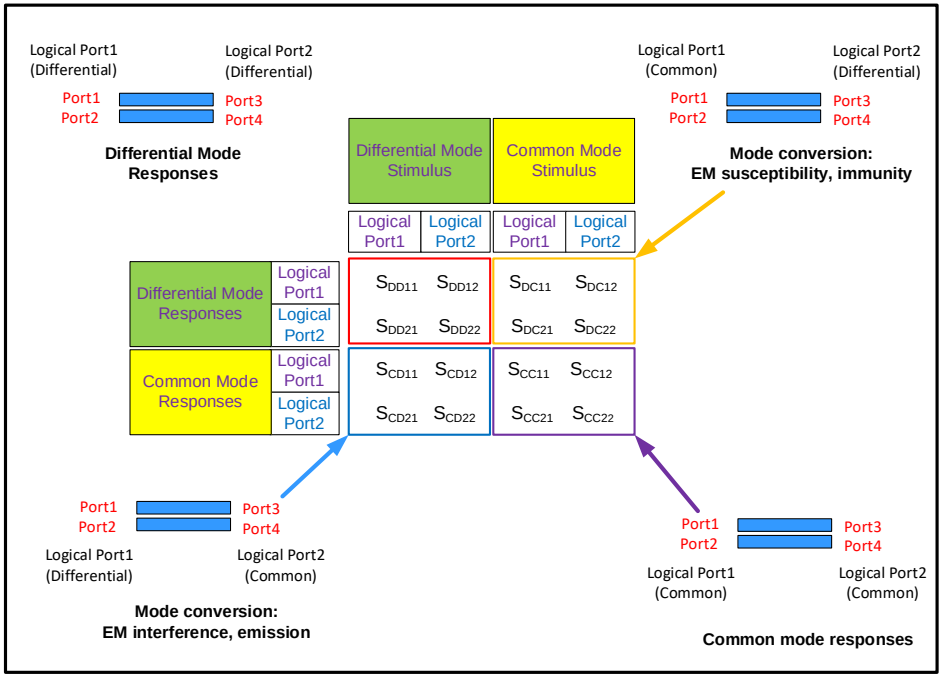


Simple 2-port S-parameters for a reciprocal passive device

Differential S-Parameter



Differential mode responses



4-port Differential S-parameters

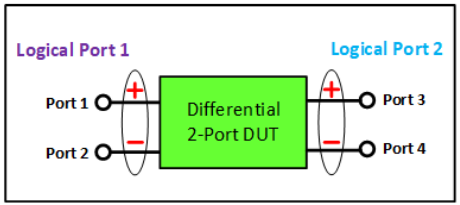
Signal Integrity Measurements using a VNA

- Time domain analysis is useful for measuring impedance values along a transmission line and for evaluating a device problem (discontinuity) in time or distance.
- For accurate TDR measurements, the analyzer should be calibrated. The measurement start and step frequencies should be equal. This is necessary for TDR measurements.
- For a Balanced input/Balanced output topology, this means that FOUR Thru connections should be made.
  - For example:

    Balanced Port 1 is ports 1 and 2

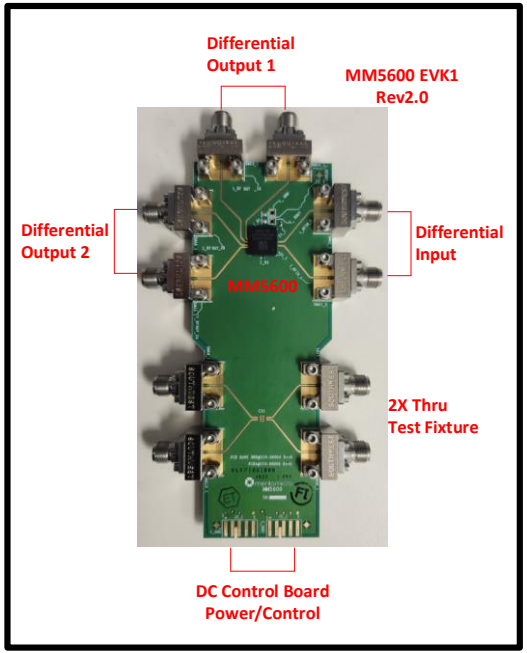
    Balanced Port 2 is ports 3 and 4

    Thru paths to be calibrated should be: Ports1-3, 1-4, 2-3, and 2-4.

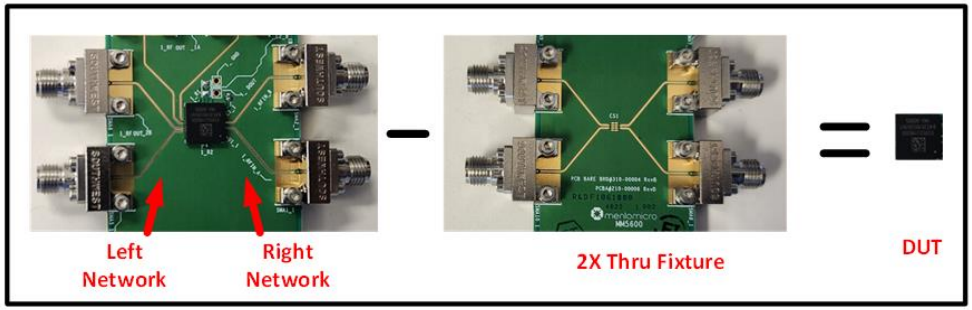


Balanced/Balanced
(2 logical ports – 4 physical ports)

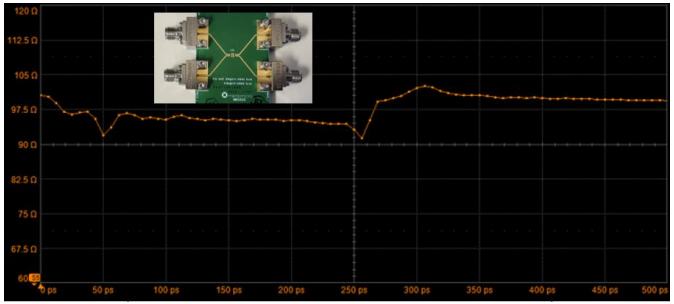
De-embedding Technique: 2x-thru De-embedding



MM5600 EVK1 Rev2.0

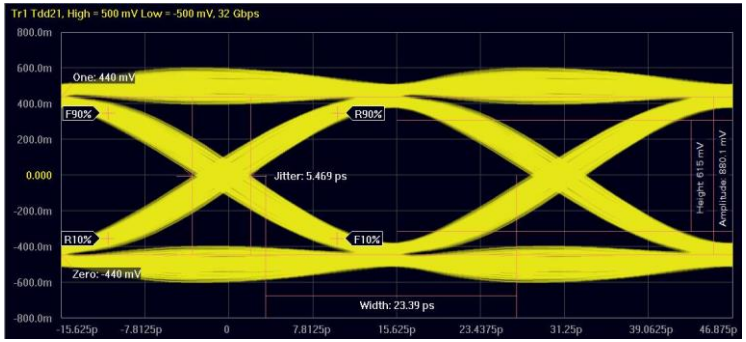


2x-thru de-embedding

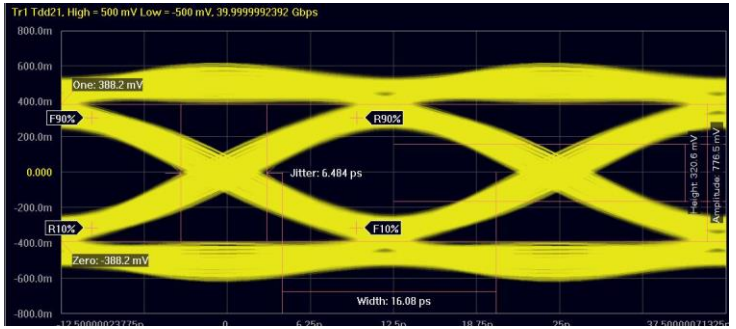


TDR measurement

MM5600– Signal Integrity Measurements



32 Gbps Eye Diagram Performance



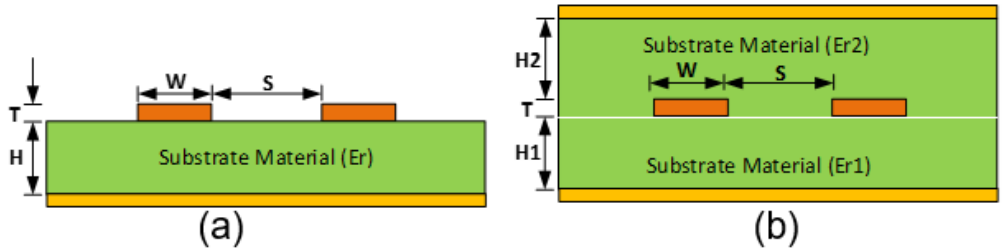
40 Gbps Eye Diagram Performance

Test conditions for measurements above are:

- 2^{15}-1 PRBS signal
- PRBS output is 1000mVp-p NRZ at RF connectors
- RF connector and RF traces are de-embedded
- Measured differentially on the MM5600 EVK board

High-Speed Digital PCB Design

- Very important to get deep understanding of fabrication houses' capability and details of their design rules in advance, then work very closely together with them.



Edge-coupled microstrip Edge-coupled stripline

- Important to choose better dielectric material with low dielectric constant, low-loss tangent, better surface roughness, Reverse Treated Copper Foil, and better PCB finish (plating method) such as EPIG, ISIG, EPAG, etc. if the design has high-speed routing on top/bottom layer.

High-Speed Digital PCB Design

- Two MM5600 devices need to be placed as close as possible to each other.
- To optimize transmission line design, wider and shorter traces are better to minimize the insertion loss.
- For the differential signals, routing should be smooth with minimum bends and tight length matching is required.
- To provide a proper de-embedding, the 2x-through needs to be implemented with symmetrical routing and placement.
- Stitching vias are required to be placed along all the high-speed routing from DUT to Connectors. If space allows, it is ideal to implement two rows of stitching vias along the RF signals routing.

High-Speed Digital PCB Design

- Optimizing via transitions is necessary to minimize the impedance mismatch. A TDR simulation using 3D EM tools is a good method to check the impedance of vias and optimize it.
- Soldermask needs to be removed on high-speed traces.
- Although it takes additional time, confirmation by running post-layout full 3D EM simulation, to obtain s-parameter, TDR, and eye diagram results, is a must to ensure that the board layout can meet the requirements.

Selecting an RF Connector

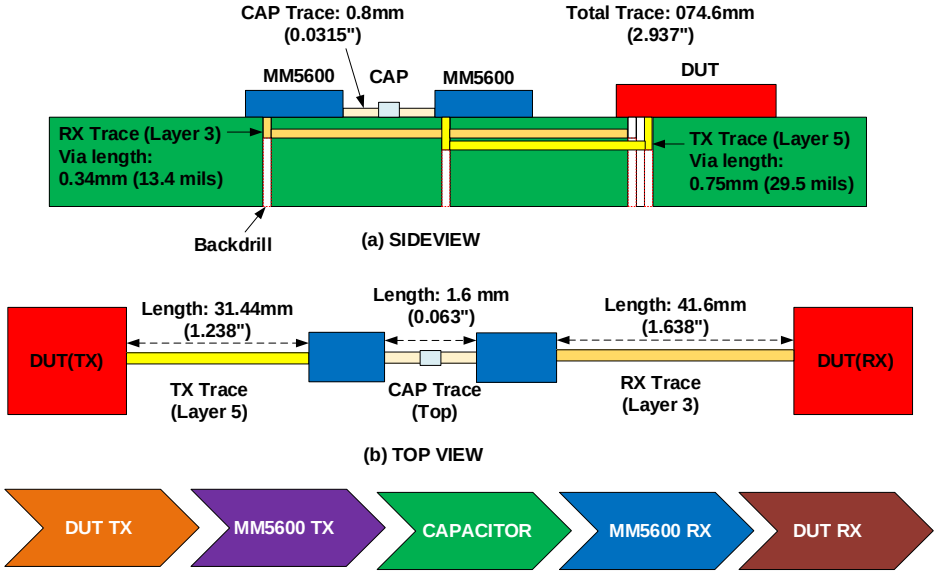
- The Nyquist frequency is 16GHz for both PCIe Gen5 and Gen6; for digital signal, need to use at least K connector (2.92mm, up to 40GHz) or V connector (1.85mm, up to 67GHz).
- For high-speed, high performance RF board, it is recommended to use a solderless PCB connector.
- For the edge launch connector, copper underneath of the connector should be flushed with the board edge, otherwise the signal will lose reference and will get an inductive spike from that area which will affect performance.

Edge Launch Connector

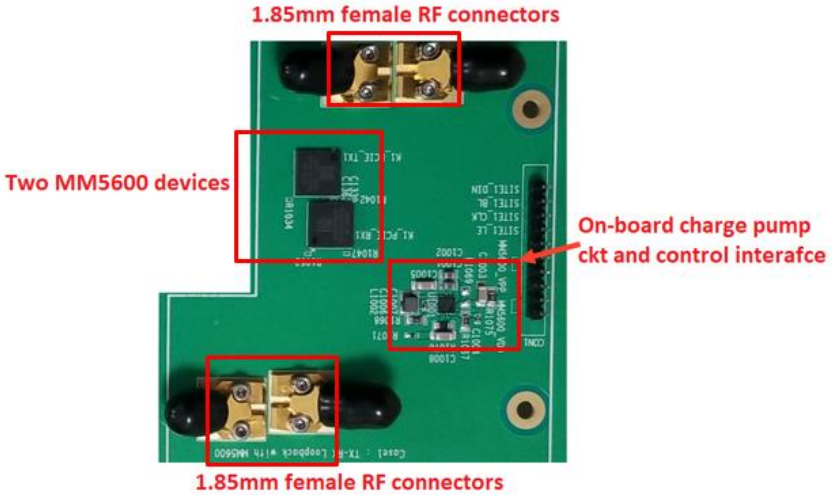
Solderless PCB connectors – 45 degree

MM5600 Loopback Circuit with Evaluation Board

- A test coupon board to evaluate the high-speed loopback circuit to make sure the load board design can meet the PCIe Gen5.0 requirements.



Load Board Structure



MM5600 Loopback Test Board

MM5600 Loopback board design with two different topologies

•A test coupon board to evaluate the high-speed loopback circuit to make sure the load board design can meet the PCIe Gen5.0 requirements.

CASE1

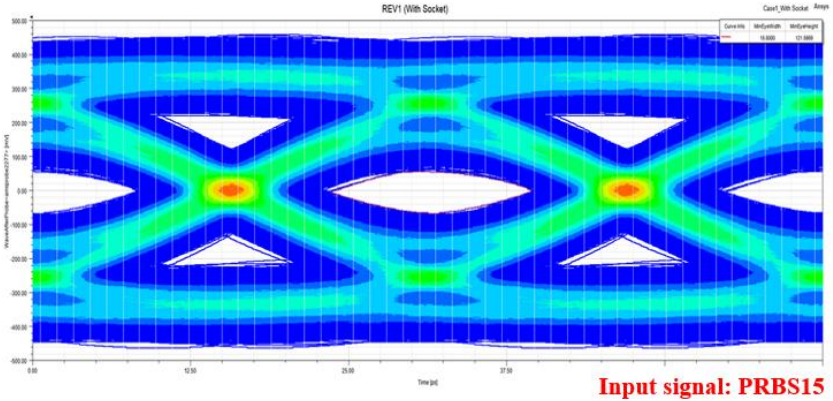
CASE2

CASE	TOPOLOGY	DETAIL
1	TX-RX Loopback with MM5600	MM5600 mounted and full path case.
2	TX-RX Loopback without MM5600 (Connected to Trace)	MM5600 is not mounted, and the internal circuit of MM5600 is mounted as a trace

Eye-Diagram Performance of the Evaluation Board – Case 1

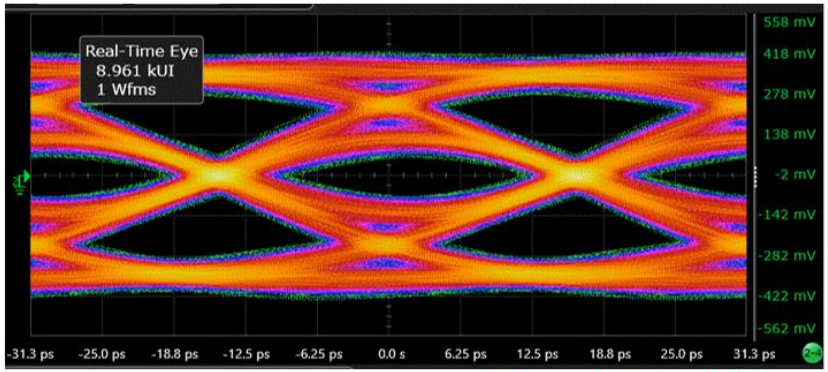
- A test coupon board to evaluate the high-speed loopback circuit to make sure the load board design can meet the PCIe Gen5.0 requirements.

Simulation Result
(Included Socket Touchstone File)



Input signal: PRBS15

Measurement Result
(De-embedded 50cm Cable of OSC Side)

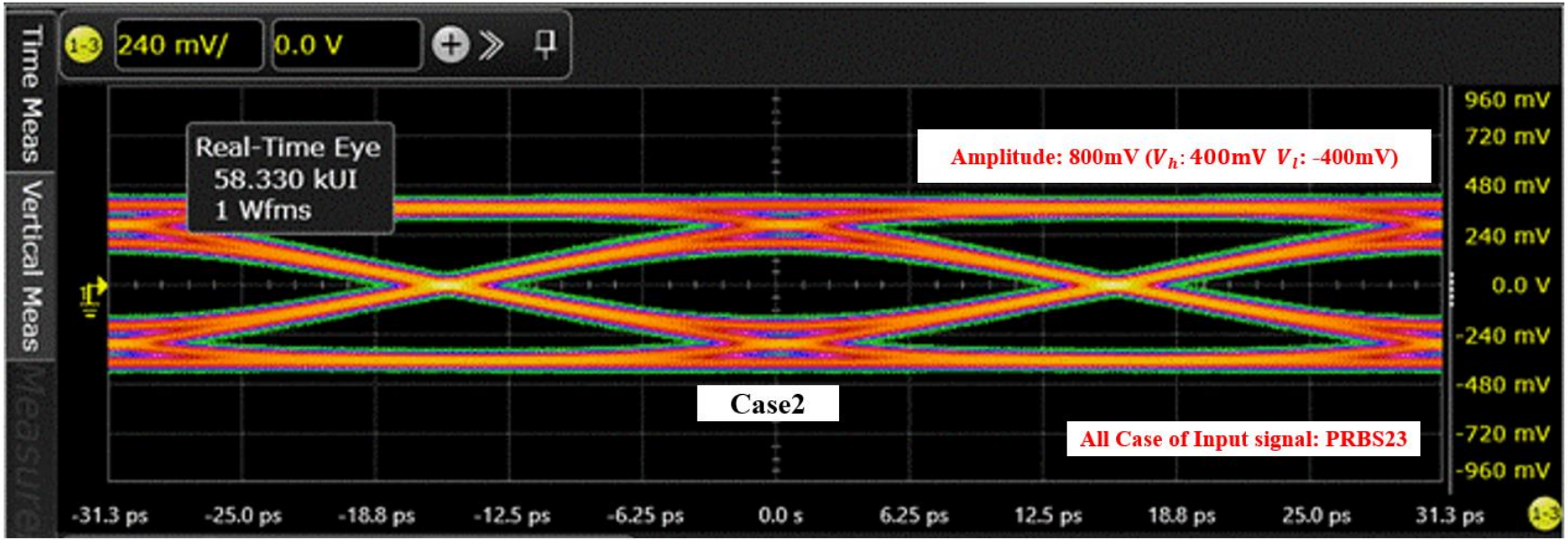


All Case of Input signal: PRBS23

Amplitude: 800mV (V_h: 400mV V_l: -400mV)

Reference Result (Measurement)		Simulation Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	15.5ps	121.0mV	20.21ps (76%)	108.0mV (22%)

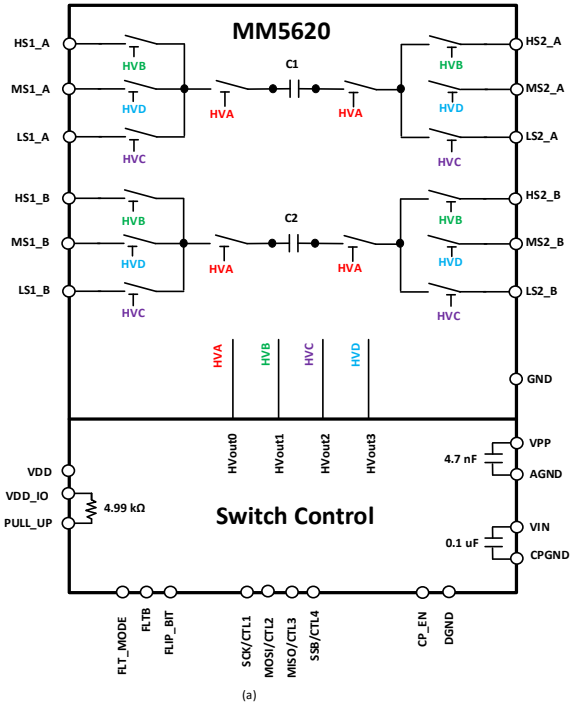
Eye-Diagram Performance of the Evaluation Board – Case 2



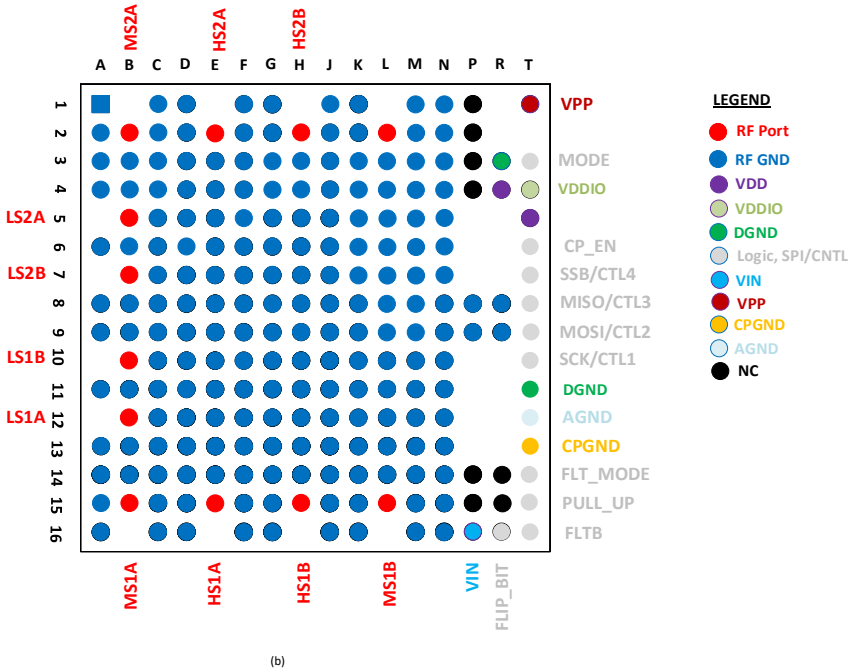
Reference Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	25.00ps (95%)	270.0mV (53%)

32Gbps Loopback without MM5600 (Connected to Trace), Measured result, NRZ, 800mVpp, PRBS 2^{23}-1

PCIe Gen6 - External Loopback using the MM5620 Device

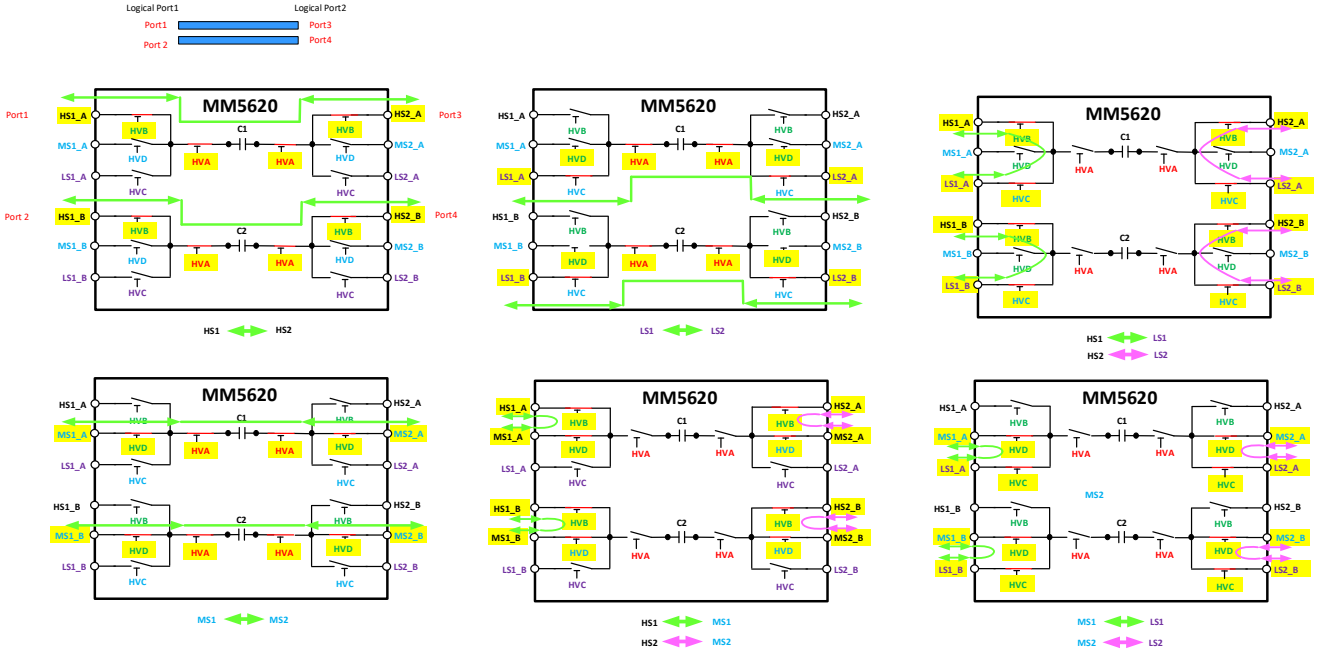


MM5620 Functional Block Diagram



MM5620 (8.2mm x 8.2 mm LGA) Top View

MM5620 - Six Possible Signal Paths

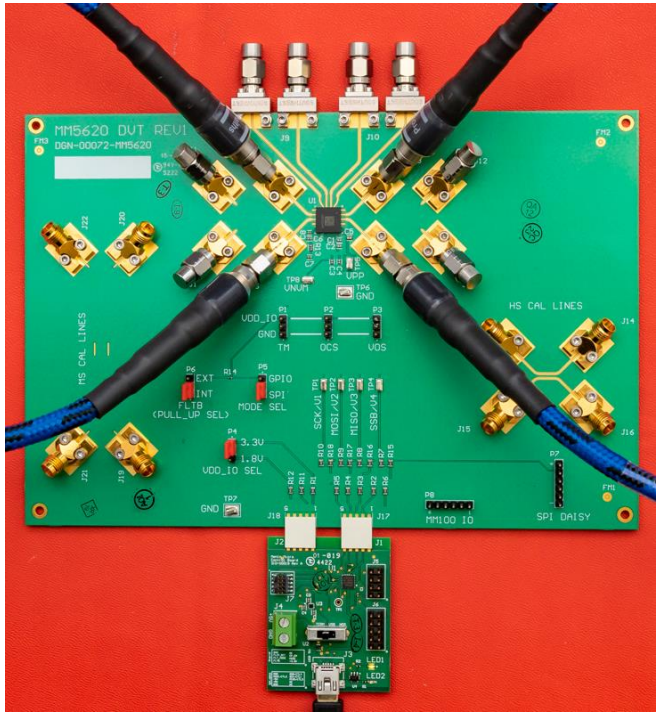


MM5620 Signal Paths

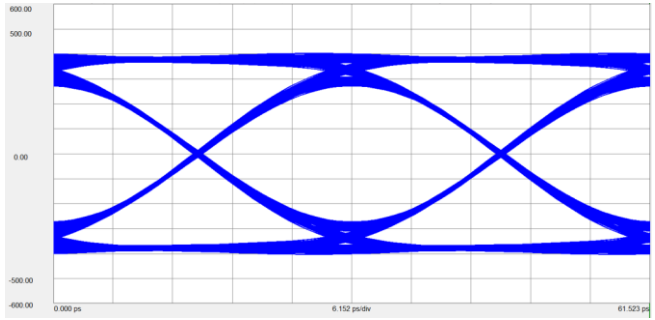
Input (Output)	Output (Input)	HVA	HVB	HVC	HVD
HS1	HS2	HIGH	HIGH	LOW	LOW
HS1	MS1	LOW	HIGH	LOW	HIGH
HS1	LS1	LOW	HIGH	HIGH	LOW
MS2	HS2	LOW	HIGH	LOW	HIGH
MS2	LS2	LOW	LOW	HIGH	HIGH
MS1	MS2	HIGH	LOW	LOW	HIGH
LS2	HS2	LOW	HIGH	HIGH	LOW
LS1	MS1	LOW	LOW	HIGH	HIGH
LS1	LS2	HIGH	LOW	HIGH	LOW

MM5620 Truth Table

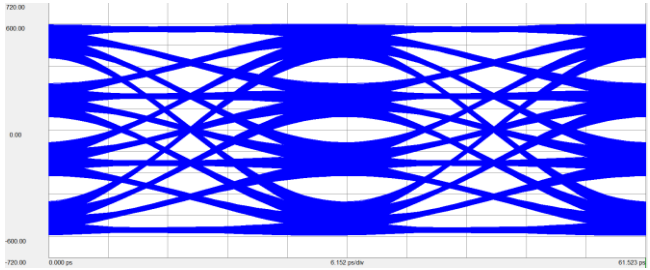
MM5620 Eye-Diagram Performance – High Speed Loopback Path



MM5620 evaluation board



PCIe Gen5: +/-400mV, NRZ, 32 GBps, PRBS 2^{15}-1



PCIe Gen6 – 32GBaud (64GBps), PAM4, PRBS 2^{15}-1

Summary and Conclusion

- The MM5600 device, Menlo's first differential DPDT switch available in production quantities, is introduced. This device can support PCIe Gen5.0 loopback test and can be used for PCIe Gen4.0 applications for improved performance and reliability by replacing EMR relays on the existing load boards
- We have presented simulated and measured eye-diagram performance of the PCIe Gen 5.0 loopback board utilizing two MM5600 devices to ensure that the load board design can meet the PCIe Gen5.0 requirements.
  - An excellent eye-diagram performance is achieved at 32Gbps signal with an eye height of 108mV without pre-emphasis or equalization enabled, and both RF connectors and transmission lines are not de-embedded.

Summary and Conclusion

- The MM5620 device, differential dual DP3T switch, is introduced; it can support PCIe Gen6.0 loopback test.
  - An excellent eye-diagram performance is achieved at 32GBaud signal with an eye height of 154 mV, both RF connectors and transmission lines are de-embedded.
- Test engineers requiring an RF switch that meets the requirements for PCIe 4.0/5.0/6.0 performance while saving crucial space in the load board and improving reliability, will appreciate a MEMS-based approach solution that is also cost competitive to EM and solid-state solutions.

High-Speed Loopback Applications by Utilizing a Differential DPDT MEMS Switch

MORE INFORMATION

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Thank you for attending !

QUESTIONS?

Thank you for attending this webinar!

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