Fully Integrated Ideal Switch Solution Meets PCIe 6.0 Requirements with HSIO Loopback

The Ideal Switch

Enabling the electrification of everything

Milliwatts-to-kilowatts, DC-to-light

April 2023

POWERED BY ideal switch™

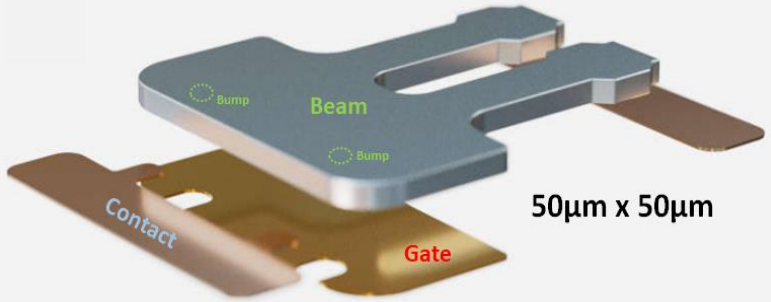
menlomicro

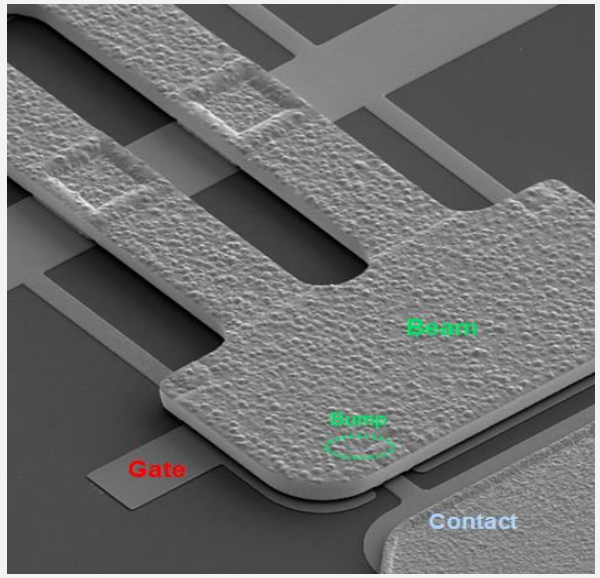
Agenda:

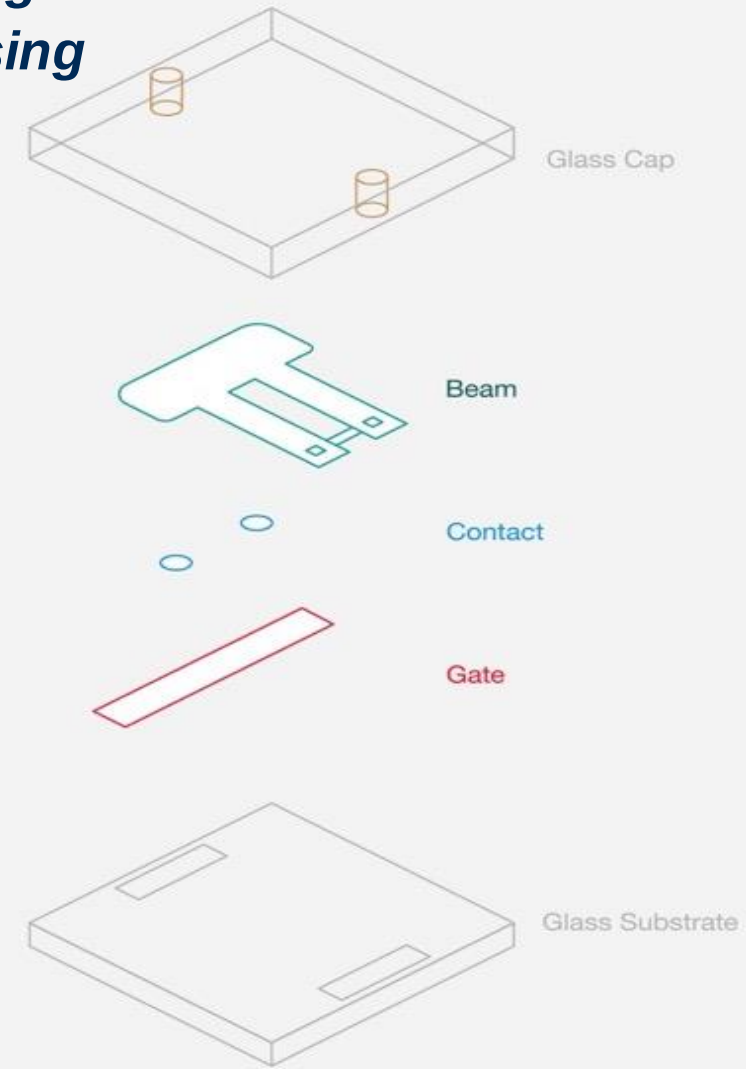
- Introduction of an RF MEMS Switch
- S-Parameter Overview
- De-embedding Technique: 2x-thru De-embedding
- Target Markets & Applications
- PCI Express Link Speed
- MM5620 – Product Introduction
- MM5620 – Measured S-Parameter Performance
- MM5620 – Control Block Diagram and External Circuits
- MM5620 – High-Speed Loopback Path Performance
- MM5620 – Double Density HSIO Loopback Mode Test
- MM5620 – Customer Evaluation Board

Introducing the Ideal Switch™

Technology platform with breakthrough innovations in materials and processing







Unique Glass Packaging

Improved RF & thermal performances
High RF power handling

Through-Glass-Via

Low parasitic and resistance
Small-size package

High Reliability

>3B switching cycles
Hermetic-sealed package

Scalability

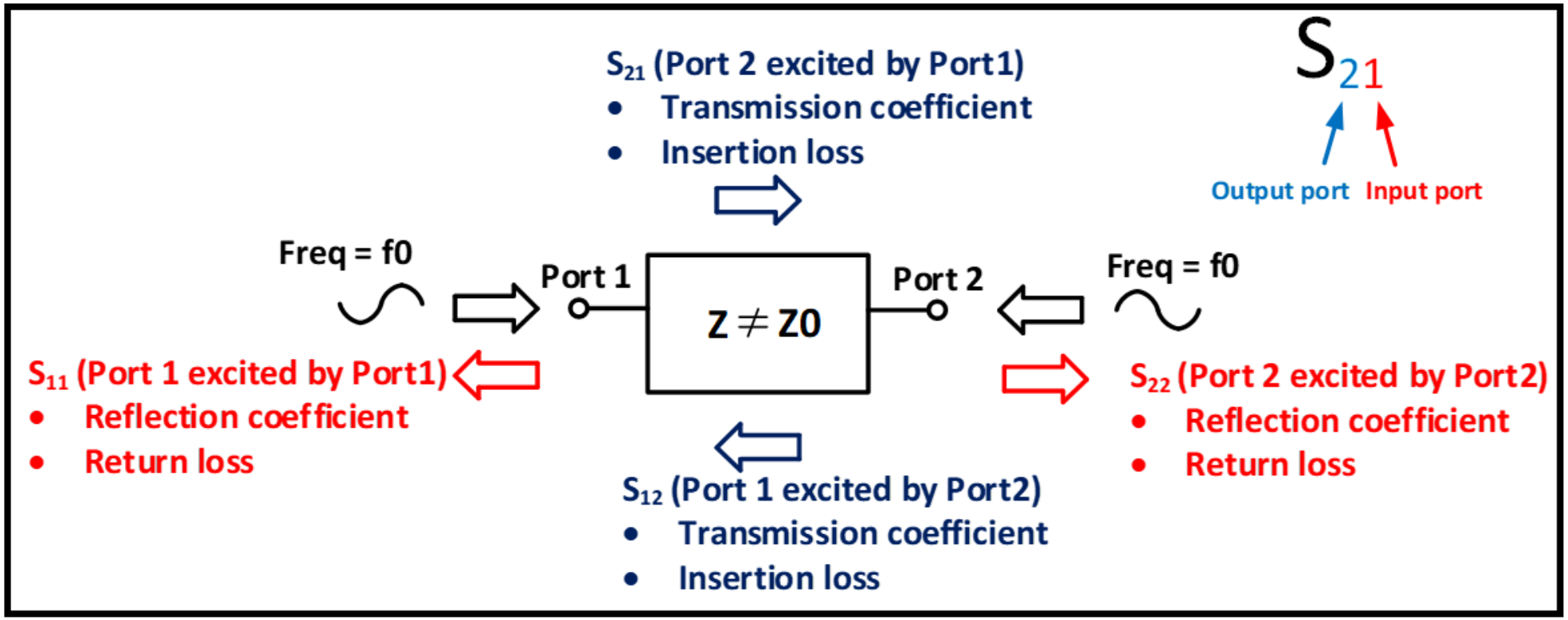
50µm x 50µm (unit cell)

Scalable switch arrays for high voltage, high current, high power

[Ideal Switch Technology - How It Works | Menlo Micro]

Two-Port S-parameters

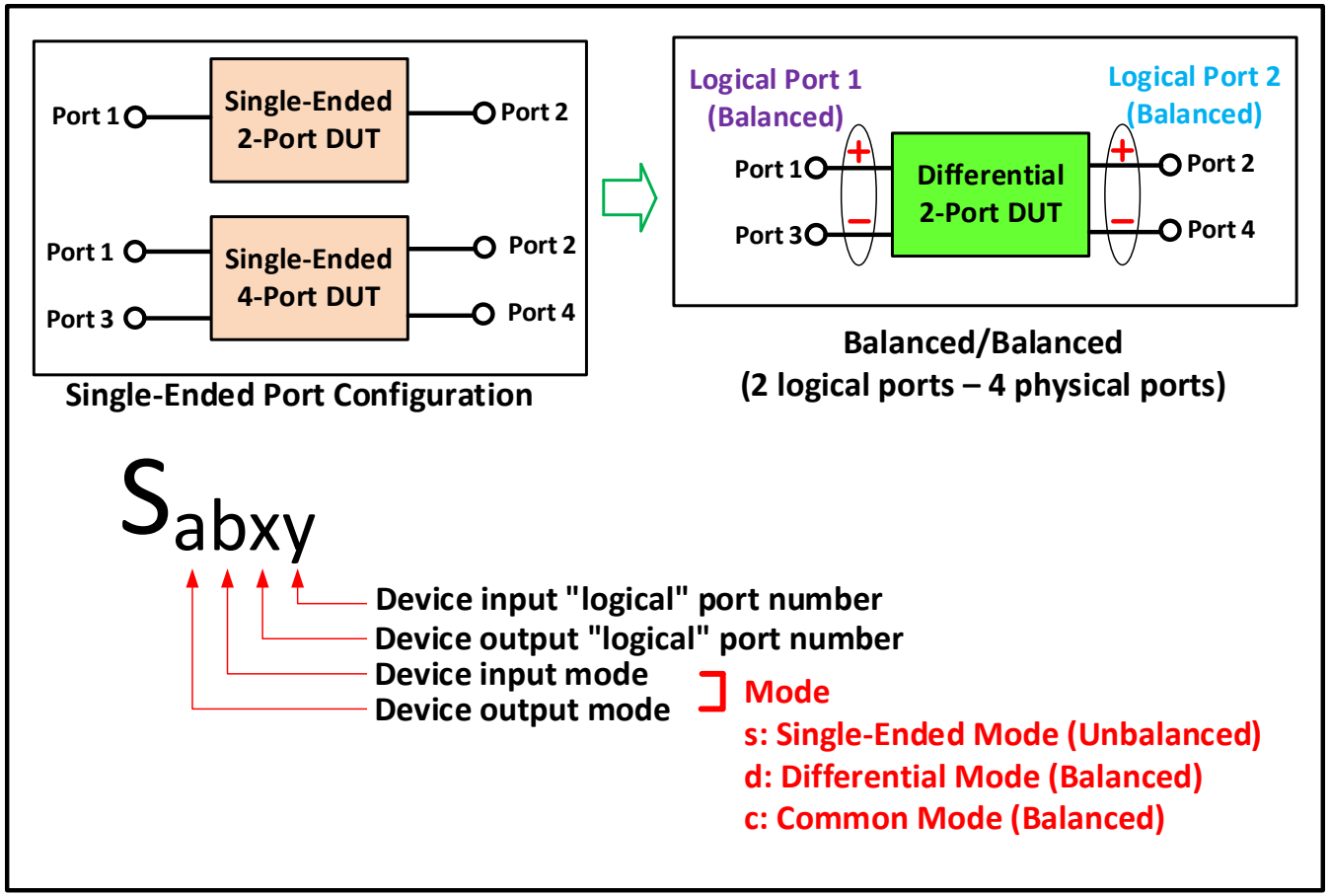
- S-parameters are complex matrices that show reflection and transmission characteristics (amplitude and phase) in the frequency domain



2-Port S-parameters

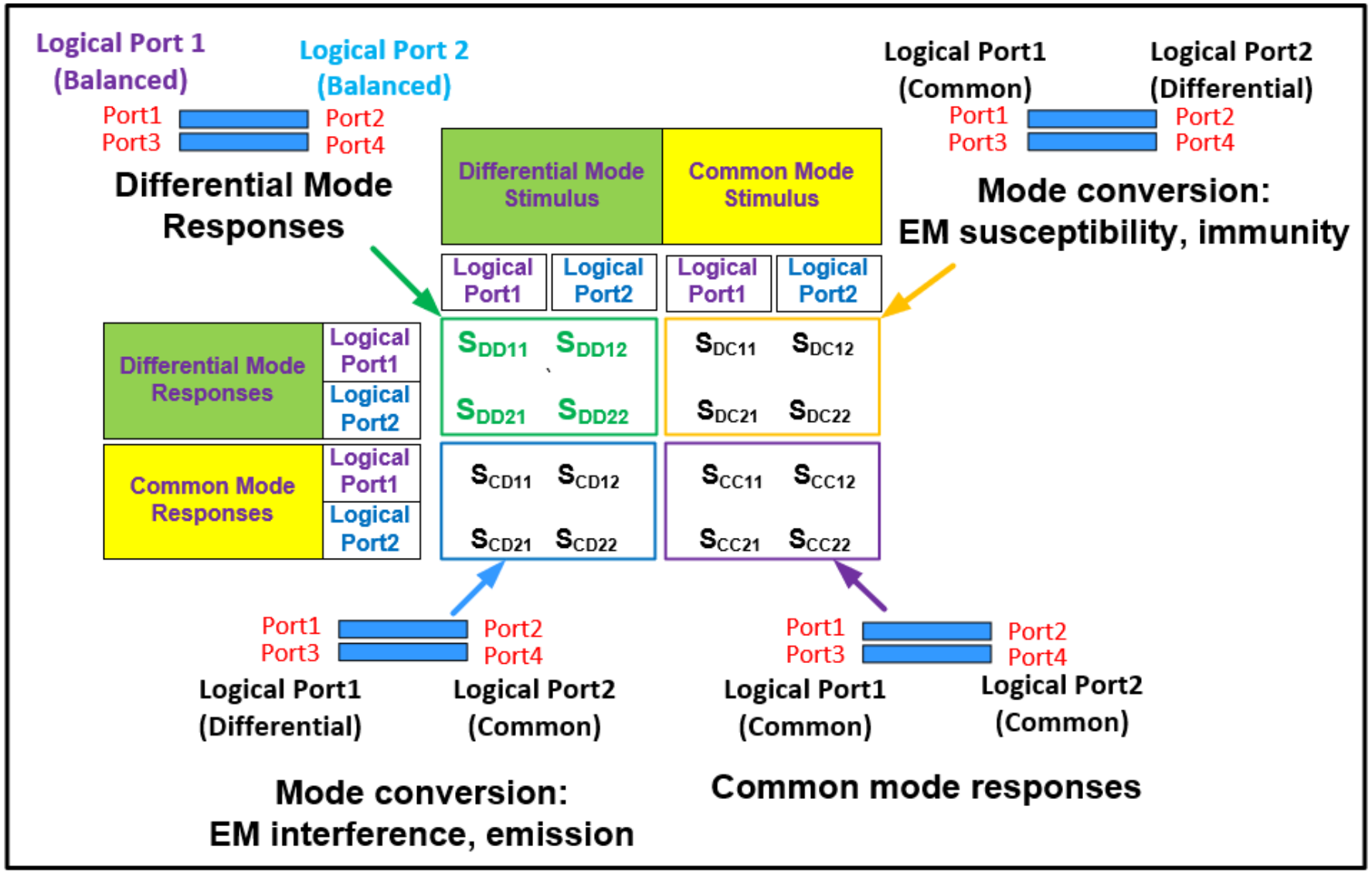
Differential S-Parameters

- Differential mode responses can be obtained by balanced measurements and are represented by differential S-parameters



Differential mode responses

4-Port Differential S-Parameters



4-Port Differential S-parameters

Touchstone File Format

- The Touchstone file contains frequency values and S-parameters

Frequency units are Hz

S-Parameters

dB and Degrees

Reference Impedance 50 Ohm

.s1p: 1-Port S-Parameter File
.s2p : 2-Port S-Parameter File
.s4p : 4-Port S-parameter File

```
!S4P File: Measurements: <Sdd11,Sdc11,Sdd12,Sdc12>,
!<Scd11,Scc11,Scd12,Scc12>,
!<Sdd21,Sdc21,Sdd22,Sdc22>,
!<Scd21,Scc21,Scd22,Scc22>:
# Hz S  dB   R 50
10000000 -46.887413 162.24268 -46.695118 -33.026134 -0.068148375 -1.0384876 -46.298244 11.523661
-46.692268 -35.953835 -46.716522 160.54953 -46.435684 14.344072 -0.066351458 -1.0450206
-0.050488863 -0.99340469 -45.303799 -10.566242 -47.015465 -141.53207 -48.130299 19.855814
-45.068867 -7.7613277 -0.055597607 -0.9842146 -47.557877 21.219717 -46.607079 -137.76706
20000000 -44.2533 106.29446 -47.321148 -59.671833 -0.07096079 -1.7549706 -47.131927 1.5383472
-47.304211 -60.167545 -44.179386 105.96419 -47.186459 2.6364694 -0.070606634 -1.7535229
-0.050903711 -1.8230745 -45.709652 -13.290565 -51.274353 -131.08434 -47.738243 54.710979
-45.554943 -13.748737 -0.050477076 -1.8270626 -47.669868 55.314487 -51.231934 -132.05318
```

SDC12

SDC11

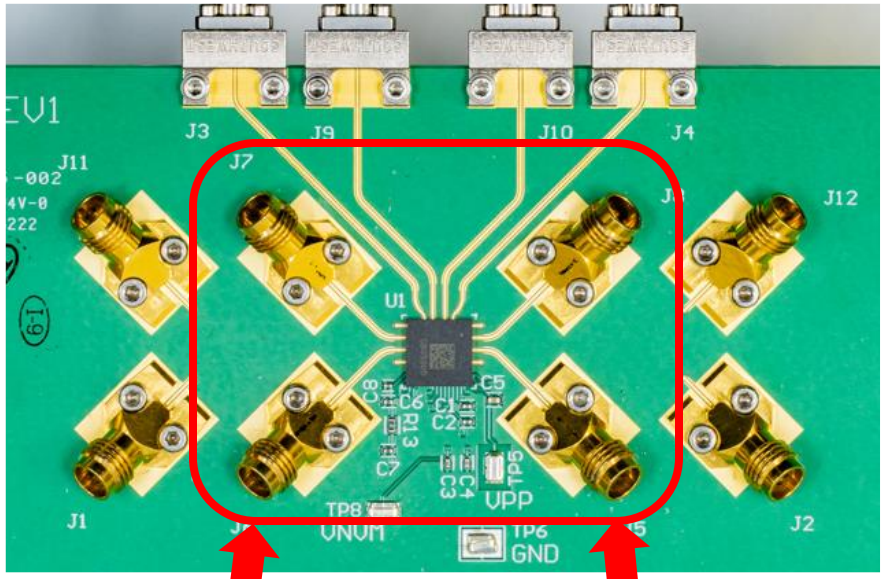
SDD12: -0.071 dB, -1.76 Degrees at 20MHz

SDD11: -44.3 dB, 106.3 Degrees at 20MHz

20,000,000 Hz → 20MHz

De-embedding Technique: 2x-thru De-embedding

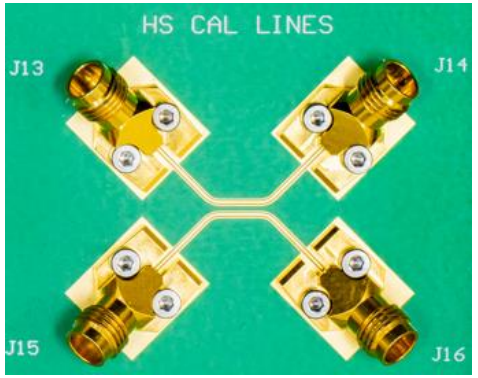
- As the device under test (DUT) is mounted on a board with input/output RF traces and connectors
- Need to de-embed the measured performance to obtain the true DUT performance



Left Network

Right Network

MM5620 Evaluation Board



2x-thru Fixture

DUT Only Performance

MM5620 – Target Markets & Applications

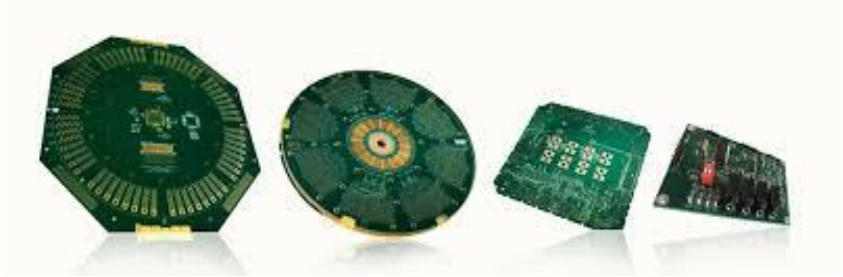
Target Markets

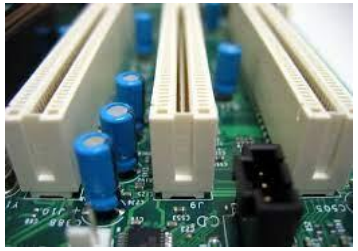
- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Test
- Compliance and loopback testing

Target Applications

- High-Speed Digital SoC Testing

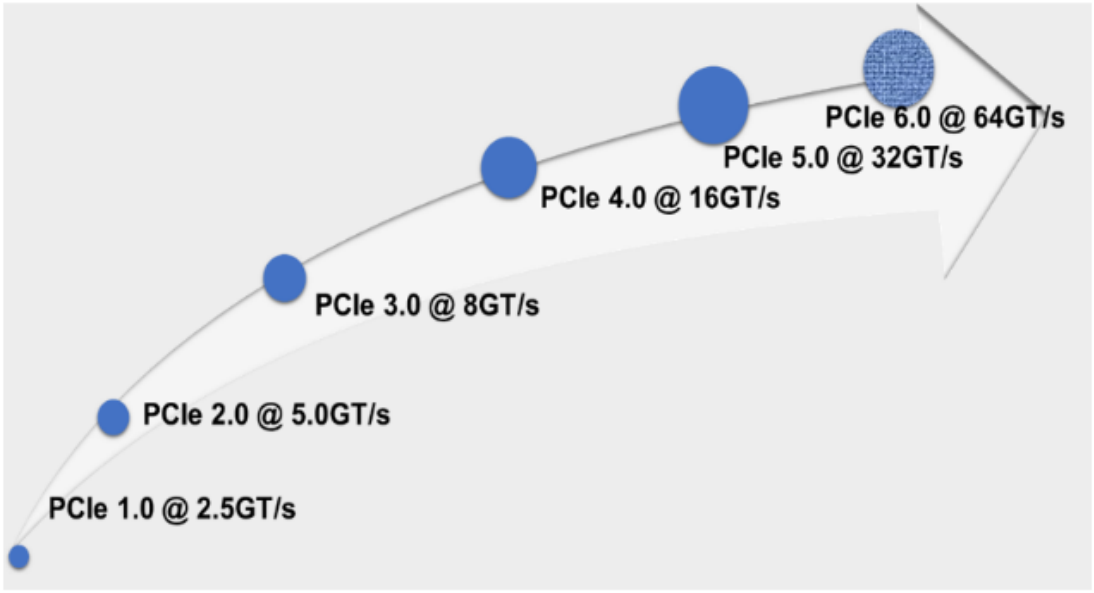
  PCIe Gen 5 & 6, SerDes, USBx.x, InfiniBand, HDMI…
- O/E module testing
- High Speed Signal Routing
- Differential Switch Matrices





PCI Express Link Speed

- PCIe 6.0 is twice as fast as PCIe 5.0, PCIe 6.0 has a 64 Gbps data rate, compared to 32 Gbps with PCIe 5.0.

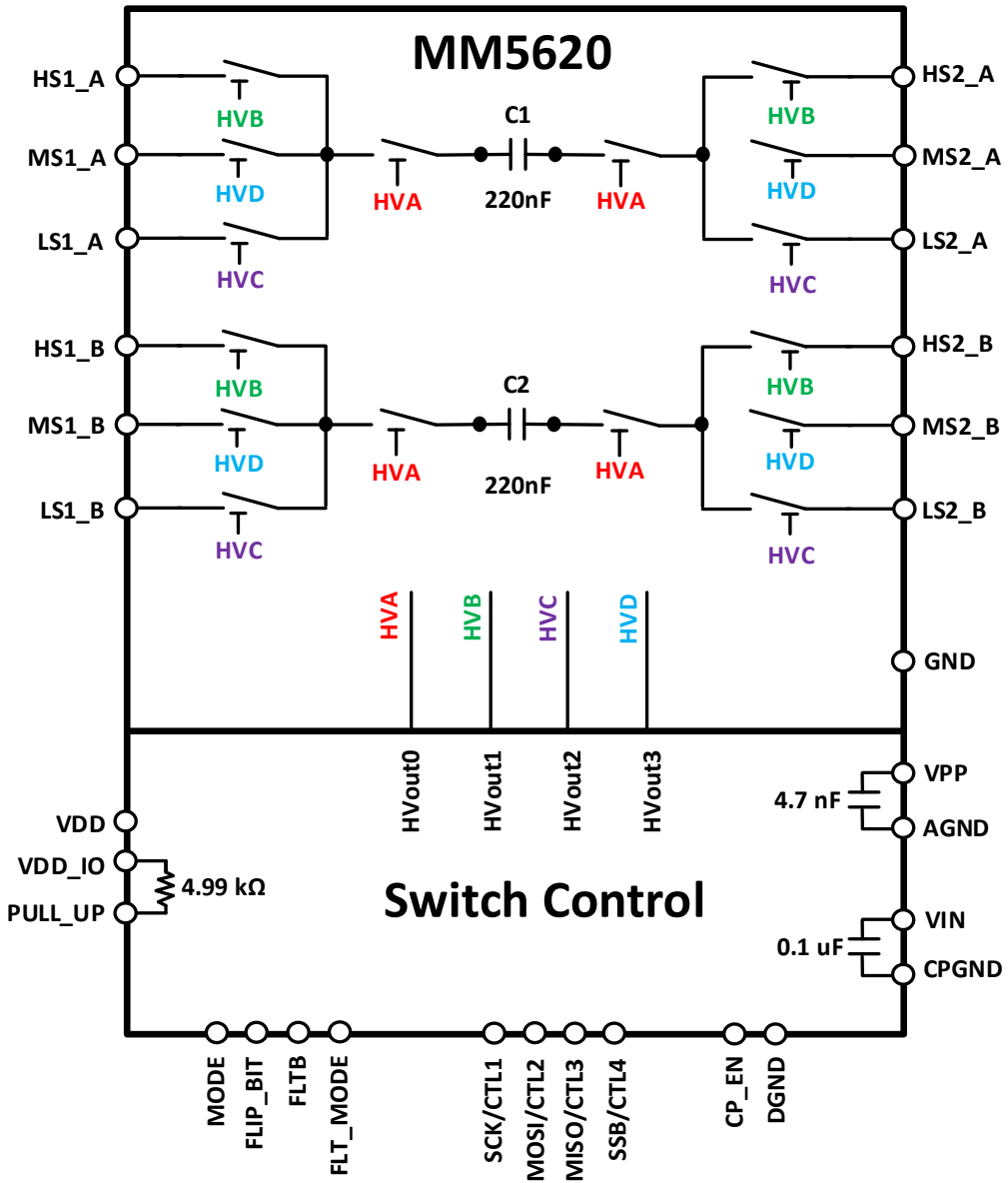


PCIe Specification	Data Rate(Gb/s) (Encoding)	x16 B/W per dirn*	Year
1.0	2.5 (8b/10b)	32 Gb/s	2003
2.0	5.0 (8b/10b)	64 Gb/s	2007
3.0	8.0 (128b/130b)	126 Gb/s	2010
4.0	16.0 (128b/130b)	252 Gb/s	2017
5.0	32.0 (128b/130b)	504 Gb/s	2019
6.0	64.0 (PAM-4, Flit)	1024 Gb/s (~1Tb/s)	2021

* - bandwidth after encoding overhead

MM5620 – Product Highlights

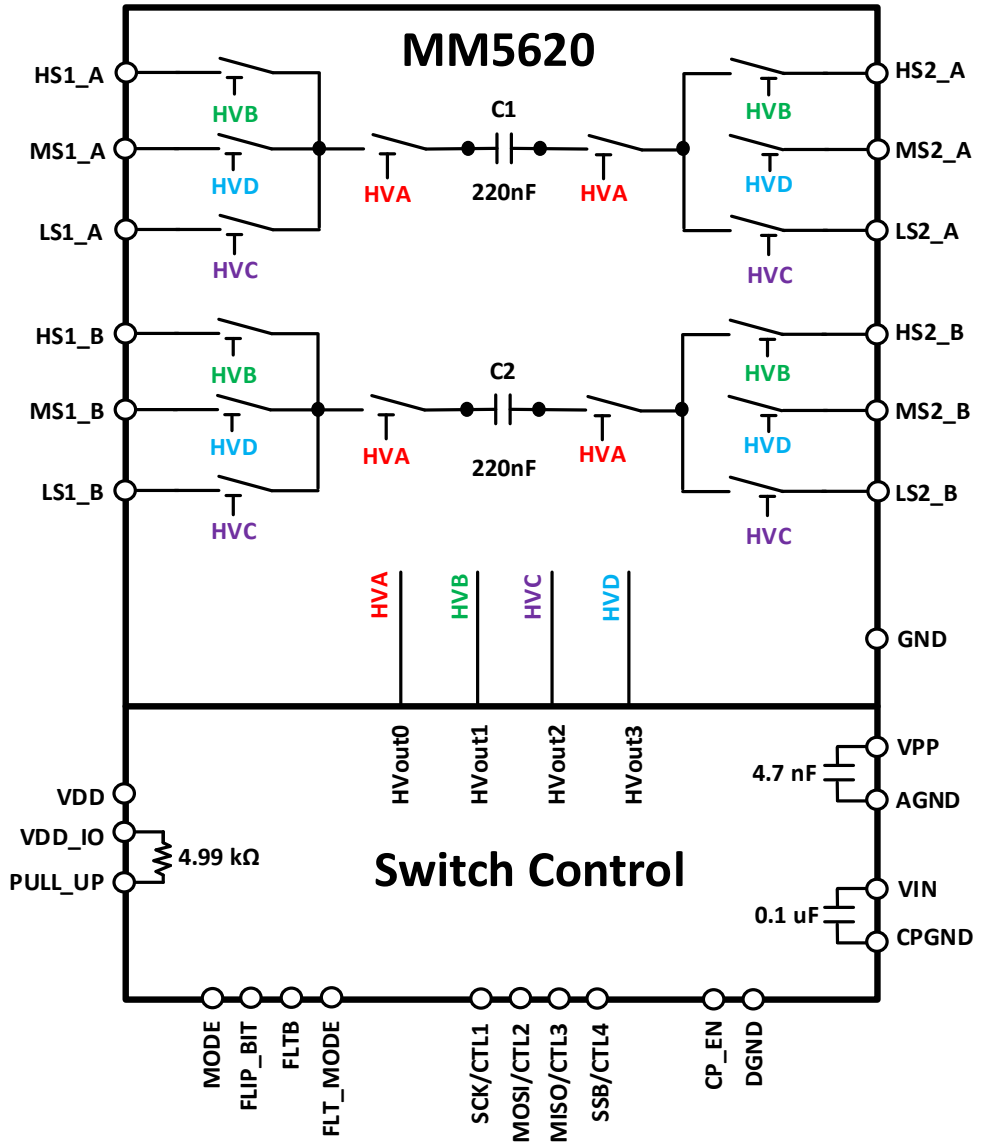
- Dual 2 Form C DPDT Differential Loopback Mode
- DC to 20 GHz range, up to 64 GT/s
- Optimized for PCIe Gen 5 & 6, SerDes
- Built-in AC coupling capacitors
- Integrated high-voltage driver
- Power supply +5 V (Charge Pump) and +3.3 V
- SPI and GPIO interface
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA



[Menlo MM5620 Preliminary Datasheet (menlomicro.com)]

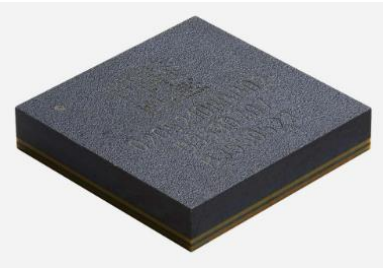
MM5620 - Functional Block Diagram

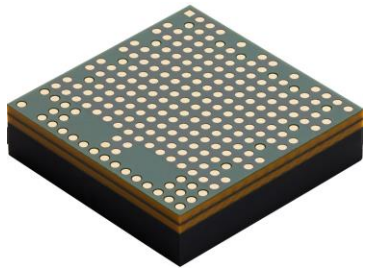
- Differential, Dual DP3T
- High-speed(HS) loopback path supports 64 GT/S PAM-4
- Flexible functionality:
  - HS1 → HS2 (loopback)
  - MS1 → MS2 (loopback)
  - HS → LS (ATE)
  - LS → LS (LS loopback)
  - HS1 → MS1 (ATE)
  - HS2 → MS2 (ATE)

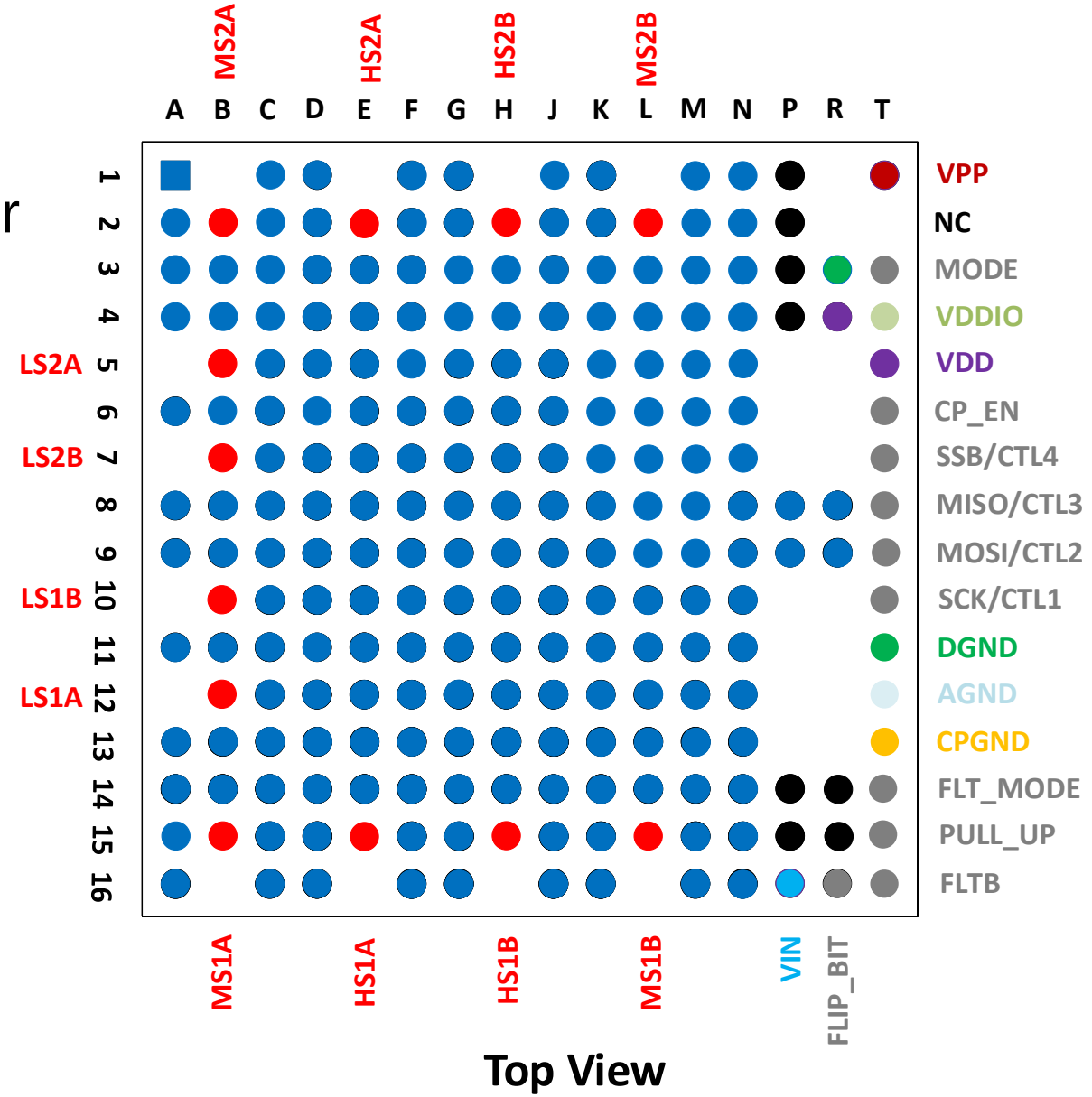


MM5620 - LGA 16x16 Footprint Diagram

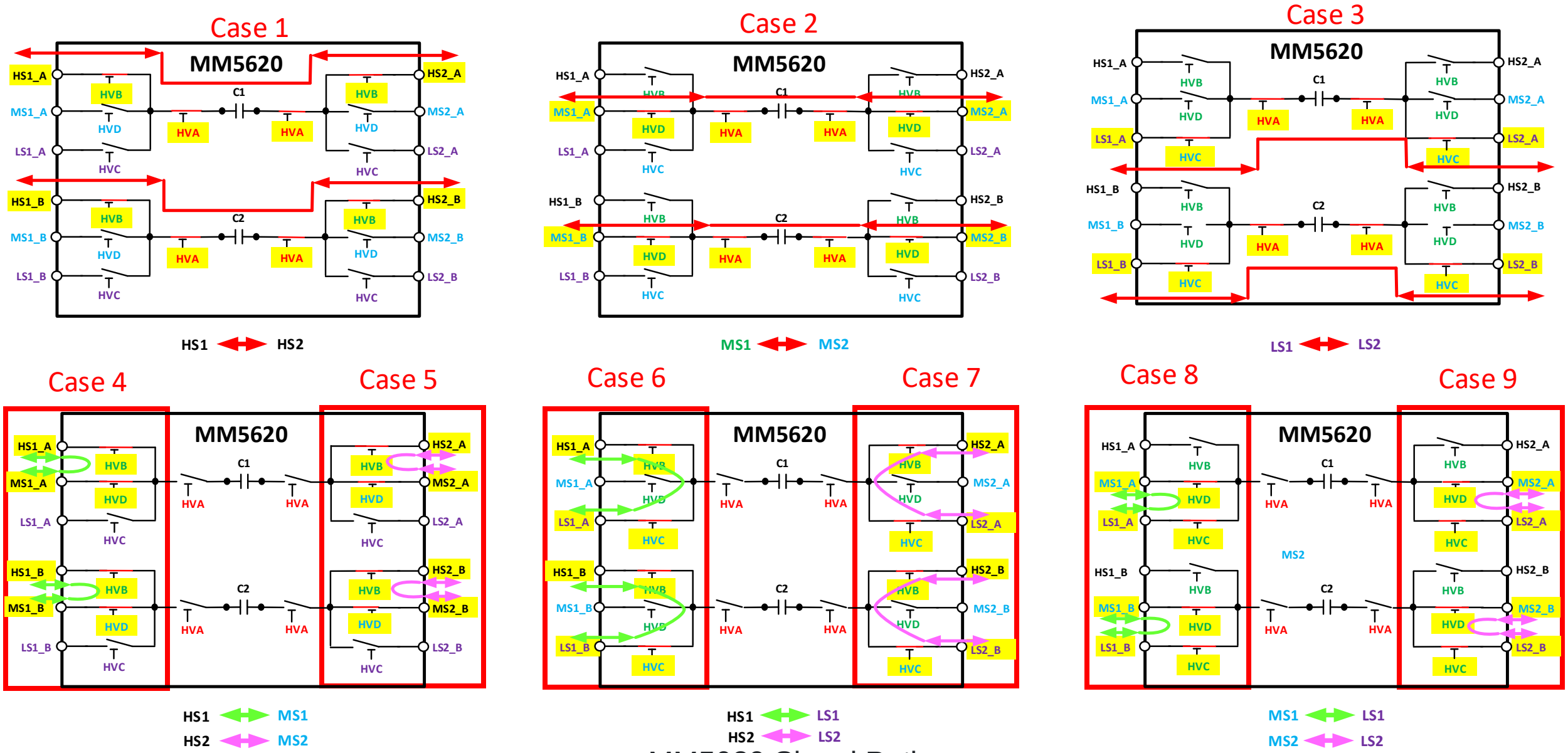
- Key Features:
  - Size: 8.2 x 8.2 mm^2
  - 0.5 mm pitch / 0.3mm pad diameter
  - 16x16 LGA array – with removed pads as needed
  - Internal V_{PP} capacitor
  - Internal 4.9k pullup resistor
  - Internal 0.1uF/10V Vin to CPGND bypass capacitor
  - SPI & GPIO control







MM5620 – Six Signal Paths, Nine Measurement Cases



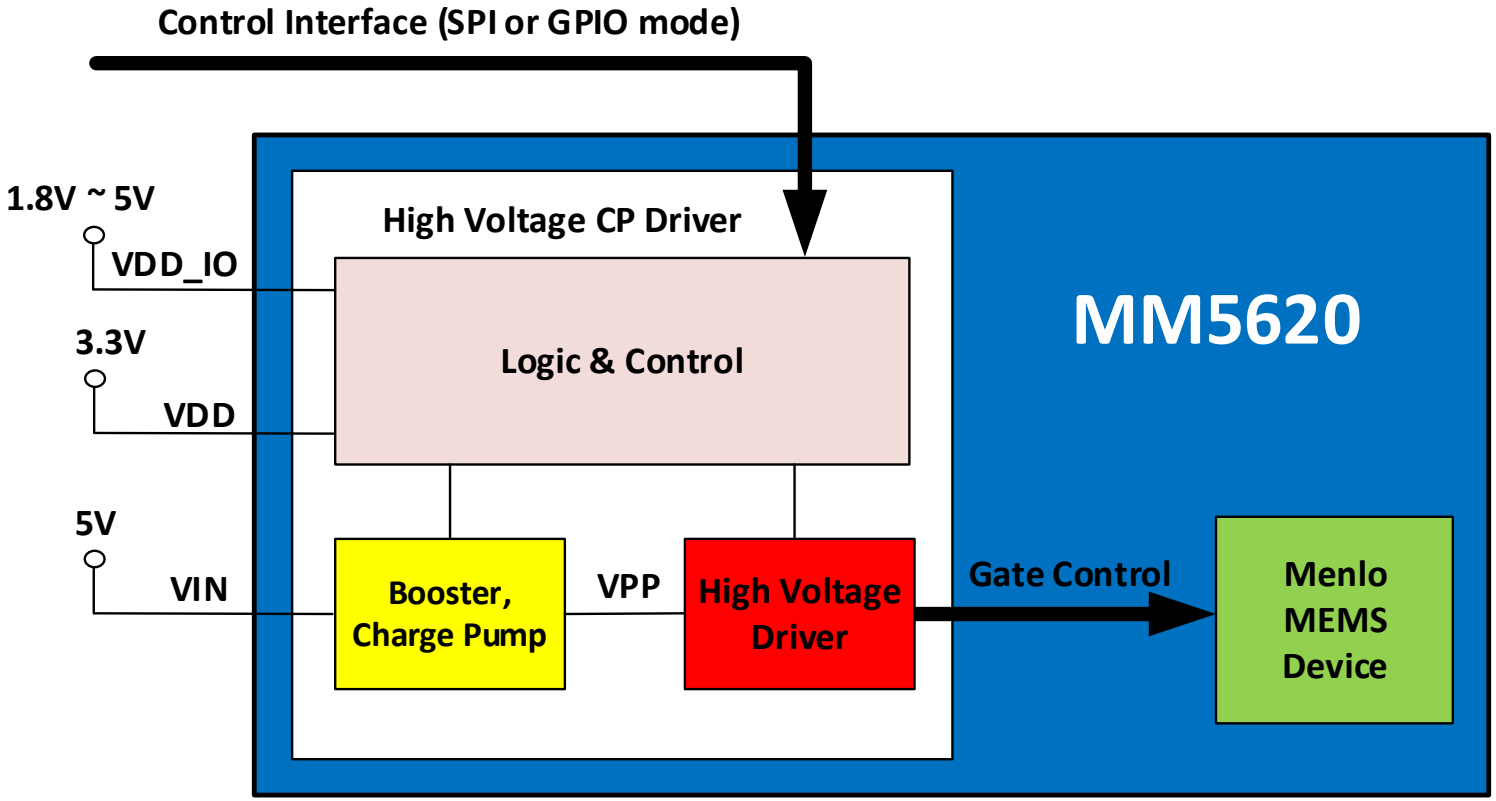
MM5620 Signal Paths

MM5620 – Measured S-Parameter Performance

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Differential Insertion Loss						
High Speed (HS1 to HS2)	SDD21		2.3		dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)			3.3			
HS1 to MS1			1.4			
HS2 to MS2			1.4			
HS1-LS1			2.9			@ 6 GHz, Not de-embedded
HS2-LS2			2.9			
MS1_LS1			3.1			
MS2_LS2			3.1			
Low Speed (LS1 to LS2)			3.0			@ 3 GHz, Not de-embedded
Differential Return Loss						
High Speed (HS1 to HS2)	SDD11		19		dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)			15			
HS1 to MS1			13			
HS2 to MS2			12			
HS1-LS1			23			@ 6 GHz, Not de-embedded
HS2-LS2			23			
MS1_LS1			25			
MS2_LS2			25			
Low Speed (LS1 to LS2)			27			@ 3 GHz, Not de-embedded

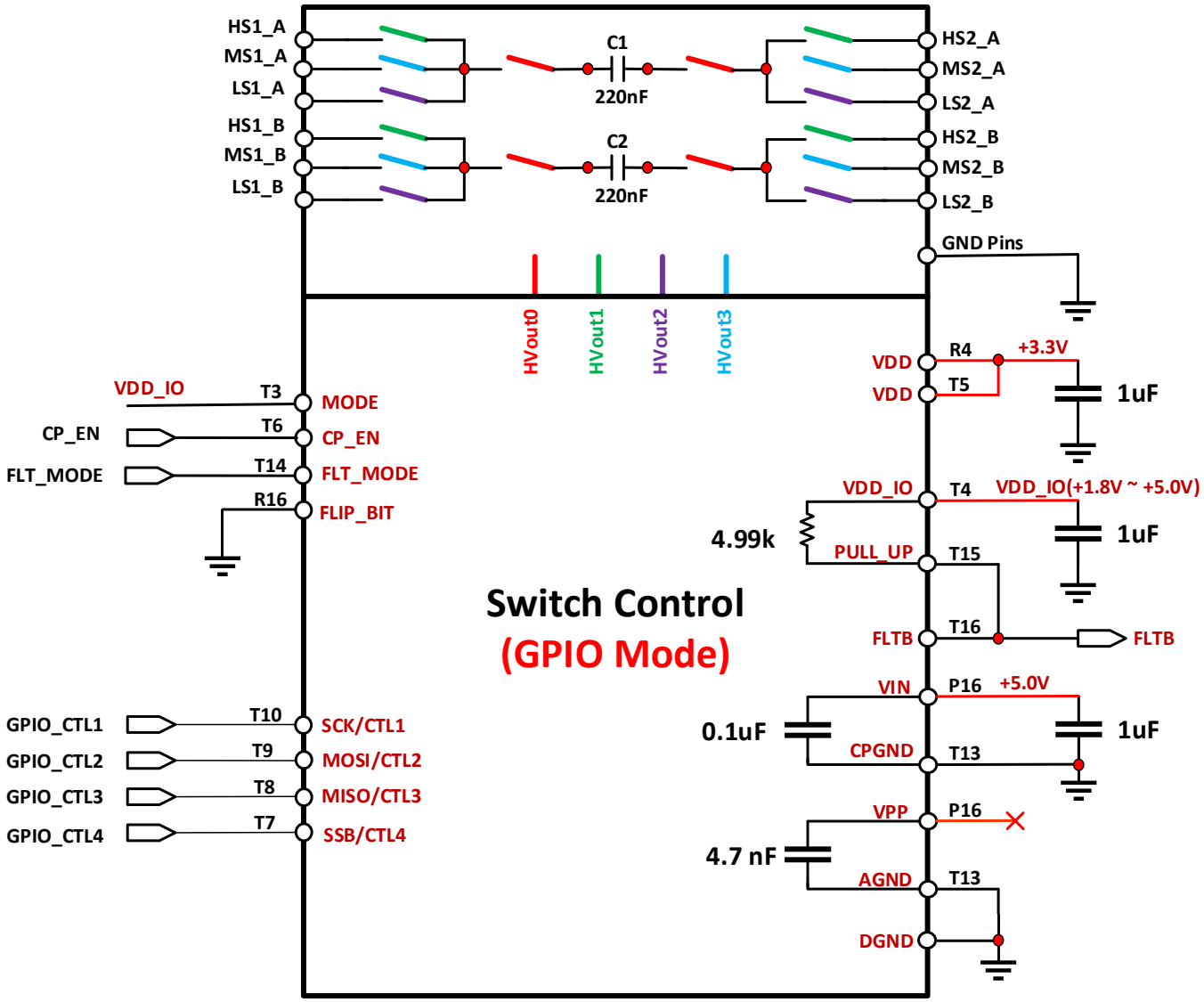
MM5620 - MEMS Switch Control Block Diagram

- The communication interface: GPIO and SPI
- VDD_IO: Digital I/O supply (+1.8V to +5.0V)
- VDD: +3.3V supply to analog circuits
- VIN: +5V supply to the internal charge pump



MM5620 – External Circuit (GPIO Mode)

- Enable the GPIO Mode:
  - MODE: Connect to VDD_IO
  - FLIP_BIT: Connect to GND
- Enable the Charge Pump
  - CP_EN: Connect to VDD_IO
- Disable the Fault Mode:
  - FLT_MODE: Connect to VDD_IO
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CP_EN pin low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor



MM5620 – External Circuit (SPI Mode)

- Enable the SPI Mode:
  - MODE: Connect to GND
- Enable Spread Spectrum:
  - FLIP_BIT: Connect to VDD_IO
- Enable the Charge Pump
  - CP_EN: No connect
- Disable the Fault Mode:
  - FLT_MODE: Connect to VDD_IO
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CP_EN pin low and then high to re-start the IC
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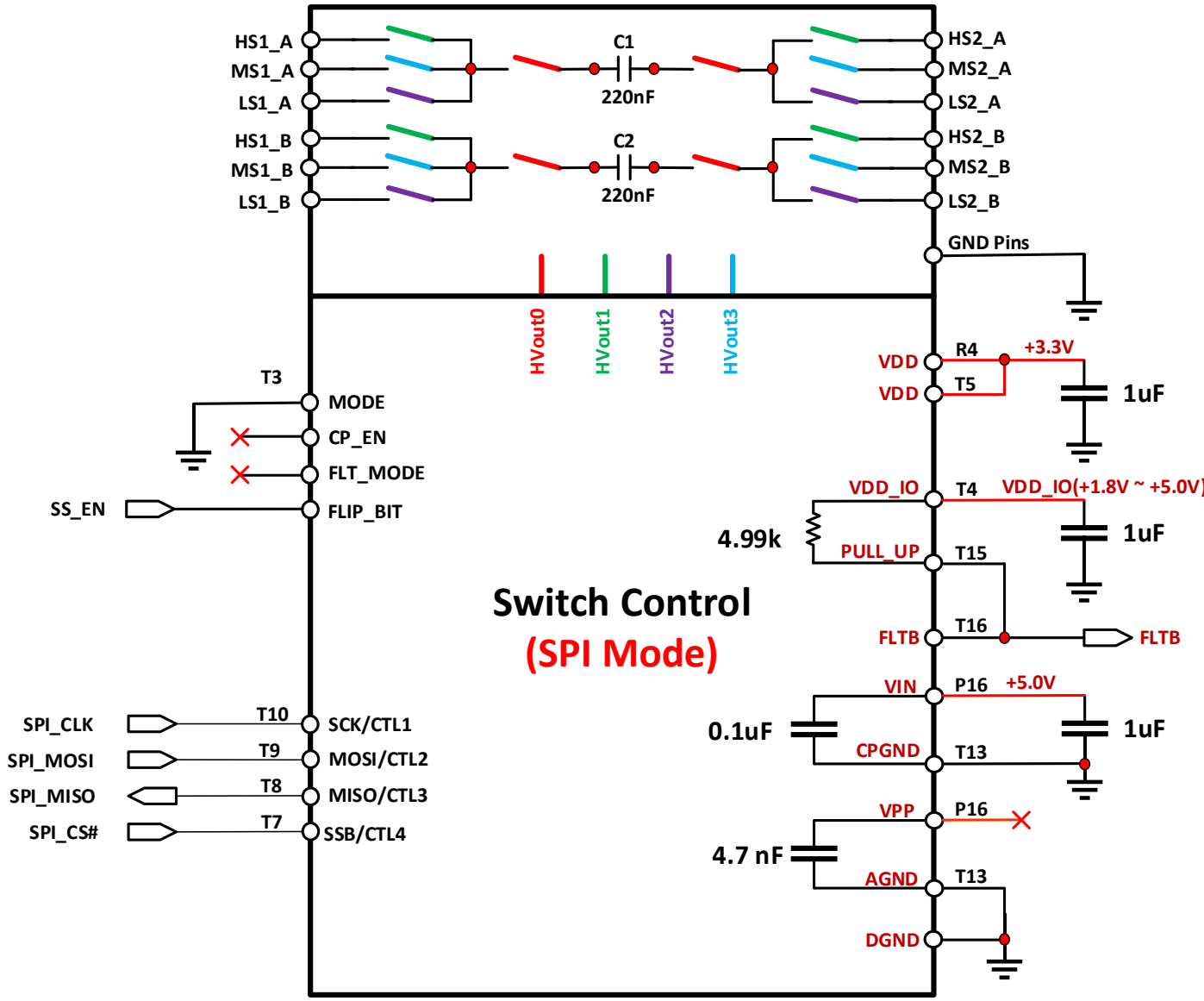
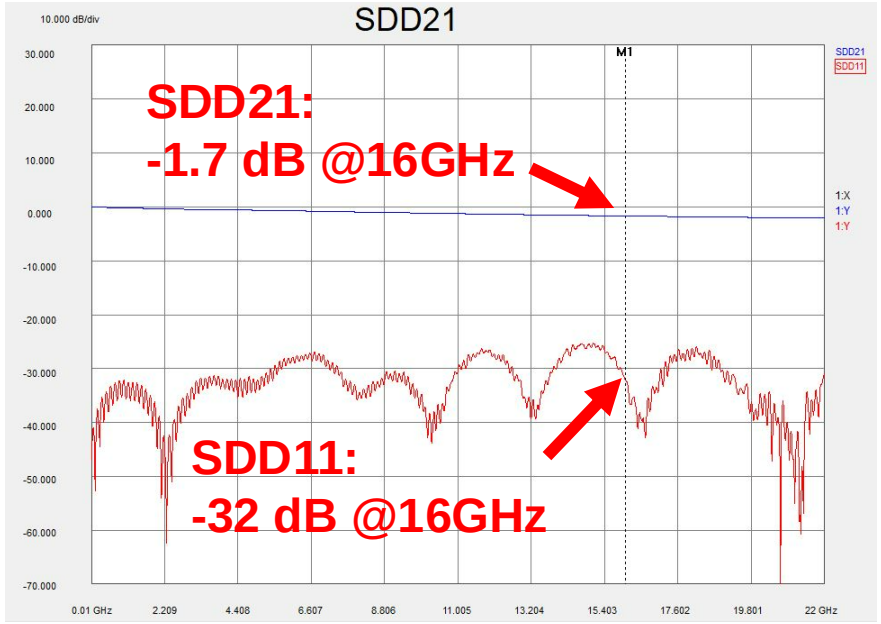
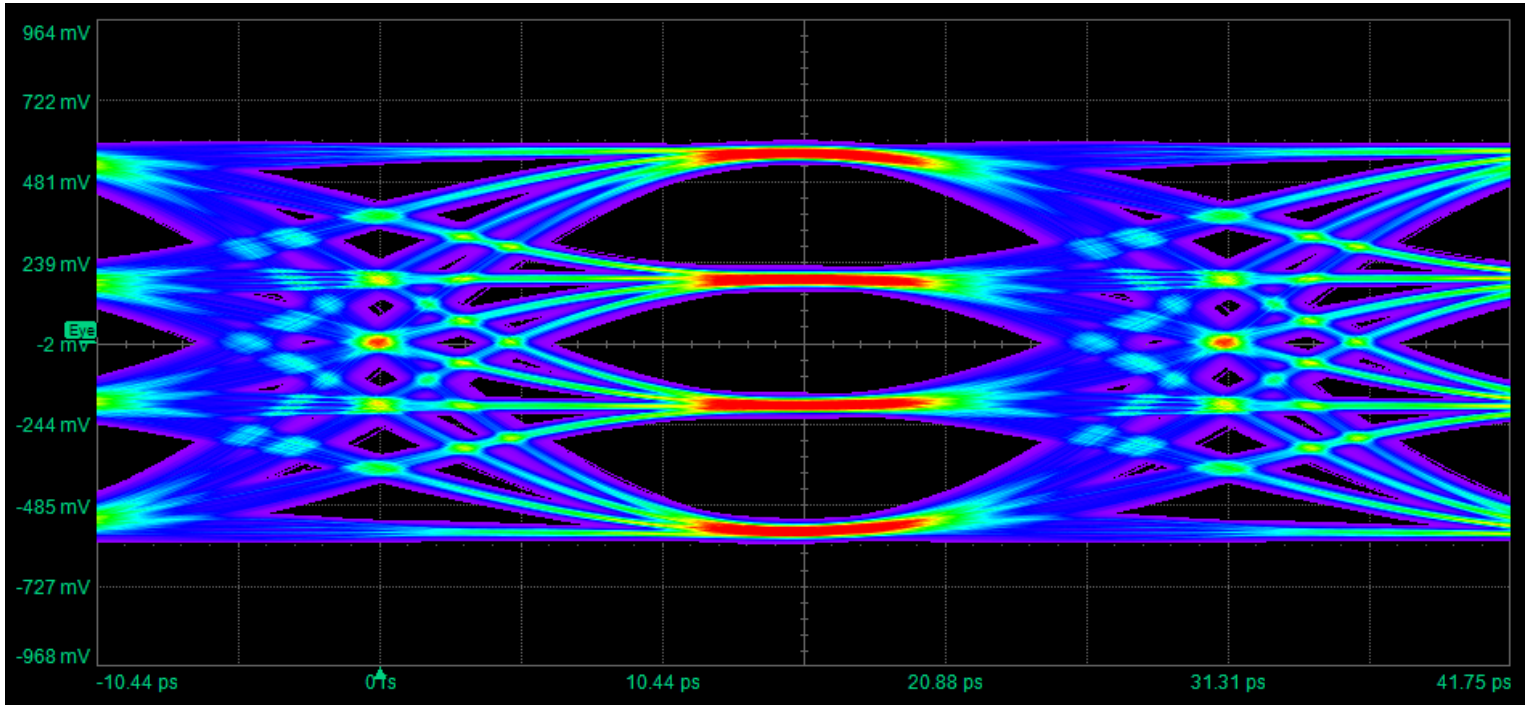
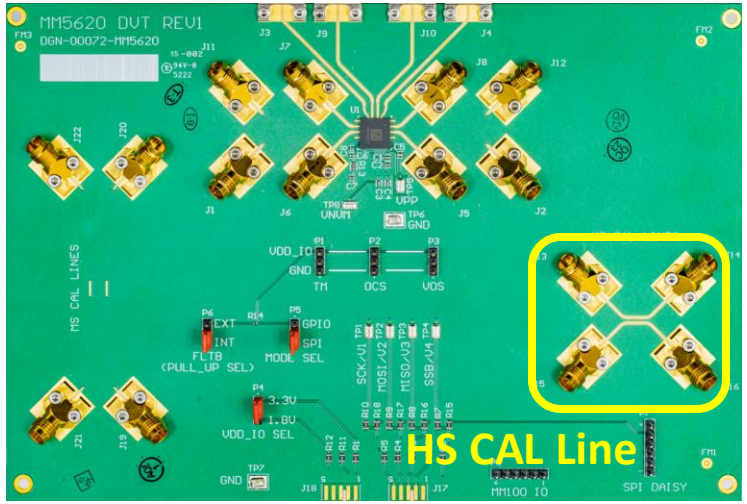


MM5620 - S-Parameter Performance (HS CAL Line)



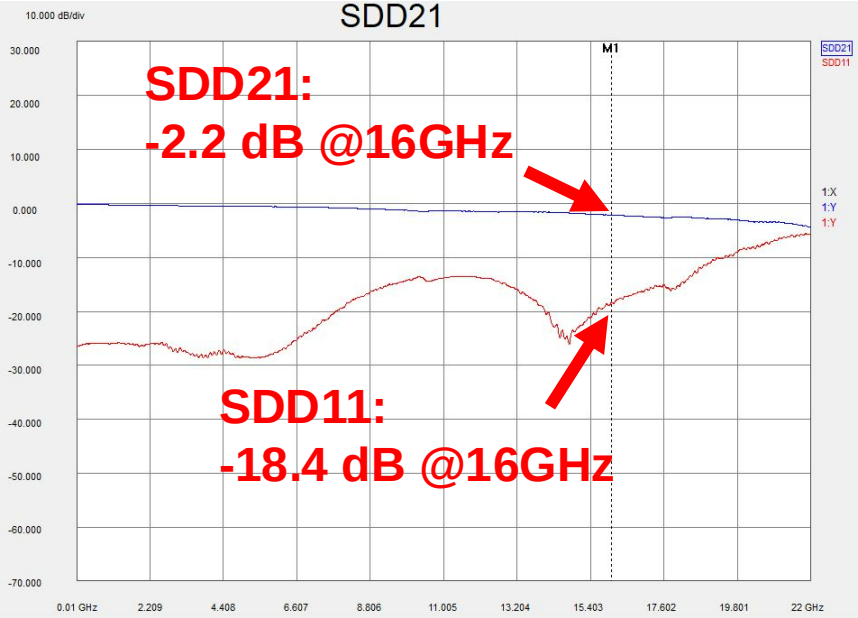


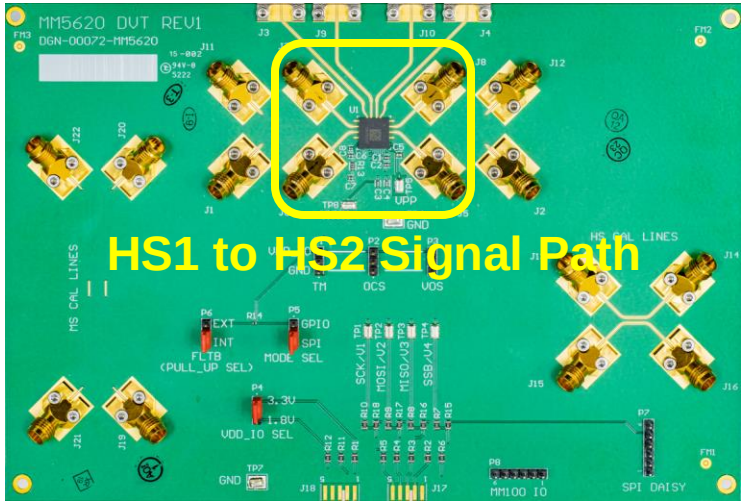


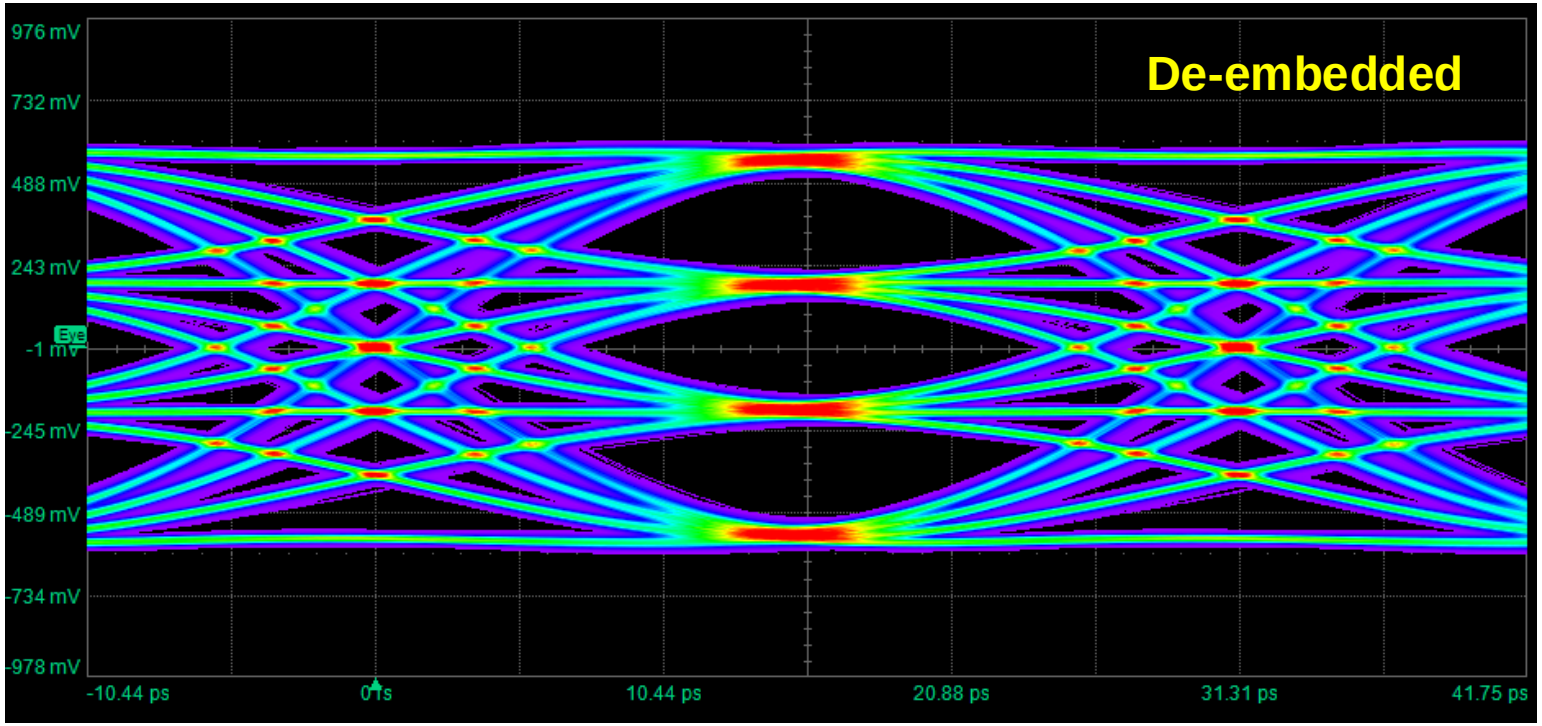
Eye-Diagram Test Conditions

- PCIe Gen6
- PAM4, 32 Gbaud, PRBS 2^{15}-1
- +600 mV/-600mV

MM5620 S-Parameter Performance (HS1 to HS2 Signal Path)



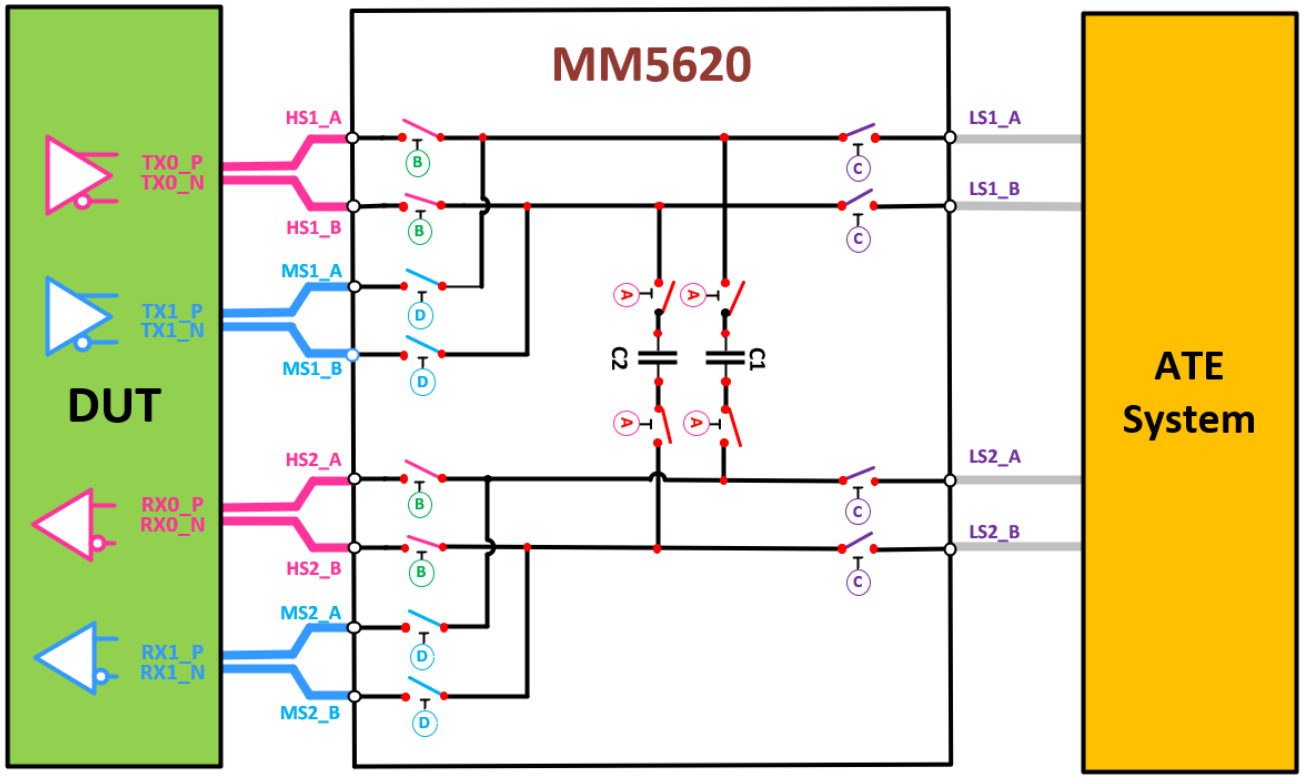




Eye-Diagram Test Conditions

- PCIe Gen6
- PAM4, 32 Gbaud, PRBS 2^{15}-1
- +600 mV/-600mV

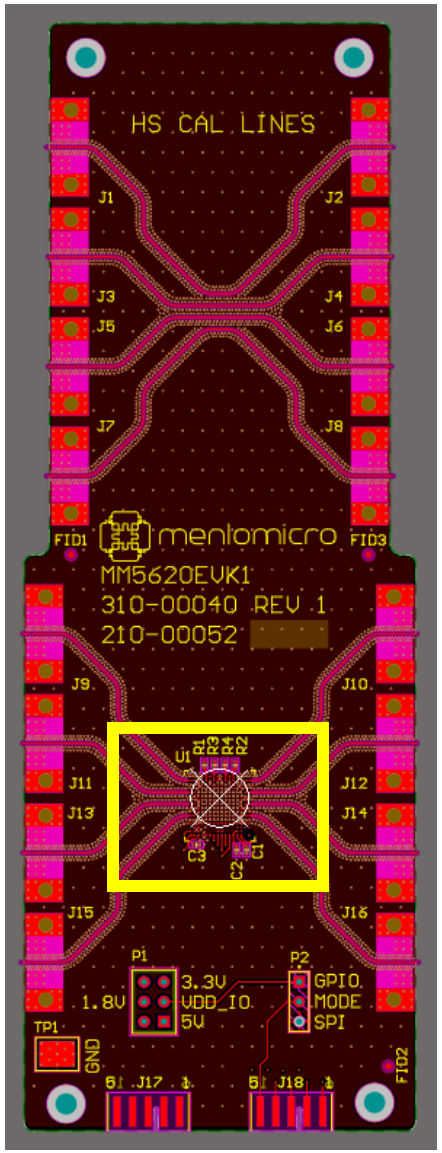
MM5620 – Double Density HSIO Loopback Mode Test



- Test Two PCIe 4/5/6 lanes at high-speed using ONE MM5620 device
  - TX0_X ← → RX0_X (HS1 ← → HS2) at speed test
  - TX1_X ← → RX1_X (MS1 ← → MS2) at speed test
- LS signals can be shared for low frequency and DC sweep test
- Two transmitters can be ALWAYS ON to reduce test time
- Fully bi-directional signal paths

MM5620 – Customer Evaluation Board

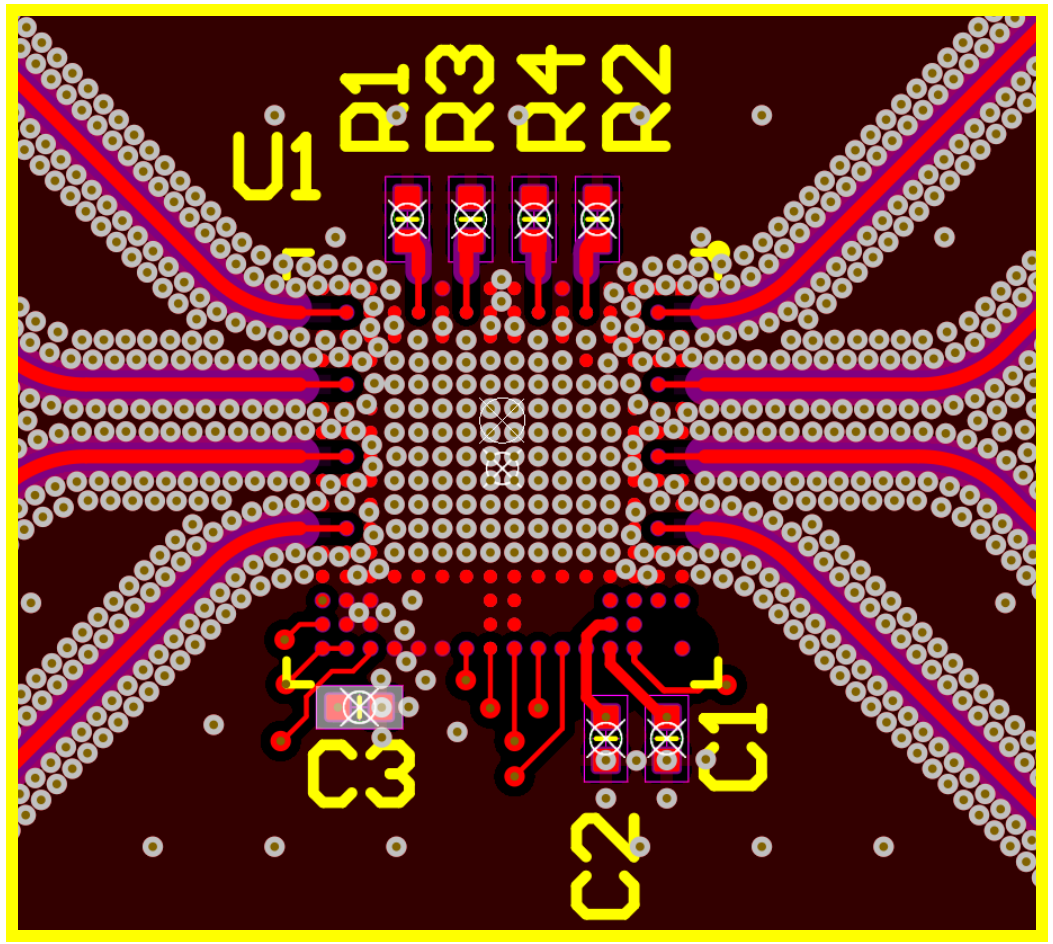
On-board
2X-Thru Fixtures



MS1A
HS1A
HS1B
MS1B

MS2A
HS2A
HS2B
MS2B

MM5620 EVK



MM5620 Area