High-Speed Loopback Applications by Utilizing a Differential DP3T MEMS Switch

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***Abstract*—This paper introduces a Differential DP3T MEMS switch for high-speed digital applications over 64 Gbps. Ever-increasing electronic system performance is forcing faster communication between chipsets and memories. Precision high-speed testing of chipsets on design-in-boards is forcing test engineers to utilize higher precision components on loopback paths. Switches to route the signals back into the DUT have become widely adopted on design-in-boards as a method for precision high-speed testing of chipsets. Many of these paths include PCIe 5.0/6.0, and other high-speed SerDes interfaces.**

One of the limiting factors with increasing data rates, such as PCIe 5.0/6.0 specifications, is the switch performance at higher frequencies. The MEMS switch has a switching speed of 10us versus milli seconds range for a bulky EM relay. This allows for a significant increase in test speed and DUT throughput. The small size of the device enables higher test site density so again increasing DUT throughput. The lifespan of the MEMS switch is three billion cycles, compared to up to ten million life cycles for EM relays could help reduce the test system downtime.

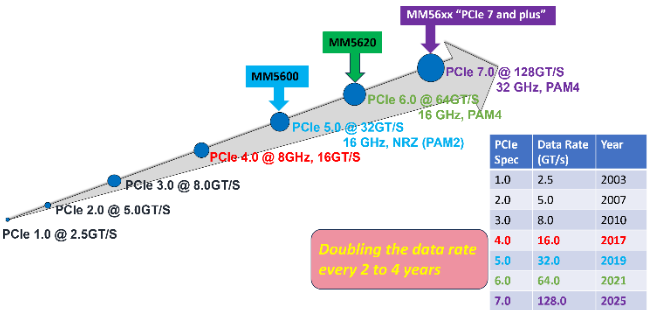
Keywords—SerDes, PCIe Gen5, PCIe Gen6, CXL, MEMS switch, Loopback test, Differential switch

I. Introduction

PCI Express is a common high-speed serial bus; as data consumption increases the required speed goes faster and faster. PCIe 6.0 is twice as fast as PCIe 5.0, PCIe 6.0 has a 64 Gbps data rate, compared to 32 Gbps with PCIe 5.0.

Historically Electromechanical relays (EMR) have been used to implement an external loopback test for automated test equipment (ATE) applications, but it become very difficult to use EMR to support testing above PCIe 4.0 specification.

A differential DP3T MEMS switch is designed for use in applications exceeding the data rates of PCIe 6.0 test. This differential DP3T MEMS switch provides many advantages over existing EM relay solutions.



PCIe Spec	Data Rate (GT/s)	Year
1.0	2.5	2003
2.0	5.0	2007
3.0	8.0	2010
4.0	16.0	2017
5.0	32.0	2019
6.0	64.0	2021
7.0	128.0	2025

Fig. 1. The History of PCI Express – Ideal Switch

II. Introduction of an RF MEMS Switch

For a loopback board using the differential DP3T MEMS switches, MM5620 device, utilizing the Ideal Switch technology from Menlo Microsystems Inc. Every signal path is individually controllable and can be daisy-chained for multiple switches. The test board includes a control interface through GPIO or SPI for actuating the switches.

All of Menlo's Ideal Switch products are made of the unit cell which consists of beam, contact, and gate. The unit cell architecture of the MEMS switch is illustrated in Fig 2. Figure 2 is not to scale and is for illustrative purposes only.

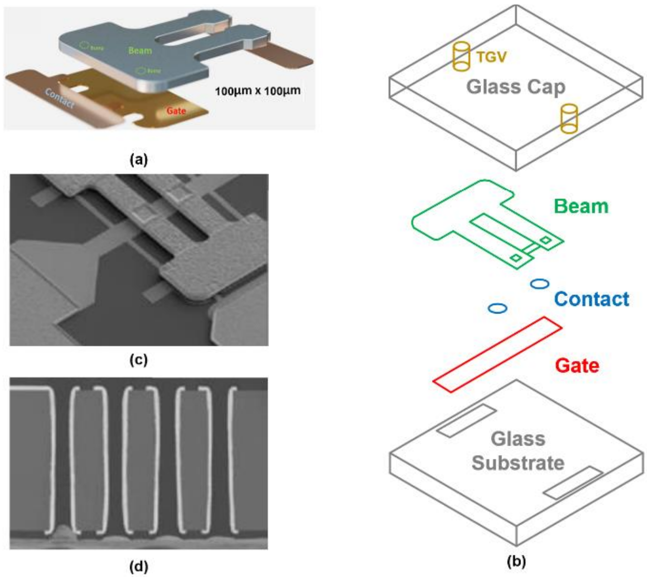


Fig 2. (a) (b) The Ideal Switch consists of the glass substrate, glass cap, through glass via, beam, contact, and gate. (c) The unit cell - only 100µm x 100µm.(d) Through Glass Vias, miniaturized packaging with the highest performance.

The MEMS switches are activated via electrostatic force, and thus require a high voltage source for switching operation. When the gate of the switch is set for a bias of 0 VDC, it places the metal cantilever beam in a non-deflected (off) state. Thus, the path between RF input and output is isolated with an air gap, like a traditional mechanical relay. When the gate is set to its required actuation voltage of +89Vdc, the electrostatic force that exists between the gate and cantilever beam is strong enough to cause it to deflect downward, forming a connection with the contact and closing the switch (on state).

Because the field is static, the current and power consumption is extremely low. The metallurgy in this beam and contact area gives reliability, of a minimum of 3 Billion cycles with typical performance closer to 50 Billion cycles. Our unique Glass Packaging provides better power handling, and improved RF performance. The Ideal Switch constructed on a glass substrate reduces parasitics and improves RF performance. It is very important to achieve much better insertion loss and linearity performance. The switch cavities are all hermetically sealed with a glass cap to enable stable resistance and switching performance. Through glass vias provide a low resistance path to get the electrical signals in and out of the package.

The MM5620 device has a built-in charge pump and high voltage driver as shown in Figure 3.

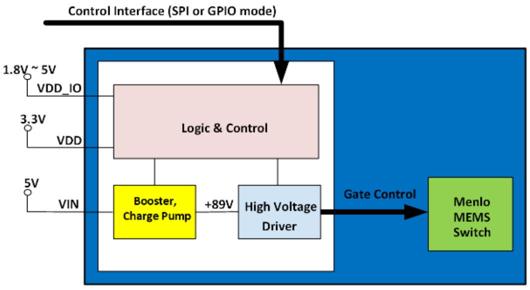


Figure 3. Control of the Ideal Switch

III. Scalable Switch Arrays With Ideal Switch

All Ideal Switch products are built using the same unit cell. Its size is very small, 100 um by 100 um and it allows easy scaling for high power handling through massive arrays. If the unit cells are placed in parallel we can get lower resistance and can carry higher current, if the unit cells are more in series, we can get higher standoff voltage, and off-channel isolation.

This scalability allows us to develop products that can meet a specific requirement. Menlo has been working with multiple customers to develop switch products targeting certain markets and application requirements.

There is an image of the system in a glass package, you can see the switches on the glass substrate, and the glass cap with the through glass vias.

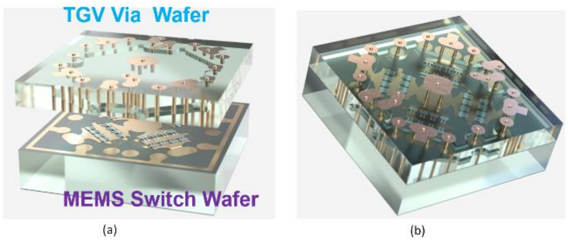


Figure 4. (a) TGV wafer and MEMS wafer (b) WL-CSP package, Thermo Compression Bonding, Hermetically Sealed

IV. Advantages of Ideal Switch®

The fundamental differences between one of Menlo's Ideal Switch products and semiconductor or solid-state switches are the losses and linearity. These can be traced back to a key figure of merit for switches called Ron Coff. This value is the On-resistance when the switch is turned on multiply the Off-capacitance when the switch is turned off. Given our metal-to-metal contact, glass insulating substrate, and air-gap open circuit, we have demonstrated Ron* Coff 5 times to 10 times lower than semiconductor switches. Our Ron Coff value for the MM5130 MEMS switch is 18 fS typical.

This is thanks to an ultra-low off capacitance, in the femto-Farad range. In addition, our switches have higher breakdown voltages than semiconductor switches and so can handle a lot more power. When it comes to comparing our products to conventional mechanical relays, the Ideal Switch enables products that are significantly smaller, in many cases more than 50 times smaller in volume.

The smaller size and smaller mass of our mechanical actuator allow us to have switching times 1000 times faster than conventional mechanical relays, and the innovations in materials enable a 1000 times longer lifetime.

V. PCIe Gen 6.0 – External Differential Loopback Using the MM5620/MM5622 Device

For High-Speed Loopback applications, Menlo developed the MM5620 differential Dual DP3T switch supporting the high-speed differential signal switching required in PCIe Gen 5 and 6 and high-speed SerDes applications.

It is the highest-performing differential switch in the market, targeting PCIe Gen 5 and 6, high-speed SERDES applications. The MM5620 is based on Menlo's Ideal Switch® technology and can operate up to 64 GT/s or 20 GHz for high-performance applications.

The Electromechanical Relays (EMR) have been used for loopback tests up to PCIe Gen4, but it has performance limitations for PCIe Gen 5 applications. There are many significant advantages to using the MM5620 switch over existing EM relay products.

Figure 5 shows a simplified functional block diagram and pinout of the MM5620 device. The upper part is the switch units and the lower part is the charge pump and high-voltage driver.

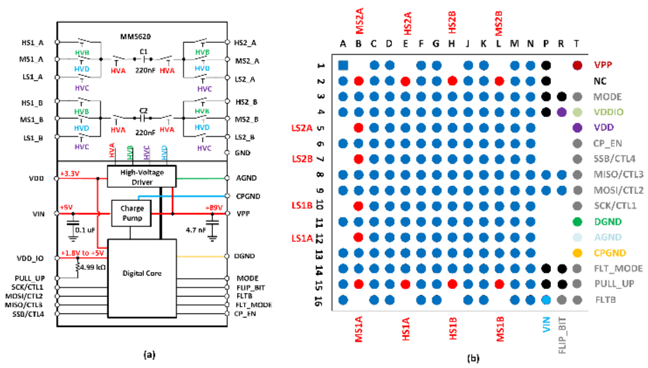


Figure 5. (a) Functional Block Diagram (b) MM5620 (8.2mm x 8.2 mm LGA) Top View

There are six possible controls as shown in Figure 6. Three are the loopback signal paths through AC coupling capacitors and the other three are the loopback signal paths without AC coupling capacitors.

Three possible signal paths are going through the AC coupling capacitors, high speed 1 to high speed 2, medium speed 1 to medium speed 2, and low speed 1 to low speed 2. Six more supported signal paths are not going through the internal capacitors.

These switches are controlled by four high-voltage outputs from the built-in switch control module. There are many differential signal paths supported and it gives flexible functionality.

The switch requires high voltage to drive the gate to control the switch on and off. The MM5620 device has an internal charge pump and a high-voltage driver. The charge pump input voltage is 5V and an additional digital supply is required this is selectable within the 1.8 to 5 V range on the VDD_IO pin and sets the level for digital communications with the device. The switch can be controlled using either GPIO or SPI mode.

The MM5620 provides high reliability and greater than 3 billion switching cycles guaranteed.

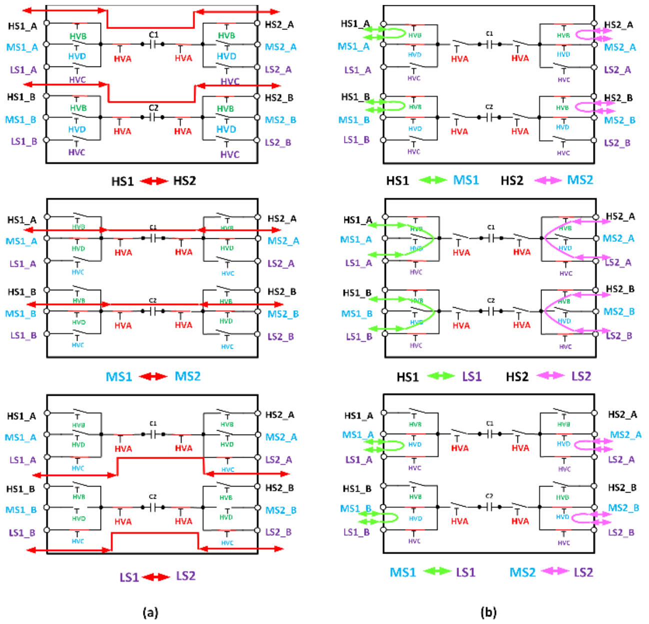


Figure 6. (a) Loopback signal paths through AC coupling capacitors. (b) Loopback signal paths without AC coupling capacitors.

Figure 7 shows differential insertion loss (SDD21) and differential return loss (SDD11) for the high-speed loopback path.

For the AC coupling signal paths, the high-speed one to high-speed two path shows a low insertion loss of about 1.49 dB and 28 dB of return loss at 16 GHz.

The mid-range return loss is a little bit worse than 15 dB of return loss, it can be improved by optimizing the PCB to PAD launch using a tear-drop transition. S-parameter files are available to assist in simulation of the board transition and overall performance during the design phase.

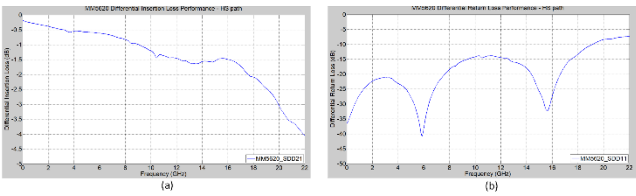


Figure 7. (a) SDD21 (b) SDD11

VI. MM5620 Eye-Diagram Performance – High-Speed Loopback Path

Figure 9 shows an eye diagram at 32 Gbaud (64Gbps). Table 1 shows eye-diagram performance, it was post-processed based on measured S-parameter performance. The three eyes are wide open and clean.

Test conditions for measurements are as below:

- PCIe Gen 6.
- PAM4, 32 Gbaud (64Gbps).
- PRBS 2^{15}-1.
- 500mVp-p (+250mV/-250mV).
- RF connector and RF traces are de-embedded.
- Measured differentially on the MM5620 Evaluation board (Figure 8).

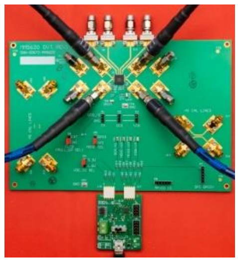


Figure 8. MM5620 Evaluation Board

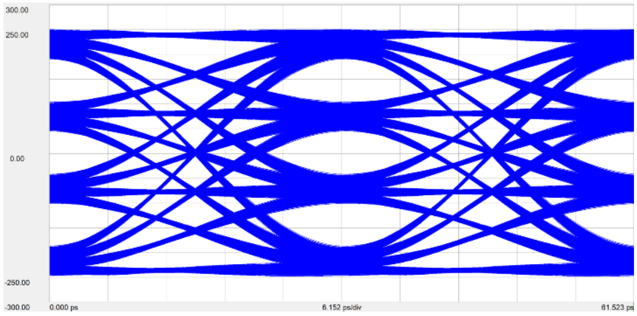


Figure 9. MM5620 PAM4 Eye-Diagram

For applications with built-in AC Coupling capacitors the MM5622 device is available and does not have built-in AC-coupling capacitors, it supports only DC-coupled signal paths.

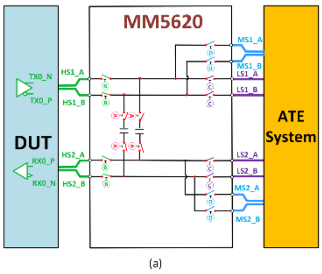
Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	64	83.6	11	10.2
1/2	64	84.2	13	8.5
2/3	64	84.2	11	10.4

Table 1. MM5620 PAM4 Eye-Diagram Performance

VII. MM5620 Use Case

The MM5620 devices are widely adopted in the test and measurement industry to perform full PCIe Gen6 validation as well as full CXL(Compute Express Link) validation. It enables single insertion testing, covering the at-speed, 64 Gbps, signal loopback test, providing access to the tester's high-speed instruments, and also providing access to DC instrumentation for parametric measurement.

Figure 10 shows an example of how to perform these three tests using a single MM5620 device.



Test Mode	HVA LB	HVB HS	HVC LS	HVD MS
PCIe G6 Loopback	ON	ON	OFF	OFF
Scan test	OFF	ON	OFF	ON
DC/Low freq test	OFF	ON	ON	OFF
All OFF	OFF	OFF	OFF	OFF

(b)

Figure 10. (a) PCIe G6 loopback test block diagram (b) Truth table

VIII. HIGH-SPEED DIGITAL PCB DESIGN

To achieve a good high-speed PCB design to meet the specific design target, it is very important to get a deep understanding of your fabrication houses' capability and details of their design rules in advance, then work very closely together with them.

Most high-speed differential lines use either an edge-coupled microstrip or an edge-coupled stripline. A differential pair can be implemented as loosely or tightly coupled. Figure 11 shows differential Microstrip vs. differential Stripline construction, and Table 2 describes the pros and cons between the loosely and tightly coupled trace routing options.

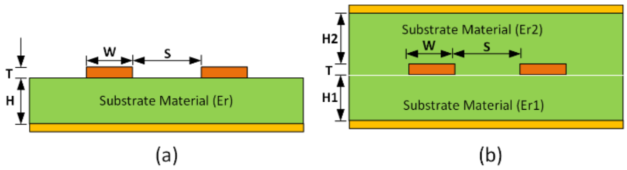


Figure 11. T(Copper Thickness), W(Trace Width), S (Spacing), H (Substrate Height), and B (Substrate height) (a) edge-coupled microstrip (b) edge-coupled stripline

Routing	Advantage	Disadvantage
Loosely Coupled	• Thinner dielectrics required for the same trace width • Less sensitivity to trace-to-trace variations provides better impedance control	Consumes more PCB area
Tightly Coupled	• Higher routing density • Smaller trace width for the same trace impedance • Better common mode noise rejection	Impedance control is highly sensitive to trace-to-trace variations

Table 2. Loosely vs. Tightly Coupled Trace Routing

PCIe Gen6 uses the Nyquist frequency of 16 GHz, the material choices, their properties, and their manufacturing tolerances must be carefully considered and modeled as they can lead to signal integrity issues.

The signal attenuation from the substrate material includes dielectric loss, conductor loss, reflections due to mismatched impedance, and radiation loss. Losses due to radiation are usually very small and negligible. The remaining losses can be attributed to the various properties of the substrate material choice. Material properties that directly affect the link performance include:

- Loss tangent (tan(δ)/Df)
- Dielectric constant (Er/Dk)
- Fiberglass weave composition
- Copper surface roughness

The skin depth also needs to be considered; at RF and microwave frequencies the current is conducted at the surface of the transmission line and that depth of current flow is called skin depth. For low-loss designs, it is best to avoid Nickel in the plating (ENIG/ENEPIG), even a very thin layer of Nickel will cause high loss due to its low skin depth and the majority of the current being carried in the high loss Nickel layer.

It is important to choose better dielectric material with low dielectric constant, low-loss tangent, better surface roughness, Reverse Treated Copper Foil, and better PCB finish (plating method) such as EPIG, ISIG, EPAG, etc. if the design has high-speed routing on top/bottom layer.

For the differential signals, routing should be smooth with minimum bends, and tight length matching is required. Stitching vias are required to be placed along all the high-speed routing from DUT to connectors. If space allows, it is ideal to implement two rows of stitching vias along the RF signals routing as the operating frequency approaches 20 GHz. Optimizing via transitions is necessary to minimize the impedance mismatch. A TDR simulation using 3D EM tools is a good method to check the impedance of vias and optimize it. The solder mask needs to be removed on high-speed traces.

Although it takes additional time, confirmation by running post-layout full 3D EM simulation, to obtain s-parameter, TDR, and eye diagram results, is a must to ensure that the board layout can meet the requirements.

IX. CONCLUSION

The MM5620 device, Menlo's differential DP3T switch, is introduced. This device can support the PCIe Gen6 loopback test and can be used for PCIe Gen5 applications for improved performance and reliability by replacing EMR relays on the existing load boards.

We presented the eye diagram of the MM5620 device to ensure that the load board design can meet the PCIe Gen6 requirements. An excellent eye-diagram performance is achieved at 64 Gbps signal without pre-emphasis or equalization enabled.

Test engineers requiring an RF switch that meets the requirements for PCIe Gen5/6 performance while saving crucial space in the load board and improving reliability will appreciate a MEMS-based approach solution that is also cost-competitive to EM and solid-state solutions.

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