Preliminary Datasheet
MM101– 8 Channel MEMS High Voltage Driver

Product Overview

Description

The MM101 is an 8-Channel Low-Voltage Serial to High-Voltage Parallel Converter with Push-Pull Outputs and an Internal Charge Pump Converter. The device is designed for MEMS applications where high voltage generation and driving capability are desired in a high integration form factor. The internal Charge Pump operates with a 5.0 V input source to generate a high-voltage source for the 8-Channel Output Drivers. The circuitry includes Power-On-Reset and Power ON/OFF Sequence Control. The communication interface consists of two modes of operation: GPIO and SPI, selected with the input control MODE pin.

Features

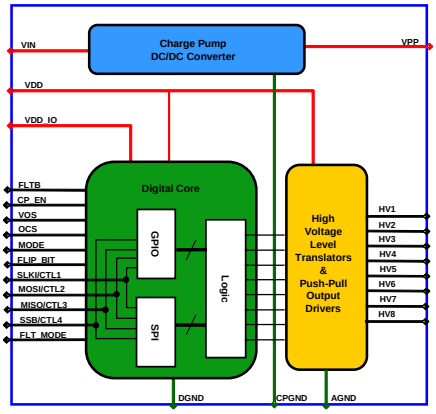
- Eight High-Voltage Push-Pull Output Channels
- Internal Charge Pump Voltage Converter
- Power-On-Reset (POR)
- Selectable Communication Interface (SPI, GPIO)
- Up to 33MHz SPI Clock Speed
- VDD_IO Supply allows I/O levels to range from 1.8V to 5.0V
- SPI can be daisy-chained
- Under Voltage Protection for VPP and VDD
- Fault Indicators (Latched SPI register bit and unlatched Open-Drain FLTB pin)
- Available in a 5x5mm QFN package, and WLCSP Flip Chip package.

Applications

- Microelectromechanical Systems
- Displays
- High Voltage Driver Applications

Markets

- Load/DIB for Semiconductor Test
- RF Systems
- Test and Measurement



RoHS COMPLIANT

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM101 should be restricted to the limits indicated in Recommended Operating Conditions

Electrostatic Discharge (ESD) Safeguards

The MM101 is a Class 0 ESD device. When handling the MM101, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Power Sequencing

Power-Up Sequence

- Connect Ground
- Apply VDD, VDD_IO and VIN – no supply sequencing restrictions on VDD, VDD_IO and VIN.
- Apply VPP (if using external high voltage supply)
- Apply input control signals

Power Down Sequence

- Reverse the order of the Power-Up sequence.

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	VDD	-0.3	3.6	V
I/O Supply Voltage	VDD_IO	-0.3	5.5	V
Charge Pump Input	VIN	-0.3	5.5	V
Charge Pump High Voltage Output	VPP	-0.3	105	V
Logic Input Voltage		-0.3	VDD_IO + 0.3	V
ESD rating of low voltage pins HBM			2000	V
ESD rating of VPP pin HBM			1000	V
ESD rating of HV# pins HBM			500	V
Junction Temperature Range		-55	165	°C
Storage Temperature Range		-55	165	°C

Table 2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Conditions
High Voltage Supply	VPP	10	100	V	If using external VPP supply
High-level input voltage	V_{IH}	0.7 * VDD_IO	VDD_IO	V	
Low-level input voltage	V_{IL}	0	0.3 * VDD_IO	V	
Operating Temperature		-55	125	°C	Ambient

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted (Note 1). Operating with all analog and digital GND pins connected to system ground (0 V). VPP = 85V, CPP = 4.7nF, unless otherwise specified.

Table 3 Power Supply Specifications

Parameter	Symbol	Note	Min	Typ	Max	Unit	Test Conditions
Charge Pump Power Supply	VIN		4.5	5.0	5.5	V	
VIN Current (Dynamic)	I_{VIND}	2		1.5	2.5	mA	Charge pump ON, VPP = 85V, I_{OUT} = 20uA, outputs switching at 10 kHz, C_L = 2pF per CH.
VIN Quiescent Current	I_{VINQ}			1.25	2.0	mA	Charge pump ON, VPP = 85V, I_{OUT} = 20uA, all I/O static
Low Voltage Logic Supply	VDD	2	3.0	3.3	3.6	V	
VDD UVLO Rising Threshold	$UVLO_{RISE}$		2.77	-	2.95	V	

VDD UVLO Falling Threshold	$UVLO_{FALL}$		2.72		2.90	V	
Low Voltage Digital Current	I_{DD}		-	400	500	µA	SPI mode outputs switching at 10 kHz, OCS = 0, C_L = 2pF per CH.
Low Voltage Digital Quiescent Current	I_{DDQ}		-	285	350	µA	Charge Pump OFF, all I/O static
Low Voltage Digital Sleep Mode Current	$I_{DDSLEEP}$		-	<1	10	µA	Charge pump OFF, Sleep Mode ON
Logic Reference Level	VDD_IO		1.71		5.25		
I/O Logic Supply Current	I_{DD_IOQ}			<10	50	uA	Outputs switching at 10 kHz.

Table 4 Digital Interface AC and DC Specifications

Parameter	Symbol	Note	Min	Typ	Max	Unit	Test Conditions
Logic I/O Level High	I/O_{VH}		0.7 x VDD_IO		VDD_IO	V	
Logic I/O Level Low	I/O_{VL}		0	-	0.3 x VDD_IO	V	
Logic I/O Hysteresis (SCK only)	I/O_{VH}		-	0.25	-	V	
Digital Input Capacitance (MM101-03)	C_{IN}			3	5	pF	
SDO Load Capacitance	C_{SDO}	3,4	-	-	10	pF	
SDO Source Current @ VDD_IO: 5 V 3.3V 1.8V	I_{SDOH}		 180 75 20	 290 140 35	-	mA	VOUT = 0.8 x VDD_IO

SDO Sink Current @ VDD_IO: 5.0 V 3.3 V 1.8 V	I_{SDOL}		140 65 20	260 140 40	-	mA	VOUT = 0.2 x VDD_IO.
Pull up current at SSB pins	I_{VOS}		-	20	-	µA	SSB pull-up is only in SPI mode
SSB pull-up resistor (to VDD_IO)	R_{PU}	-	120	200	280	kΩ	SPI MODE
Internal pull down resistors	R_{PD}	7	120	200	280	kΩ	SSB pull down is only in GPIO mode
CP_EN pin toggle low time	T_{TOGGLE}		500	-	-	ns	Minimum time CP_EN has to be held low to re-start the IC from fault condition
FLTB pin max sink current			65	140		mA	FLTB = GND VDD_IO=3.3V

Table 5 Digital Interface Timing Specifications

Parameter	Symbol	Note	Min	Typ	Max	Unit	Test Conditions
SPI Clock Frequency	SCK		-	-	33	MHz	
SDI Valid to SCK Setup Time	t_{SU}	2	2			ns	
SDI Valid to SCK Hold Time	t_{HD}		5			ns	
SCK High Time	t_{HI}		15.5	-	-	ns	
SCK Low Time	t_{LO}		15.5	-	-	ns	
SSB Pulse Width	t_{CSH}		15	-	-	ns	
LSB SCK to SSB High	t_{CSHLD}		15	-	-	ns	
SSB Low to SCK High	t_{CSSU}		15	-	-	ns	

SDO Propagation Delay from SCK Falling Edge	t_{SDOH}		10	-	-	ns	C_L = 10pF
SDO Output Valid after SSB Low	t_{CSDO}		20	-	-	ns	
SSB Inactive to SDO High Impedance	t_{SDOZ}		-	-	10	ns	

Table 6 Charge Pump and Driver Specifications

Parameter	Symbol	Note	Min	Typ	Max	Unit	Test Conditions
High Voltage CP Output Low Level High Level	VPP		77 87	80 90	83 93	V	
Maximum Charge Pump Output Current	$I_{CP,MAX}$		15			µA	VIN = 4.5V VPP = 85V
Charge Pump Output Ripple (peak-to-peak)	V_{RIPPLE}	2	-		10	mV	All HV Driver Outputs Off
Droop in VPP voltage	V_{DROOP}	2	-	-	0.2	V	
Power-On-Reset	POR	3	-	1.25	2.50	ms	Delay from application of VIN and VDD to all circuits active and stable
Charge Pump Start-Up Time	T_{ST}	5	-	20	33	ms	VIN = 4.5V, VPP = 90V I_{OUT} = 20uA VPP bypass C = 4.7nF
Driver Output Voltage High	HV_{OH}		VPP-1		-	V	

Driver Output Voltage Low	HV_{OL}		-	-	1	V	
Driver Output Current Low Level High Level	$I_{HV\#}$		24 48	30 60	36 72	µA	Per channel VPP = 85 V
Output Enable Rising Threshold	V_{EN}		75 65	78 68	81 71	V	VOS=HIGH VOS=LOW
Output Disable Falling Threshold	V_{DIS}		68 58	71 61	74 64	V	VOS=HIGH VOS=LOW
Spurious Performance	P_{SPUR}	6			-123	dBm	Spread Spectrum ON

Notes:

1. Specs are production tested at room temperature with temperature guard bands built into the limits unless otherwise noted.
2. Specification is obtained by characterization.
3. Specification is for design guidance only.
4. SDO load capacitance = PCB trace from SDO to input port (MM101 SDI or µC) + receiver C_{IN}
5. (from CP_EN pin or bit toggled high to VPP rises to 90% of set value)
6. Clock power measured in the RF path of an MM5130 MEMs switch. Measured with one channel enabled, and with 50Ω terminations on all RF ports.
7. The following pins have pull-down resistors: SDI, SCK, SSB, CP_EN, FLIP_BIT, OCS, and FLT_MODE.

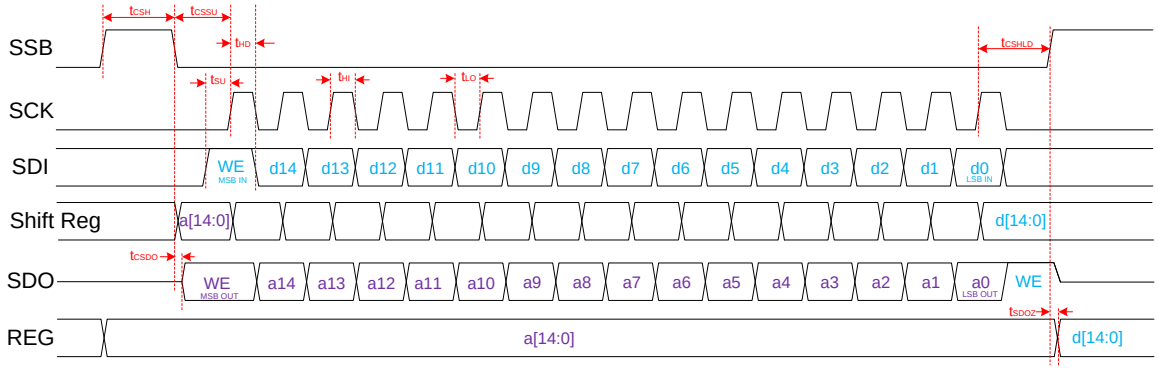


Figure 1: SPI Timing Diagram

Functional Block Diagram

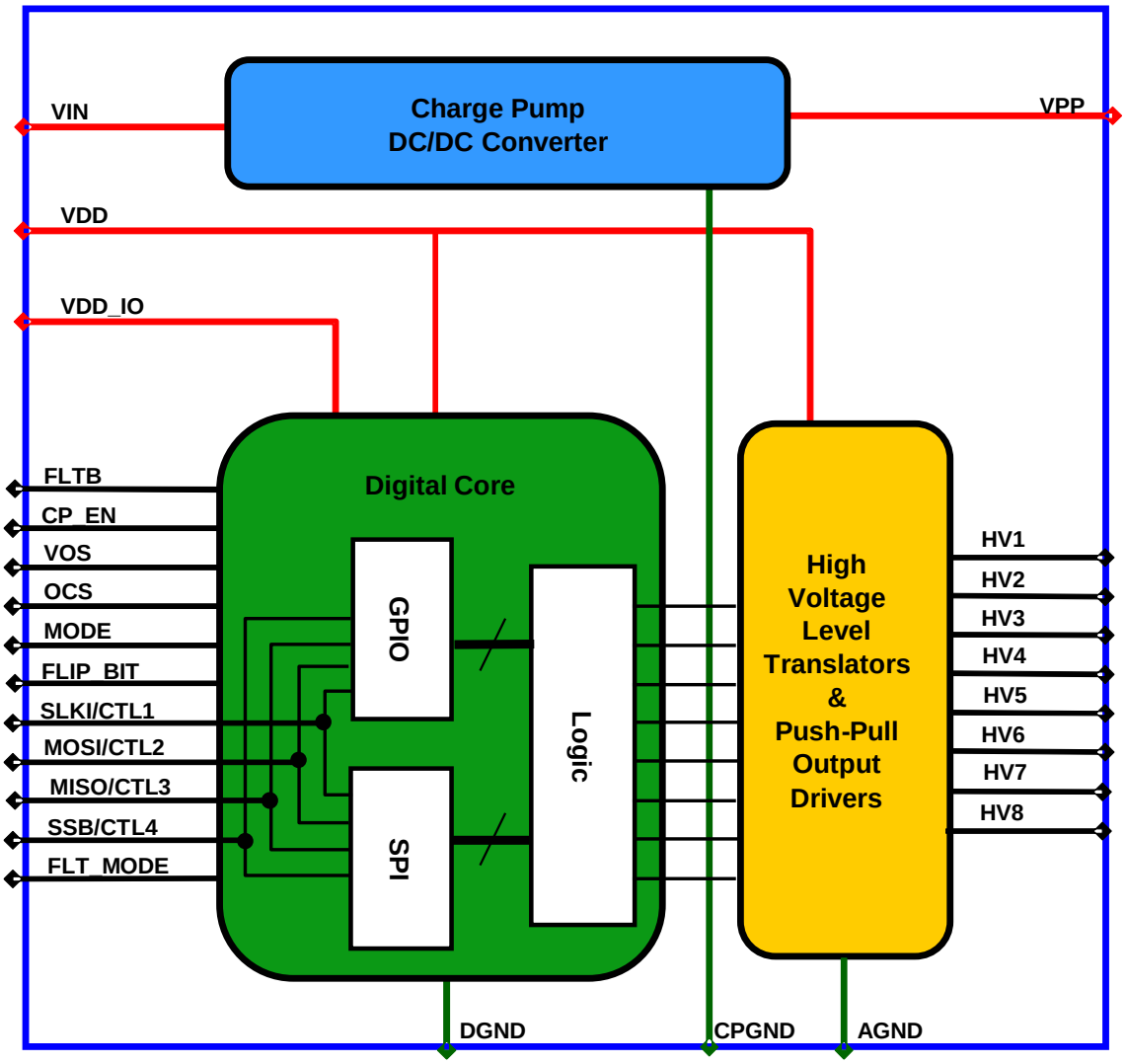


Figure 2: Functional Block Diagram

32-Lead QFN Package Pinout

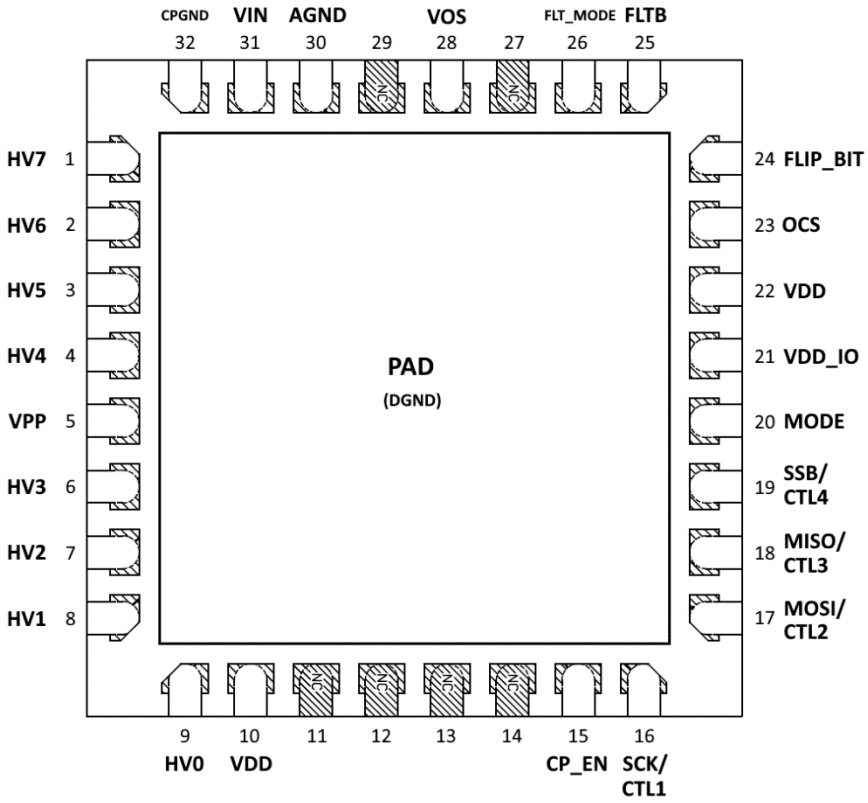


Figure 3: MM101 5 mm x 5 mm QFN package pinout (Top View/As Mounted)

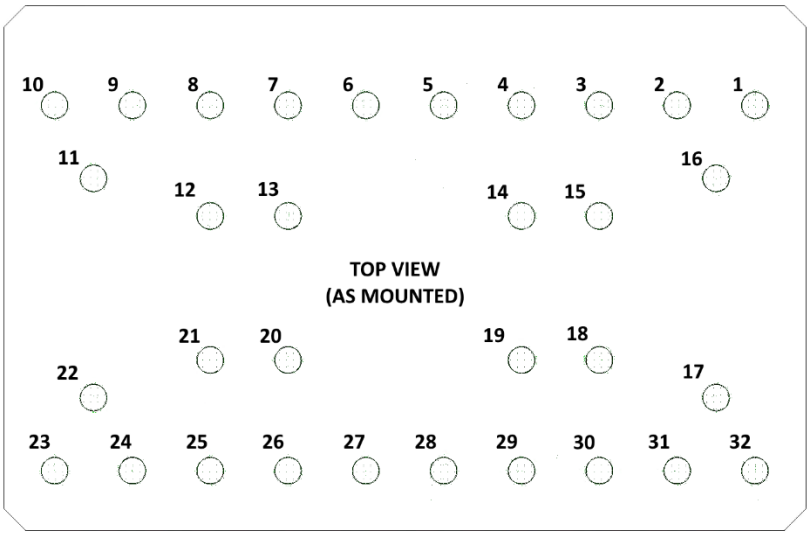


Figure 4: MM101 2.37 mm x 1.58 mm Flip-Chip package pinout (Top View/As Mounted)

Table 7 Detailed Pin Description

QFN Pin #	Flip Chip Pin #	Name	Description
1-4, 6-9	**2-9**	HV#	High voltage outputs.
5	**14, 15**	VPP	High-voltage input to the output drivers. Bypass with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor, to the CPGND pin.
10, 22	**1, 20, 21**	VDD	3.3 V supply to digital/analog circuits. Bypass with a low ESR 1 µF ceramic capacitor.
11-14, 27, 29	**32**	NC	No Connect
15	**17**	CP_EN	Charge pump enable pin in GPIO mode. Pull-up to VDD_IO to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
16	**31**	SCK/CTL1	Clock input in SPI mode; HV output control in GPIO mode. Has an internal pull-down resistor.
17	**30**	MOSI/CTL2	SPI data input in SPI mode; HV output control in GPIO mode. Has an internal pull-down resistor.
18	**16**	MISO/CTL3	SPI data output in SPI mode; HV output control in GPIO mode. Has an internal pull-down resistor.
19	**29**	SSB/CTL4	Chip select in SPI mode; HV output control in GPIO mode. Has an internal pull-up resistor to VDD_IO in SPI mode, and an internal pull-down resistor in GPIO mode.
20	**28**	MODE	Logic level input to switch inputs between SPI and GPIO modes. Connect to GND for SPI mode. Connect to VDD_IO for GPIO mode.
21	**27**	VDD_IO	For 3.3 V nominal digital I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). Bypass with a low ESR 1 µF ceramic capacitor if separate from VDD.
23	**26**	OCS	Output Current Select in GPIO mode. Connect to VDD_IO for high level or GND for low level. Has an internal pull-down resistor. Pin is ignored in SPI mode.

QFN Pin #	Flip Chip Pin #	Name	Description
24	**12, 13**	FLIP_BIT	In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and HV0-7. Refer to Table 8. Set high in SPI mode.
25	**25**	FLTB	Fault indicator in GPIO and SPI modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when fault is detected. Can be left open if not used. Pull-up voltage must be ≤ VDD_IO.
26	**22**	FLT_MODE	Fault Mode select in GPIO mode. Pull to VDD_IO to disable Fault Mode. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
28	**23**	VOS	Output voltage select in GPIO mode. Connect to VDD_IO for high level or GND for low level. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
30	**24**	AGND	Analog ground, should be connected to PCB ground.
31	**10**	VIN	Connect to 5 V power supply. Bypass with a low ESR 1 µF ceramic capacitor. When using external VPP supply (i.e. not using the internal charge pump), connect VIN to CPGND.
32	**11**	CPGND	Charge pump ground, should be connected to PCB ground.
PAD	**18, 19**	DGND	Digital ground, should be connected to PCB ground.

Functional Description

The MM101 is an 8-Channel Low-Voltage Serial to High-Voltage Parallel Converter with Push-Pull Outputs and an Internal Charge Pump Converter. The device is designed for MEMS applications where high voltage generation and driving capability are desired in a high integration form factor.

The device consists of three main design blocks: Internal Charge Pump, Communication Interface, and 8-High Voltage Push-Pull Drivers.

Charge Pump

The Internal Charge Pump operates from a 5.0V nominal input to generate the high voltage VPP for the HV Drivers. The output voltage can be selected to be either 90V or 80V using the VOS pin in GPIO mode or VOSET bit in SPI mode.

The VOS pin has a low current internal pull-down to GND. If the pin is left open or connected to VDD, the output volt-age defaults to 80 V. Pulling the pin to VDD_IO sets the output high level to 90V. Likewise, in SPI mode, if the VOSET register bit is zero, the output level (HV#) high levels are 80V. If VOSET is set to 1, the HV# output levels are 90V.

The charge pump is designed to simultaneously drive 8 High-Voltage Push-Pull Drivers with a total load capacitance of 10pF.

Supplying an External High Voltage

If it is desired to use an external voltage instead of a charge pump:

- VIN should be connected to CPGND.
- VPP should be applied 0.1msec or more after VDD is applied.
- VOS pin should be set according to the VPP voltage that will be applied externally (80V/90V). This will ensure that the internal VPP under-voltage comparators function correctly.
- When using an external supply to drive VPP in GPIO mode, the status of the CP_EN pin affects VPP under voltage faults.

High Voltage Outputs

The eight, high-voltage outputs are powered from VPP and controlled by the digital inputs.

In SPI mode, the output current may be set to either the low level or high level by using the OCS register bit. The default state of OCS is a logic zero, which sets the output

current level to low. In GPIO mode, the output current level is determined by the state of the OCS pin.

Programming

Communication Interface

The driver interface two modes of operation; **Serial** and **GPIO (Parallel)**, selected by the **MODE** input pin.[1]

All the SPI pins (except SSB pin), the FLIP_BIT and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float.
The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is VIN4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

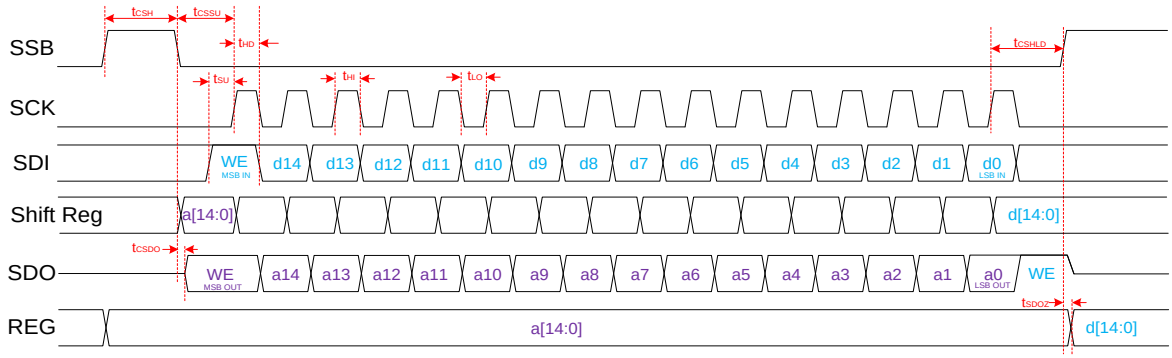


Figure 4: SPI Timing Diagram

Serial Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. (See Daisy Chain Operation figures 7 to 9)
The SPI works at any frequency up to a maximum of 33 MHz and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

[1] If MODE is toggled from GPIO to SPI, it is a good practice to pulse SSB low before the first 16-bit transaction. This will reset the SPI and ensure that it is ready to receive the first data packet.

SPI Interface Mode

SPI timing diagrams are provided in Figures 4 to 9. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data (D_N) to Target, while Target passes its previous (D_N-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

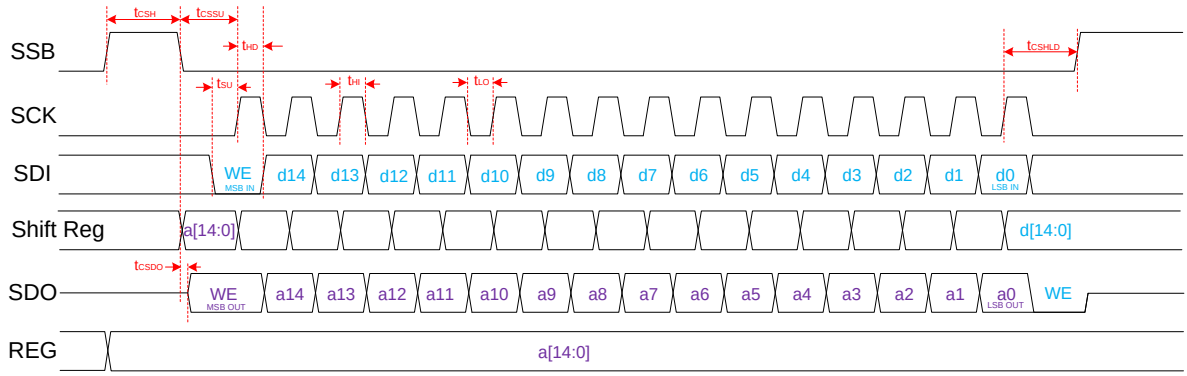


Figure 5: SPI Read Only (1 IC, No Daisy Chain)

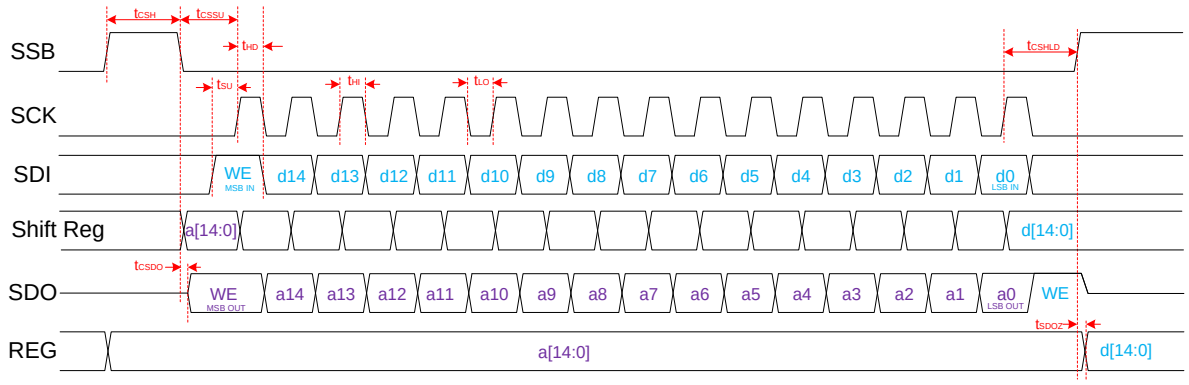


Figure 6: SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the SDO pin while clocking the SCK pin. Register STATE holds the state of the 8 high-voltage outputs and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high.

Register CONTROL holds six control bits (OCSET, CPEN, VOSET, VPPCOMP, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high.
In SPI mode, the OCS, VOS, CP_EN and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

STATE REGISTER

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
HV7	HV6	HV5	HV4	HV3	HV2	HV1	HV0
bit 7							bit 0

bit 7: **HV7**
1 = HV7 Output is Enabled (High)
0 = HV7 Output is Disabled (Low)
bit 6: **HV6**
1 = HV6 Output is Enabled (High)

0 = HV6 Output is Disabled (Low)

bit 5: **HV5**
1 = HV5 Output is Enabled (High)
0 = HV5 Output is Disabled (Low)

bit 4: **HV4**
1 = HV4 Output is Enabled (High)
0 = HV4 Output is Disabled (Low)

bit 3: **HV3**
1 = HV3 Output is Enabled (High)
0 = HV3 Output is Disabled (Low)

bit 2: **HV2**
1 = HV2 Output is Enabled (High)
0 = HV2 Output is Disabled (Low)

bit 1: **HV1**
1 = HV1 Output is Enabled (High)
0 = HV1 Output is Disabled (Low)

bit 0: **HV0**
1 = HV0 Output is Enabled (High)
0 = HV0 Output is Disabled (Low)

CONTROL REGISTER

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	VOSET	CPEN	OCSET
bit7							bit 0

bit 7: **WR_EN**
1 = Enable write mode
0 = Disable Write mode (read only)
bit 6: **FSTAT**[2]
1 = VPP OR VDD Fault status = faulted
0 = VPP OR VDD Fault status = NOT faulted
bit 5: **SLEEP**[3]
1 = SLEEP mode active (all analog circuits disabled)
0 = SLEEP mode inactive (all analog circuits enabled)
bit 4: **FLTMODE**
1 = Fault Mode Disabled (shutdown Disabled)
0 = Fault Mode Enabled (shutdown Enabled)
bit 3: **VPPCOMP**
1 = VPP under-voltage comparator is disabled
0 = VPP under-voltage comparator is active
bit 2: **VOSET**
1 = VPP is set to its high level
0 = VPP is set to its low level
bit 1: **CPEN**
1 = Charge Pump is enabled
0 = Charge Pump is disabled
bit 0: **OCSET**
1 = Output current is set to its high level
0 = Output current is set to its low level

[2] VPP and VDD faults are latched. Once this bit is set high, it must be written to 0 to clear the fault.
[3] The SLEEP bit is forced low in GPIO mode.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the SDO of one chip to the SDIN of the next chip in the chain, as shown in Figure 7. SPI timing diagrams with daisy-chained devices are provided in Figure 8 and Figure 9.

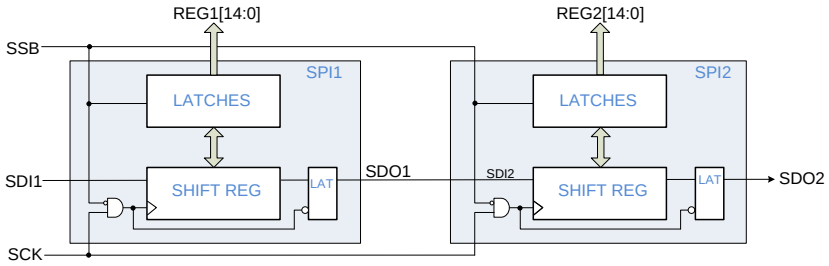


Figure 7: SPI with 2 ICs Daisy-chained

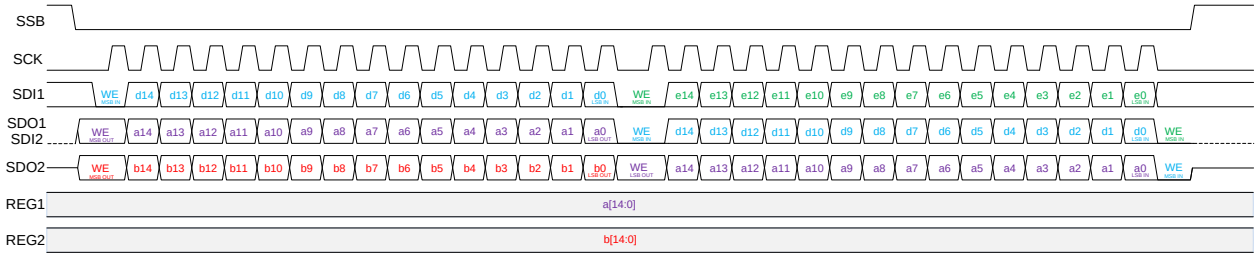


Figure 8: SPI Read Only (2 ICs Daisy-chained)

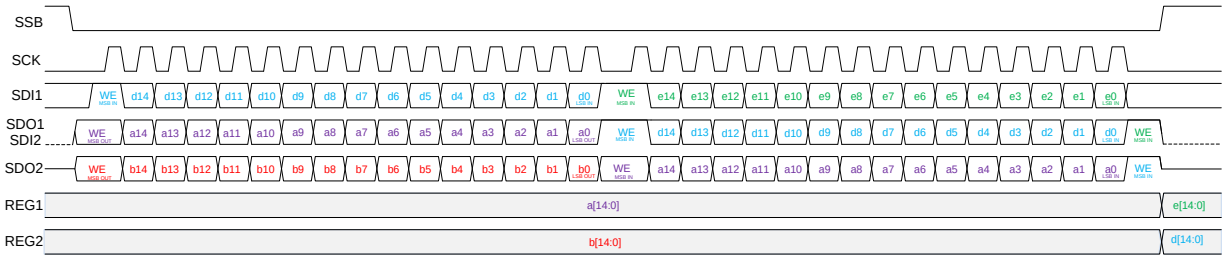


Figure 9: SPI Read & Write (2 ICs Daisy-chained)

GPIO Communication

MODE = 1 activates the GPIO (General Purpose Input Output or Parallel Mode) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs, as described in the Detailed Pin Description.

Table 8 HV# State Table in GPIO mode

Count	Input Signals					HV							
	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	7	6	5	4	3	2	1	0
0	1	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
2	1	0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
3	1	0	0	1	1	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
4	1	0	1	0	0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
5	1	0	1	0	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
6	1	0	1	1	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
8	1	1	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9	1	1	0	0	1	ON	OFF	ON	OFF	ON	OFF	OFF	ON
10	1	1	0	1	0	ON	OFF	ON	OFF	OFF	ON	ON	OFF
11	1	1	0	1	1	ON	OFF	OFF	ON	ON	OFF	ON	OFF
12	1	1	1	0	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF
13	1	1	1	0	1	ON	OFF	ON	OFF	ON	OFF	ON	OFF
14	1	1	1	1	0	OFF	ON	OFF	ON	OFF	ON	OFF	ON
15	1	1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
16	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
17	0	0	0	0	1	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
18	0	0	0	1	0	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
19	0	0	0	1	1	ON	ON	OFF	OFF	OFF	OFF	ON	ON
20	0	0	1	0	0	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
21	0	0	1	0	1	ON	OFF	ON	OFF	OFF	ON	OFF	ON
22	0	0	1	1	0	OFF	ON	ON	OFF	OFF	ON	ON	OFF
23	0	0	1	1	1	ON	ON	ON	OFF	OFF	ON	ON	ON
24	0	1	0	0	0	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
25	0	1	0	0	1	ON	OFF	OFF	ON	ON	OFF	OFF	ON
26	0	1	0	1	0	OFF	ON	OFF	ON	ON	OFF	ON	OFF
27	0	1	0	1	1	ON	ON	OFF	ON	ON	OFF	ON	ON
28	0	1	1	0	0	OFF	OFF	ON	ON	ON	ON	OFF	OFF
29	0	1	1	0	1	ON	OFF	ON	ON	ON	ON	OFF	ON
30	0	1	1	1	0	OFF	ON	ON	ON	ON	ON	ON	OFF
31	0	1	1	1	1	ON	ON	ON	ON	ON	ON	ON	ON

Fault Conditions

There are two comparators[4] that can signal a fault condition - VDD under voltage fault and VPP under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO. The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than $UVLO_{RISE}$ and VPP goes higher than V_{EN}). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below $UVLO_{FALL}$ or VPP goes below VPP_{DIS}, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared – the FSTAT bit remains latched high until it is cleared via a SPI write. If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the outputs are all set low and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to re-start the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

[4] The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP_EN pin is set low.

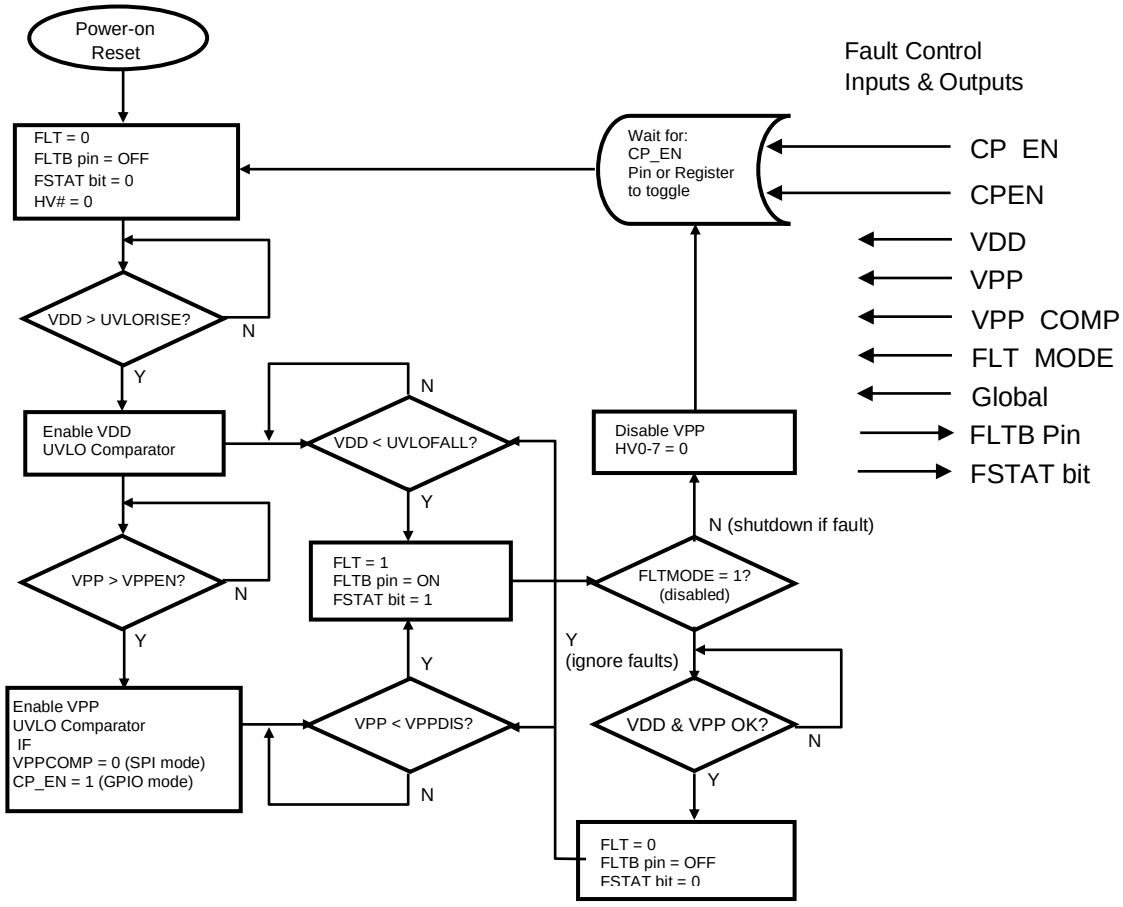


Figure 3: Flowchart for Fault

Notes:

1) The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2) VDD_IO is not monitored unless it is connected to VDD.
3) VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP_EN pin is low In GPIO mode.

External Circuitry

The MM101 internal driver requires external circuitry to operate its charge pump. The diagram below shows the suggested bypass capacitors that have been used with good results. Menlo Micro recommends selecting components with equal or better performance.

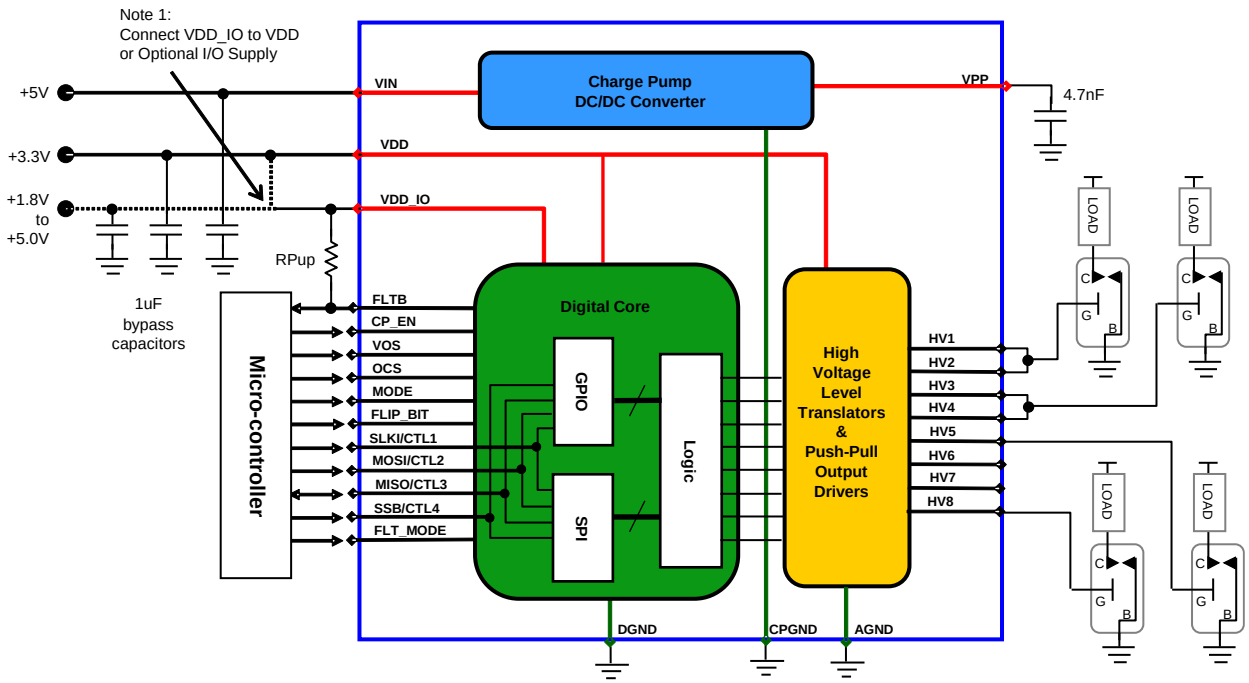
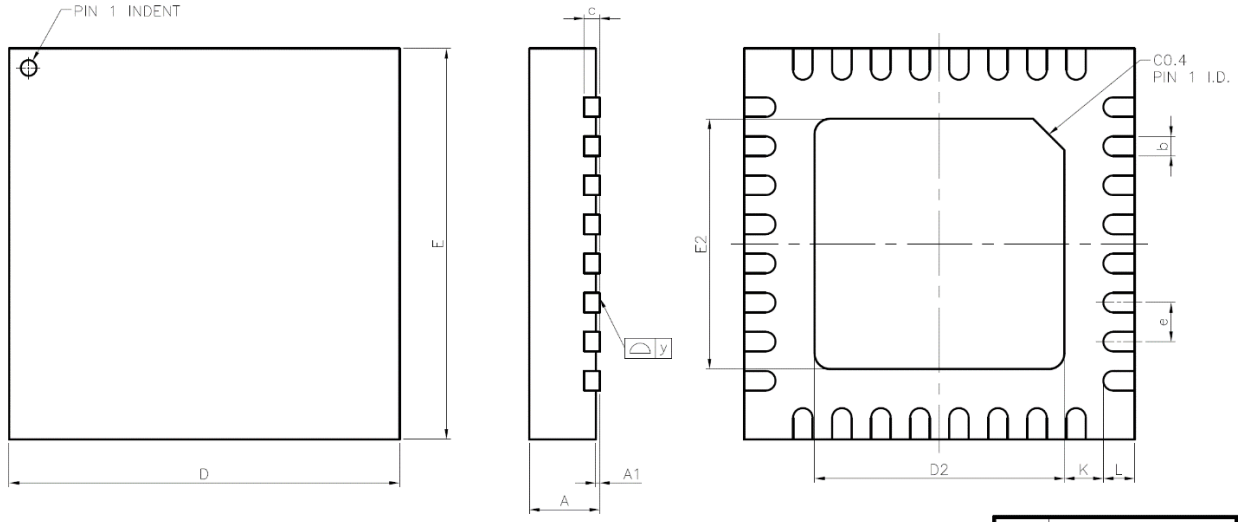


Figure 10: MM101 Application Diagram

QFN Package Drawing

The 5 mm x 5 mm 32P QFN package drawing is below.



NOTE:

1.THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.20 REF.	---
D	4.90	5.00	5.10
D2	3.15	3.20	3.25
E	4.90	5.00	5.10
E2	3.15	3.20	3.25
e	---	0.50	---
K	---	0.50	---
L	0.35	0.40	0.45
y	0.00	---	0.075

Figure 11 QFN Package Drawing

Flip Chip Package Drawing

The 2.37 mm x 1.58 mm **WLCSP** Flip Chip package drawing is below.

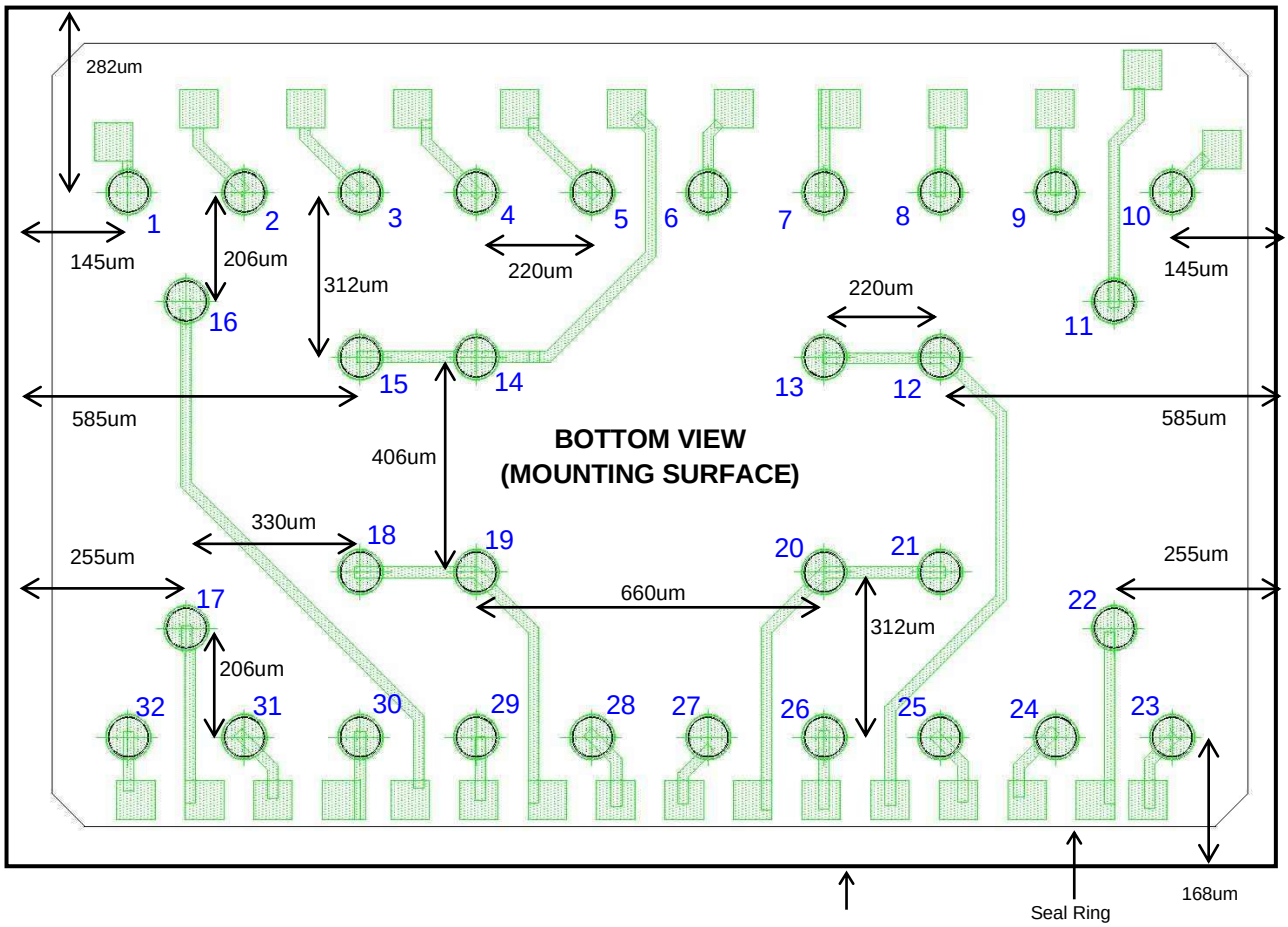


Table 9 Flip-chip SOLDER BALL locations

Ball #	Signal Name	X (um)	Y (um)		Ball #	Signal Name	X (um)	Y (um)		Ball #	Signal Name	X (um)	Y (um)
1	VDD	-990	458		12	FLIP_BIT	550	146		23	NC	990	-572
2	HV0	-770	458		13	FLIP_BIT	330	146		24	AGND	770	-572
3	HV1	-550	458		14	VPP	-330	146		25	FLTB	550	-572
4	HV2	-330	458		15	VPP	-550	146		26	NC	330	-572
5	HV3	-110	458		16	MISO / CTL3	-880	252		27	VDD_IO	110	-572
6	HV4	110	458		17	CP_EN	-880	-366		28	MODE	-110	-572
7	HV5	330	458		18	DGND	-550	-260		29	SSB / CTL4	-330	-572
8	HV6	550	458		19	DGND	-330	-260		30	MOSI / CTL2	-550	-572
9	HV7	770	458		20	VDD	330	-260		31	SCK / CTL1	-770	-572
10	VIN	990	458		21	VDD	550	-260		32	NC	-990	-572
11	CPGND	880	252		22	FLT_MODE	880	-366		-	-	-	-

X-Y position = Ball center with respect to Die Center
Bump Diameter = 100um to 105um
Bump Height = 80um

Figure 12 Solder Balls Drawing

Recommended Solder Reflow Profile

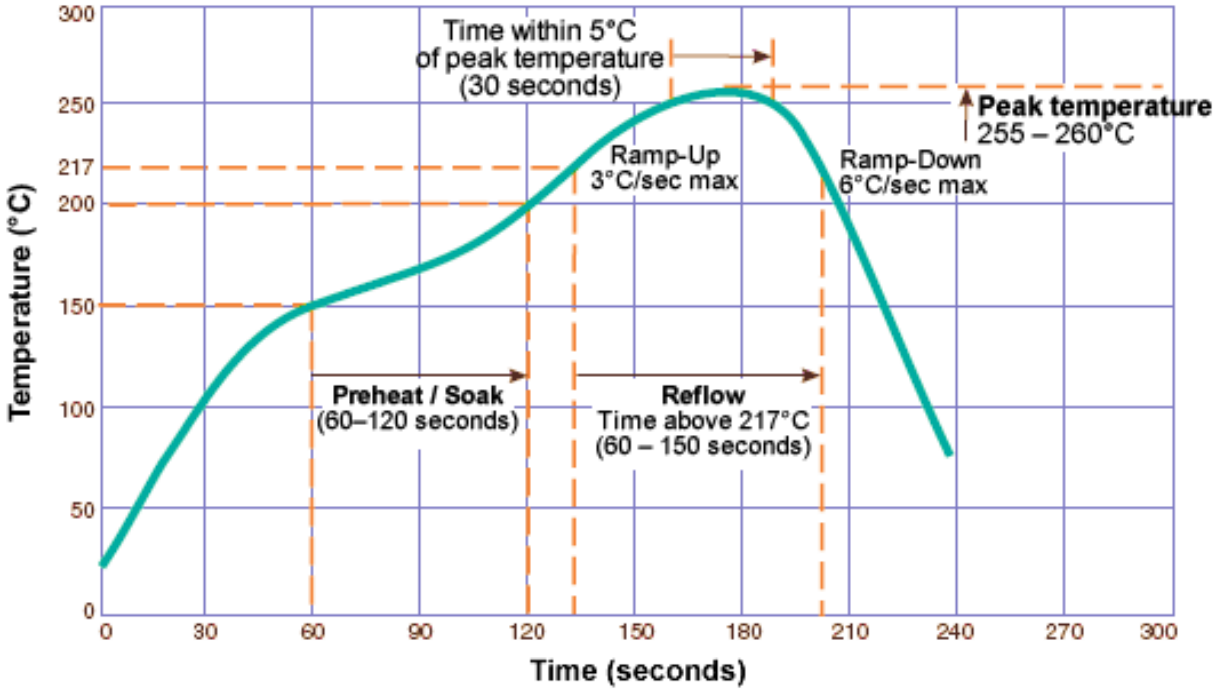


Figure 13: Reflow Profile

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 32 months or less.

Package Options and Ordering Information

Ordering Information

Part Number	ECCN	Package	Temp Range
MM101-02	EAR99	5.0 mm x 5.0 mm 32P QFN	-55°C to +125°C
MM101-03	EAR99	2.37 mm x 1.58 mm 32P WLCSP	-55°C to +125°C
MM101EVK	EAR99	USB Driver Board with MM101	

Important Information

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