MM1200

6 Channel SPST Signal Relay

POWERED BY ideal switch®

RoHS COMPLIANT

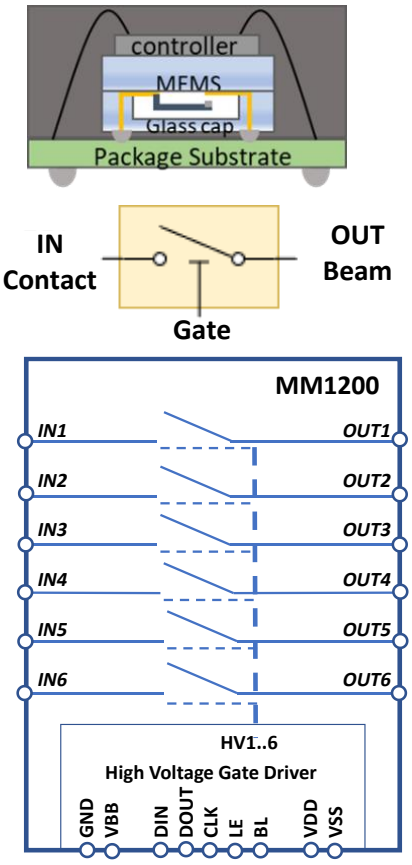
Product Overview

Description

The MM1200 device is a 6-channel SPST Signal Relay intended for signal switching applications in both DC and AC circuits. Each channel provides low on-state contact resistance, high off-state isolation, and industry-leading cycle life. Gate drivers and control logic are provided internally. Each channel can be individually controlled by the serial-to-parallel interface. The flexibility of six SPST channels enables implementation of different signal topologies such as dual SP3T, triple SP2T, or 2 x 3 matrix.

Features

- 1.0A per channel and 2.0A per package.
- Input to Output Isolation > 10GΩ typical.
- Low On-State Resistance 1.0Ω typical per channel.
- Standoff Voltage > 100V across input to output.
- Switching Time 8.5µs typical.
- High Reliability > 3 Billion Switching Operations.
- Integrated driver eliminates need for external gate driver.
- 6mm x 6mm BGA Package.



Applications

- High-Density Switch Matrices
- Automated Test and Measurement Systems
- Mechanical Relay Replacement

Markets

- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1200 should be restricted to the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM1200 is a Class 0 ESD device. When handling the MM1200, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1.

Power Sequencing

The following power sequence is recommended:

- Power-Up: Apply V_{DD}, set all inputs to known state with no signal on switches, apply V_{BB}.
- Power-Down: Power off signal on switches, remove V_{BB}, remove all inputs, remove V_{DD}.

The high-voltage supply (V_{BB}) may be applied and removed as required when V_{DD} is present. V_{BB} should not be allowed to float during operation or create a hot switch event.

Table 1. Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (V_{DD})	—	7.5	V_{DC}
High-Voltage Gate Supply (V_{BB})	—	90	V_{DC}
Driver Logic Input Levels	-0.3	V_{DD}+0.3	V
Off-State Voltage INx to OUTx[2]	-100	100	V
On-State DC Carry Voltage[3]	0	13	V_{DC}
Off-State Output Voltage to GND[4]	0	50	V_{DC}
AC/DC Carry Current per Channel[5]	—	1.0	A
Total Carry Current Across All Channels[5]	—	2.0	A
Storage Temperature Range[6]	-65	+150	ºC
ESD Rating HBM Driver Pins[7]	—	500	V
ESD Rating HBM Channel I/O Pins[8 9]	—	100	V
Mechanical Shock[10]	—	500	G
Vibration[11]	—	500	Hz

Notes:

1. All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied in the on-state.
2. This also applies to ESD events. This is a Class 0 device.
3. Voltage a given channel can carry above which unintended de-actuation may occur with V_{BB} at 80V.
4. Voltage on the output of a given channel above which unintended actuation may occur.
5. With case temperature ≤ 85°C. See Thermal and Power Handling Considerations for more information.
6. See section Storage and Shelf Life for more information on shelf and floor life.
7. Driver pins include: CLK, LE, DIN, DOUT, BL, V_{BB}, V_{DD}.
8. Channel I/O pins include: IN1 to IN6, OUT1 to OUT6.
9. IN and OUT pins must not be allowed to electrically float during channel operation. See section Floating Node Restrictions for details on avoiding floating nodes.
10. See JESD22-B104 for mechanical shock test methodology at 1.0ms, half-sine, 5 shocks/axis, 6 axis.
11. See JESD22-B103 for vibration test methodology at 3.1G and 30min/cycle, 1 cycle/axis, 3 axis.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Conditions
Driver Logic Supply Voltage	V_{DD}	4.5	5.5	V_{DC}	
High-Voltage Gate Bias	V_{BB}	78	82	V_{DC}	
Operating Temperature Range		-40	+85	ºC	Ambient

Electrical Characteristics

All specifications are valid over full temperature and voltage range unless otherwise noted.

Table 3. DC and AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
On / Off Switching				
Turn on time	—	8.5	16	µs
Turn off time	—	2.5	6	µs
Full Cycle Frequency	—	—	10	kHz
On / Off Channel Operations[1]	3B	—	—	Cycle
On/Off Channel Operations[2] (Hot Switched)				
2V, 28mA	—	810M	—	Cycle
3V, 42mA	—	130M	—	Cycle
4V, 56mA	—	13M	—	Cycle
5V, 70mA	—	1.4M	—	Cycle
Off-State Input-Output Leakage @ 100V	—	470	—	fA
On-State Resistance[3]		1.0	3.0	Ω
Off-State Capacitance (C_{IO})[4]	—	45	—	fF
Channel to Channel Off-State Capacitance (C_{Off})[5]				
In1 – In2	—	40	—	fF
In1 – In6	—	2	—	fF

Notes:

1. Predicted number of operation cycles as observed on a sample size of 75 units, 10kHz cycle rate, and room temperature with Hot Switch Restrictions.
2. Point at which 50% of the population of tested channels failed. Hot switched operations measured at room temperature. See section Switch Reliability Test Results.
3. Measured at 1A, DC.
4. Capacitance between input and output pins measured at 1MHz at room temperature.
5. Capacitance between channel inputs measured at 1MHz at room temperature.

Table 4. Driver DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
High-Voltage Gate Bias V_{BB} Current (I_{BB})	—	—	0.1	mA
Driver Logic Supply V_{DD} Current in standby (I_{DD})	—	10	50	µA
Driver Input (D_{IN}) @ V_{DD}=5.0V				
High-Level Logic Voltage V_{IH}	3.5	5.0	5.3	V
Low-Logic Input Voltage V_{IL}	-0.3	—	0.8	V
High-Logic Input Current I_{IH}	—	—	1	µA
Driver Output (D_{OUT}) V_{DD}=4.5V				
High-Level Logic Output V_{OH}[1]	4	—	—	V
Low-Level Logic Output V_{OL}[2]	—	—	0.1	V

Notes:

1. V_{OH} measured at ID_{OUT} = +0.1mA.
2. V_{OL} measured at ID_{OUT} = -0.1mA.

Table 5. Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	—	—	5	MHz
Clock Width High and Low t_{WL},t_{WH}	100	—	—	ns
Data Setup Time before Clock Rises t_{SU}	50	—	—	ns
Data Hold Time after Clock Rises t_H	50	—	—	ns
Latch Enable Pulse Width t_{WLE}	100	—	—	ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	50	—	—	ns

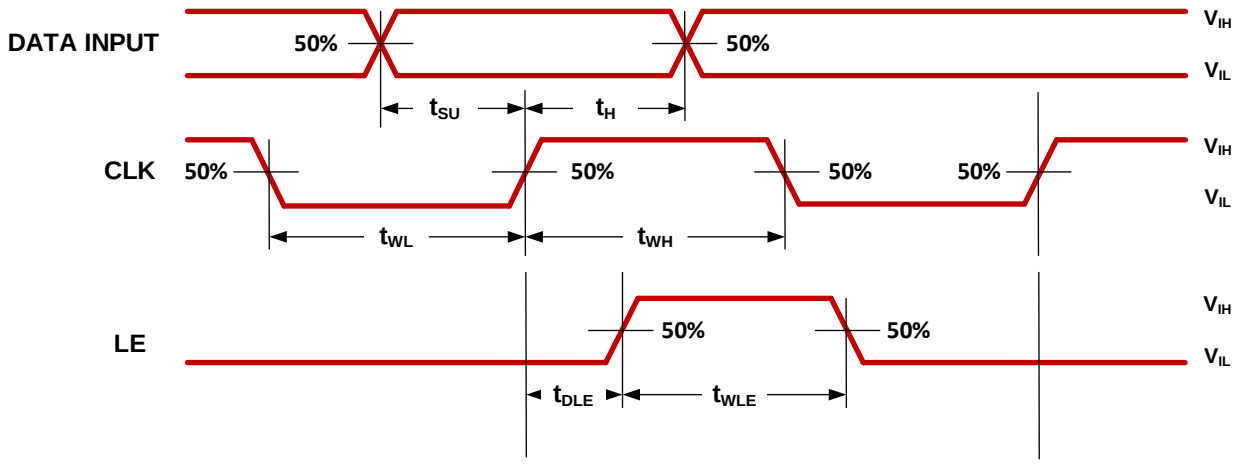
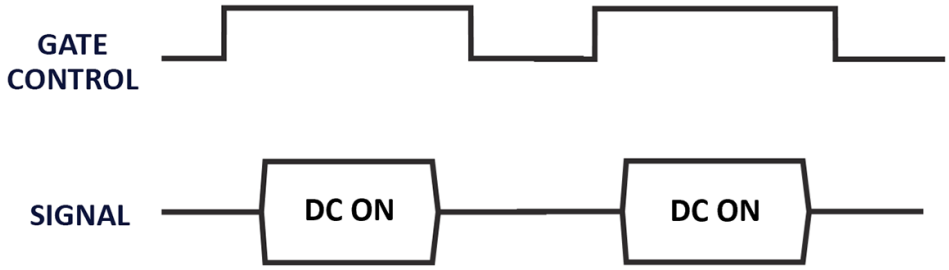


Figure 1. Driver Interface Time Diagram

Hot Switch Restrictions

The MM1200 is not intended for hot switching applications and care should be taken to ensure that switching occurs at less than 0.5V difference between the input and output. In addition, keep the voltage on the output below 6V when closing the switch.



If the MM1200 is used in hot switching applications, the number of cycling operations of the device will be degraded. See section Switch Reliability Test Results and Figure for more information.

Floating Node Restrictions

IN/OUT pins must not be allowed to electrically float during switch operation and therefore require some form of a DC path to ground to prevent charge accumulation. DC paths can be an inductor or high-value resistance that serves as a discharge path. Floating node examples and recommendations include:

- Unused IN/OUT pins: resistively terminate or tie to ground.
- Series capacitance coupling between IN or OUT pins: shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Typical Design Considerations

When using the MM1200, exercise care to maintain certain voltage levels on the switch, depending on its state.

- To avoid **Hot Switching** when opening or closing the switch, the MM1200 Input and Output always need to be within 0.5V of each other. See section Hot Switch Restrictions for more details.
- To avoid **unintended de-actuation** of a closed switch, the voltage on the output can be no greater than the 'On-State DC Carry Voltage'.

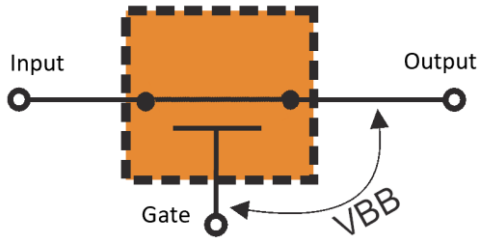


Figure 2. Closed Switch Gate (V_{BB}) to Output Voltage Considerations

- To avoid **unintended actuation** of an open switch, the output must be kept below the 'Off-State Output Voltage to GND'.
- To ensure that the switch is able to actuate, the voltage on the output must be kept below 6V when closing the switch.

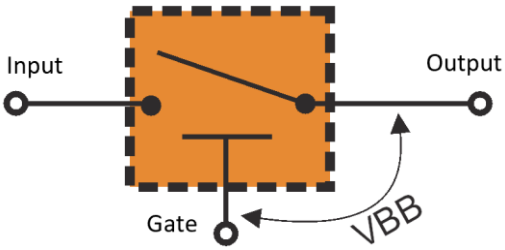


Figure 3. Open Switch Gate (V_{BB}) to Output Voltage Considerations

Thermal and Power Handling Considerations

In high-power operation, the case temperature of the MM1200 should not be allowed to exceed 85˚C. The rise in case temperature can be calculated using the power dissipated by the device and the thermal resistance.

$$\text{Power Dissipated } (P_D) = R_{ON} * I_L^2$$

Using the dissipated powers, the case temperature rise can be calculated.

$$\text{Case Temp Rise} = P_D * \Theta_{CA}$$

Where Θ_{CA}=35˚C/W.

A convenient graph of Case Temperature Rise versus Power Dissipated is shown in Figure 4 below.

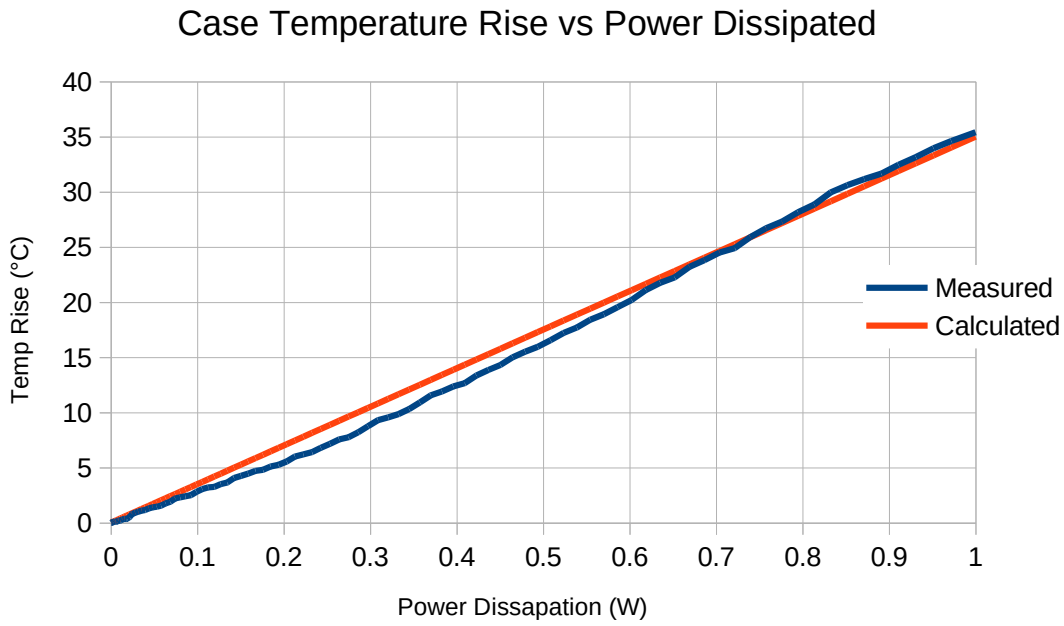


Figure 4. Case Temperature Rise versus Power Dissipated

Functional Block Diagram

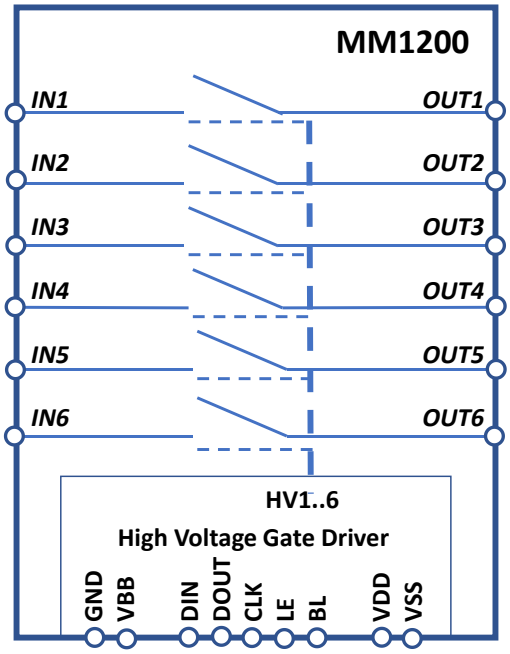


Figure 5. Functional Block Diagram

49-Lead BGA Package Pinout

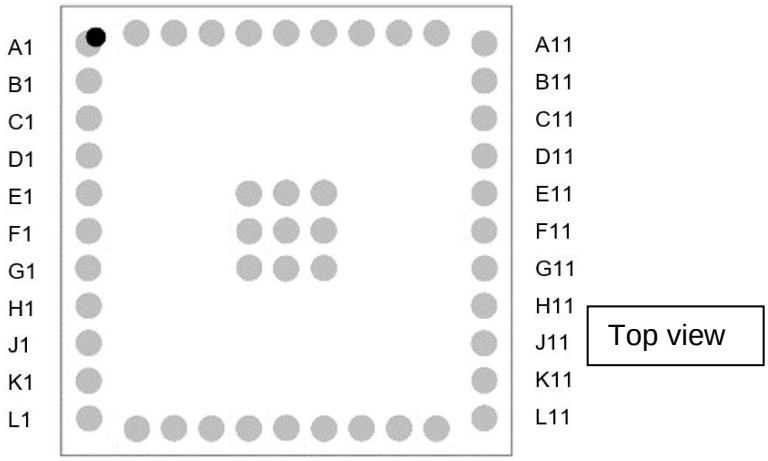


Figure6. Top View Pin Layout

Dot indicates pin 1. See Table 6 for detailed pin description.

Table 6. Detailed Pin Description

Pin Number	Pin Name	Description
GND	A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	Ground Reference, internal shield
VBB	G1	Gate Bias High-Voltage Supply
VDD	F11	Driver Logic Supply
VSS	G11	Supply Voltage Return
IN1	K1	Input (Contact 1)
IN2	L3	Input (Contact 2)
IN3	L5	Input (Contact 3)
IN4	L7	Input (Contact 4)
IN5	L9	Input (Contact 5)
IN6	K11	Input (Contact 6)
OUT1	B1	Output (Beam 1)
OUT2	A3	Output (Beam 2)
OUT3	A5	Output (Beam 3)
OUT4	A7	Output (Beam 4)
OUT5	A9	Output (Beam 5)
OUT6	B11	Output (Beam 6)
DIN	E1	Driver Serial Data Input
DOUT	H1	Driver Serial Data Output
CLK	H11	Driver Clock Input
LE	E11	Driver Latch Input
BL	D1	All Channels Off
N/C	F1, D11	Do Not Connect

EVK Performance

Typical device performance as measured on MM1200EVK evaluation board.

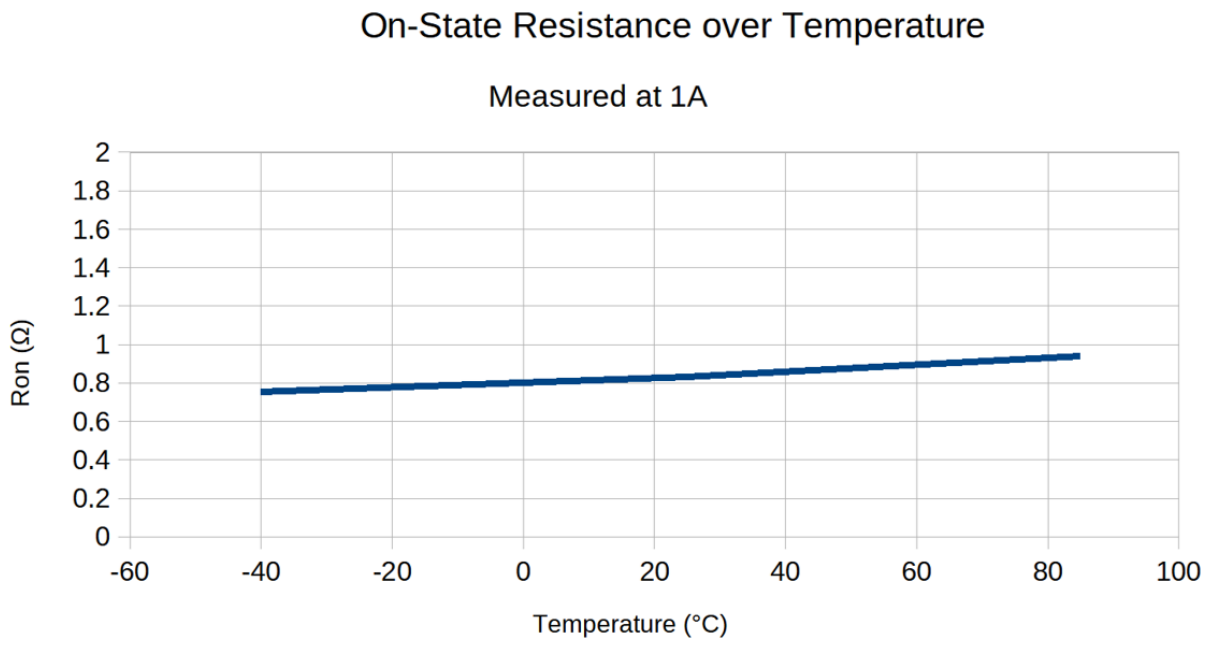


Figure 7. On-State Resistance over Temperature

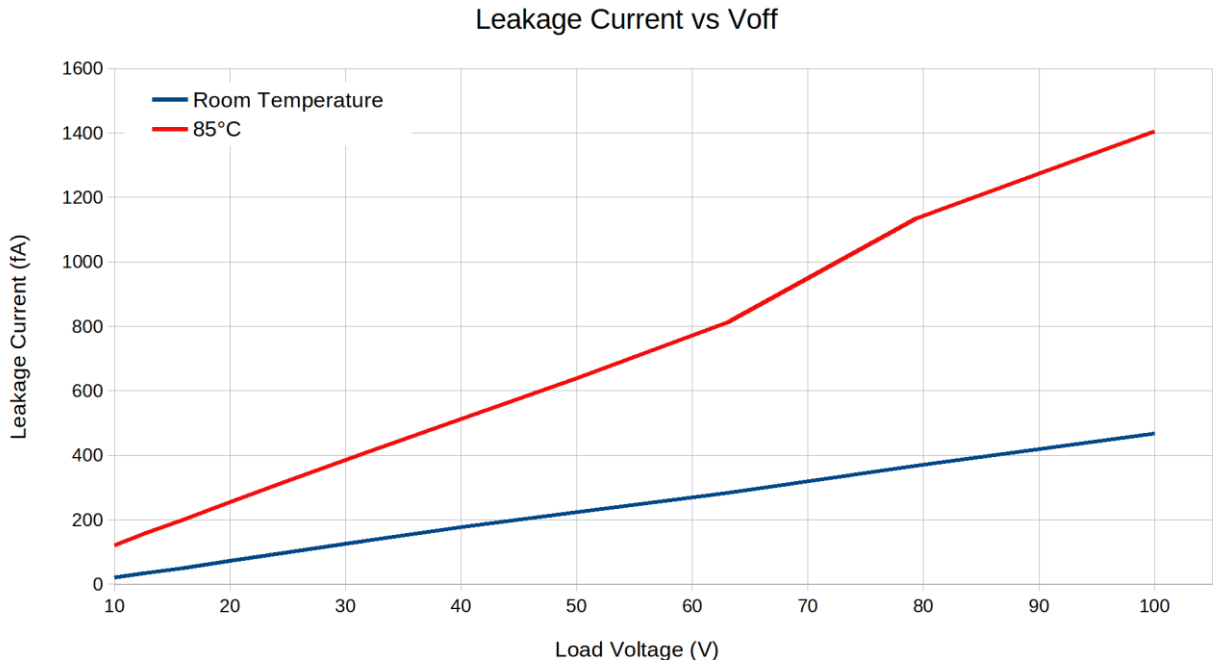


Figure 8. Off-State Input-Output Leakage Current vs V_{off}

Switch Reliability Test Results

Hot switched actuation cycling reliability per channel test results are plotted below with voltage and current varied between 2V, 28mA, and 5V, 70mA.

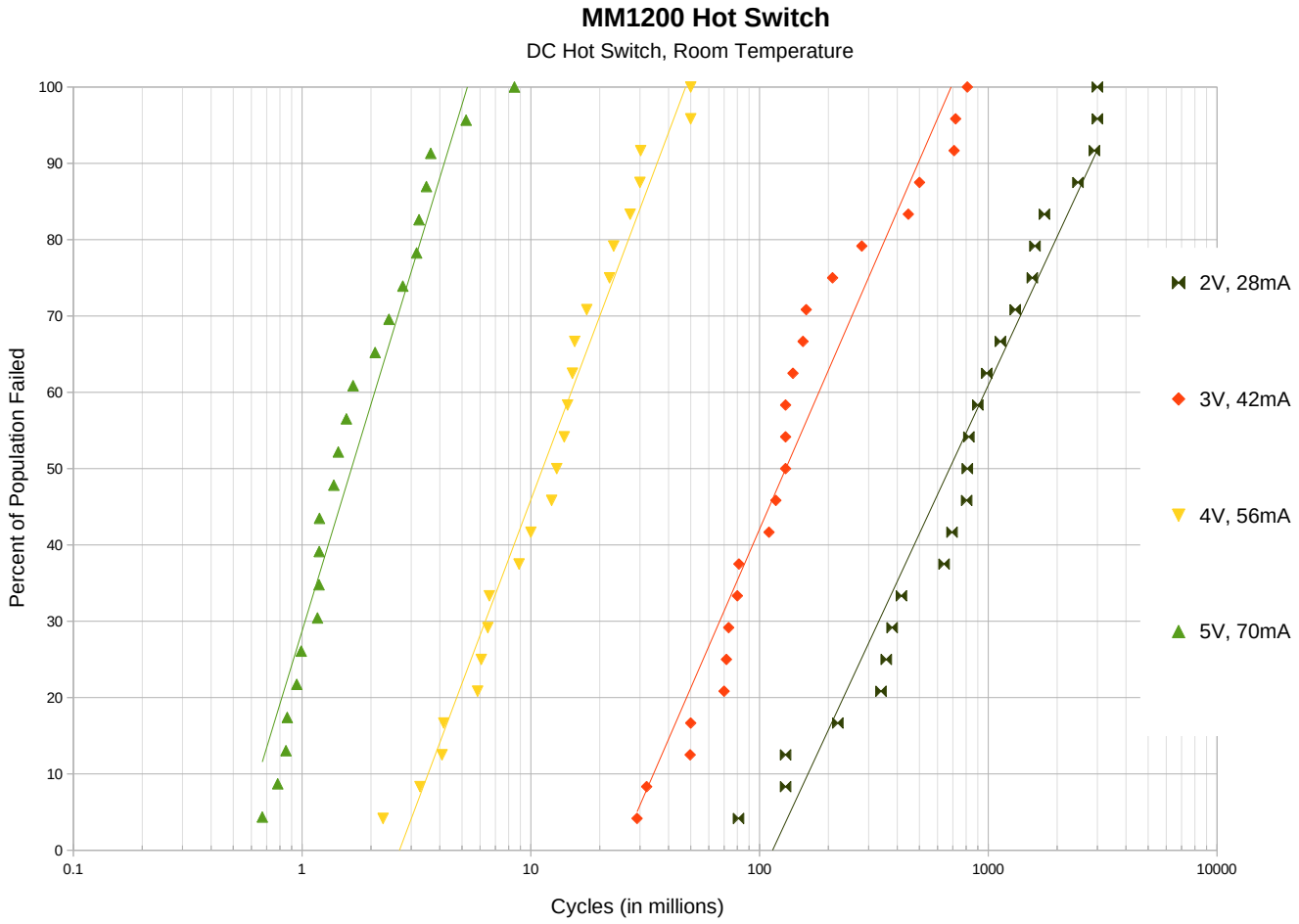


Figure 9. Hot Switch Endurance Test Results

High-Voltage Gate Driver Control

The integrated high-voltage gate driver is controlled through a serial-to-parallel interface that drives the high-voltage gate lines of the channels. Channel control data is shifted into a 10-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure .

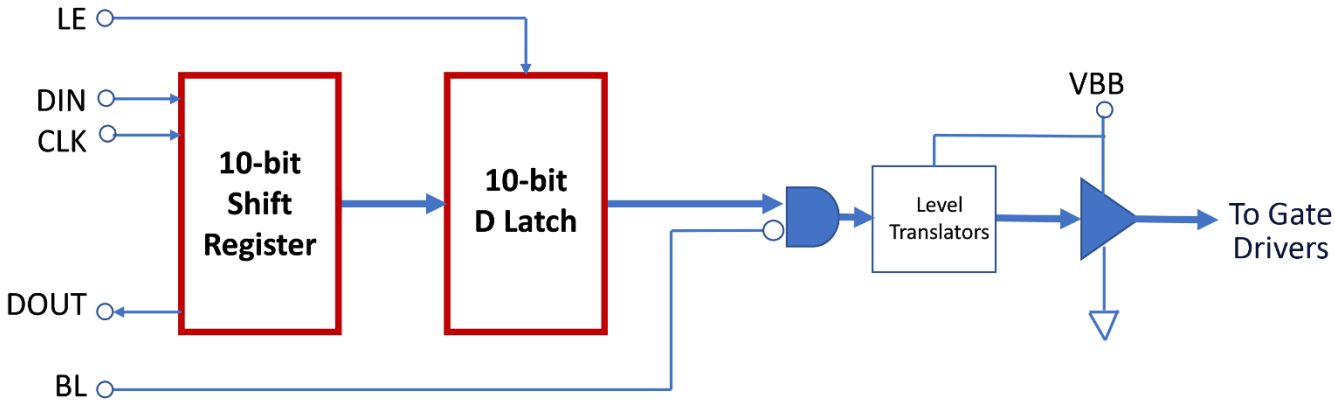


Figure 10: High-Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- A 10-bit data byte is serially loaded into shift register bits 1-to-10 on the positive edge of CLK. Shift order is MSB first starting with bit 10.
- Parallel data from the shift register is transferred to the high-voltage gate output buffers through a 10-bit D latch when the latch enable input LE is logically high. It is recommended that LE be held low while data is being shifted into the register.
- The MM1200 uses only six of the ten data bits latched for channel control. Bits 1 through 6 correspond to high-voltage gate lines HV1 through HV6, respectively. Bits 7, 8, 9, and 10 are unused bits; we recommend you set these to a logical “0”. Data bits set to logical “1” close the corresponding channel to On and “0” open the channel to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case, it is recommended to load 10-bit words consisting of four unused bits and six channel control bits so that each data packet controls one device.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically high. The pin should be logically low for normal operation.

Table 7. Truth Function Table

	Inputs				Shift Register		High-Voltage Output HVx		
Function	**Data**	**CLK**	**LE**	**BL**	**1**	**2 10**	**1**	**2 3**	**10**
All off (blank)	X	X	X	H	*	*…*	L	L L - - - -	L
Load Shift Register	H/L	↑	L	L	H/L	*…*	*	* * - - - -	*
Latched	X	X	L	L	*	*…*	*	* * - - - -	*
Transfer	H/L	X	H	L	H/L	*…*	H/L	* * - - - -	*

Notes:

H = High logic level

L = Low logic level

X = Don't care logic level

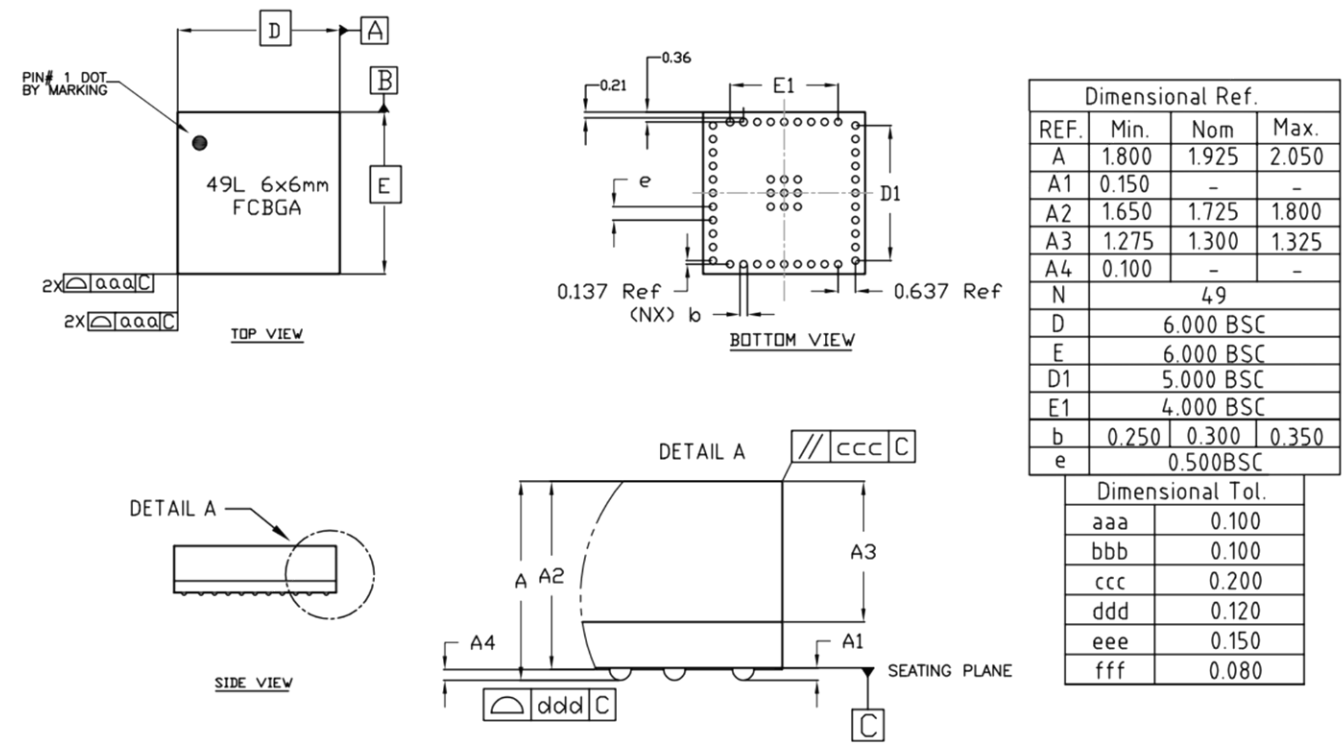
↑ = Low to high logic transition

* = Dependent on the previous stage's state before the last CLK or last LE high

HVx corresponds to high voltage gate drivers where only HV1..6 are used. A high level closes the switch.

Package Drawing

49 Lead Ball Grid Array 0.30mm Ball, 0.50mm Pitch



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.800	1.925	2.050
A1	0.150	-	-
A2	1.650	1.725	1.800
A3	1.275	1.300	1.325
A4	0.100	-	-
N	49		
D	6.000 BSC		
E	6.000 BSC		
D1	5.000 BSC		
E1	4.000 BSC		
b	0.250	0.300	0.350
e	0.500BSC		

Dimensional Tol.	
aaa	0.100
bbb	0.100
ccc	0.200
ddd	0.120
eee	0.150
fff	0.080

Figure 5. Package Drawing

Recommended PCB Layout and SMT Parameters

- PCB pad pattern diagram is shown in Figure 6.
- Connect GND node (floating shield inside the package) to Signal Ground.
- Open space around the package can have grounded thru holes.
- 20 micron (µm) thick solder mask.
- Type 3 or higher solder paste with no clean flux.
- Component placement force not to exceed 100 grams.

Recommended PCB Pad Pattern

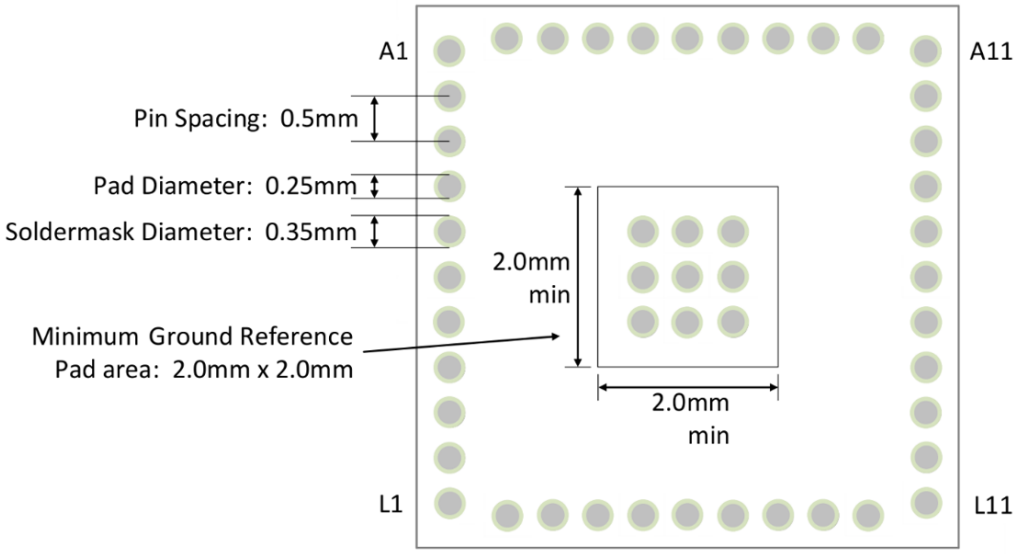


Figure 6. Recommended PCB Pad Pattern

Recommended Solder Reflow Profile

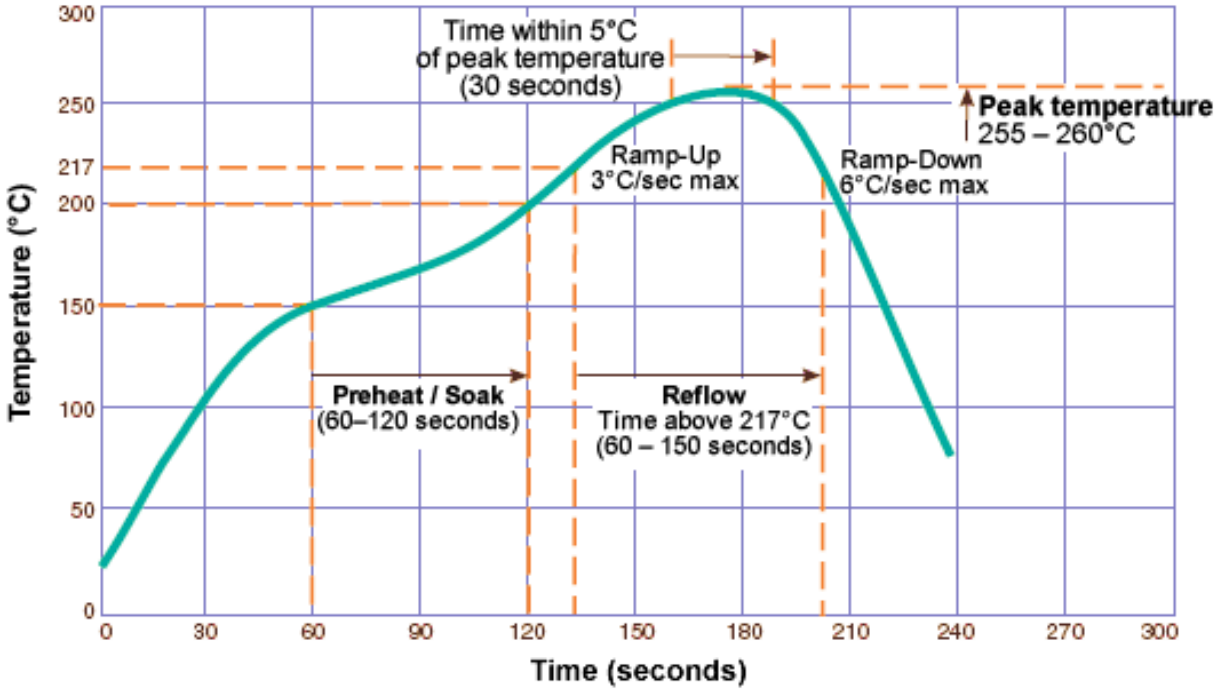


Figure 7. Reflow Profile

Follow MSL-3 (Moisture Sensitivity Level) handling precautions specified in IPC/JEDEC J-STD-020.

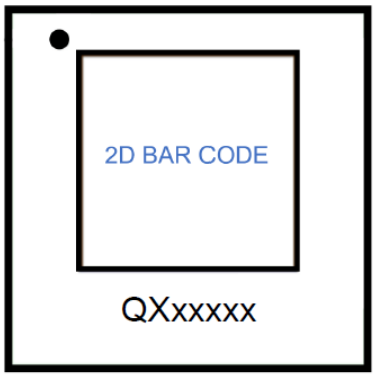
Storage and Shelf Life

Under typical industry storage conditions (≤30°C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date.
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less.

Package Marking Information

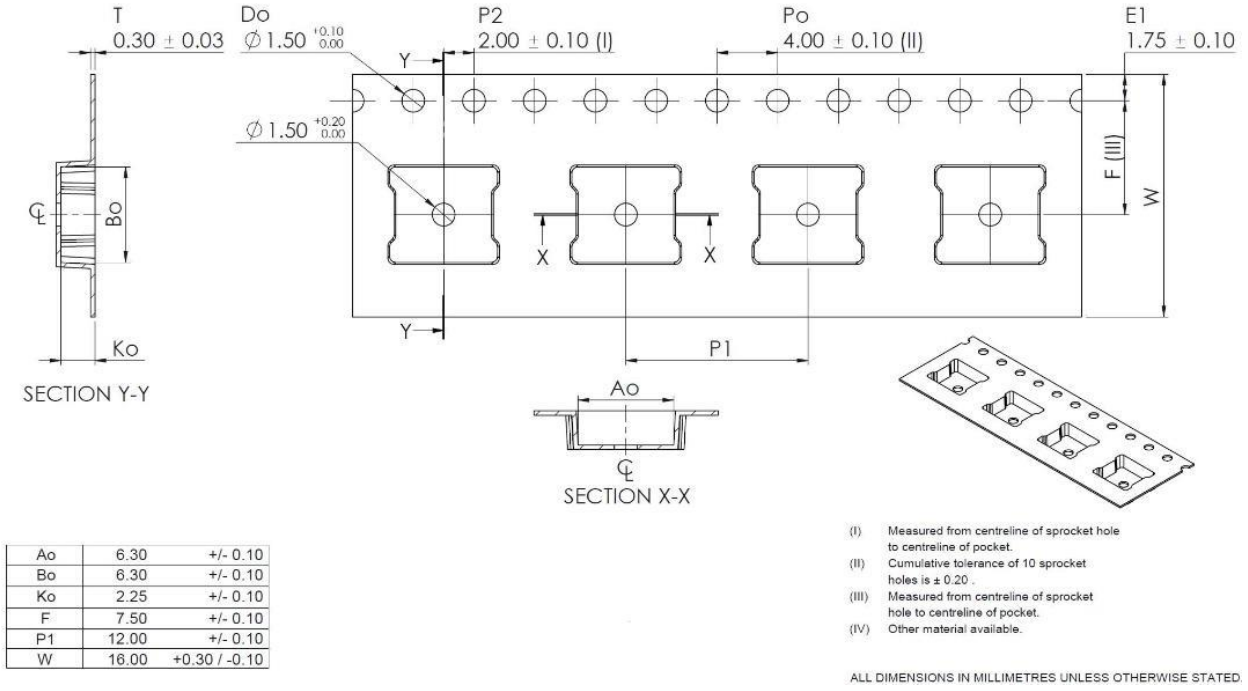
The MM1200 package marking and nomenclature are illustrated in Figure 84.



Dot ● = Pin 1 Indicator

Figure 8. Package Marking Drawing

Package Materials Information



Ao	6.30	+/- 0.10
Bo	6.30	+/- 0.10
Ko	2.25	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.00	+0.30 / -0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 9. Tape and Reel Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package Description	Temp Range	Device Marking[1]
MM1200-00NDB	6xSPST - 6mm x 6mm BGA, Industrial Temp	-40°C to +85°C	QXxxxxx
MM1200-00NDB-TR	6xSPST - 6mm x 6mm BGA, Industrial Temp, Tape and Reel (Qty 250) [2]	-40°C to +85°C	QXxxxxx
MM1200-EVK1	MM1200 Evaluation Board, 6xSPST - 6mm x 6mm BGA		
MM1200-EVK2	4x3 Switch Matrix Reference Design, 6xSPST - 6mm x 6mm BGA		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is a placeholder for a 5-digit numerical code.
2. 250pcs standard tape and reel increment.

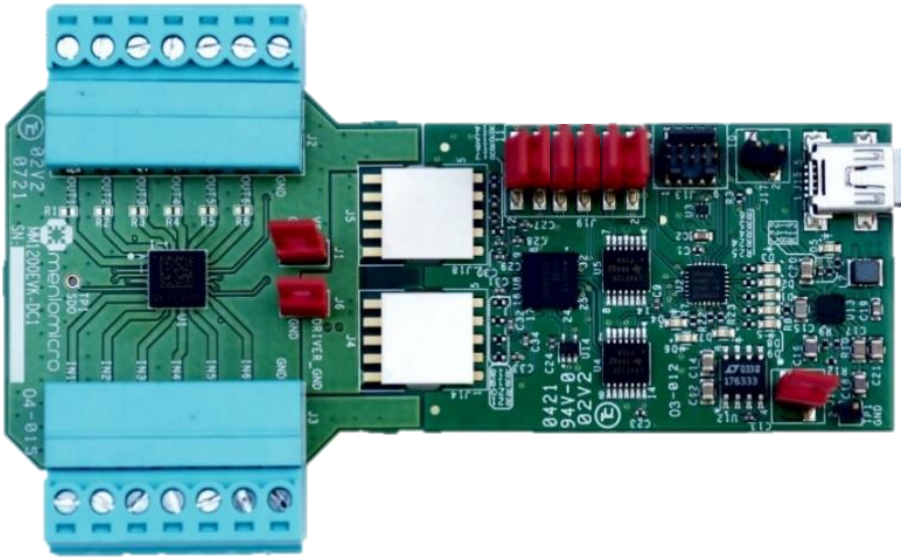


Figure 10. Evaluation Kit 1 (EVK1)

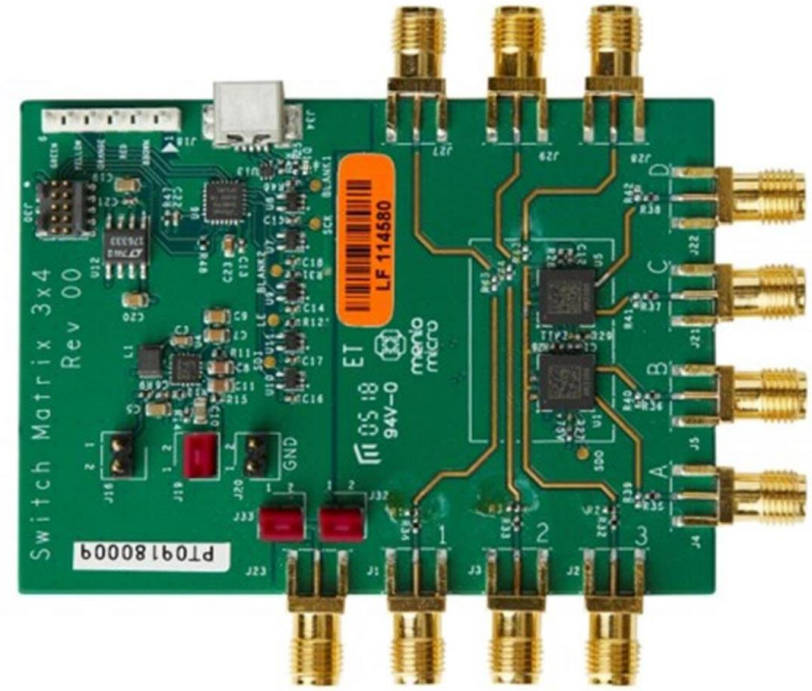


Figure 17. Switch Matrix Reference Design (EVK2)

Important Information

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