MM3100

6 Channel SPST RF Micro Switch

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RoHS COMPLIANT

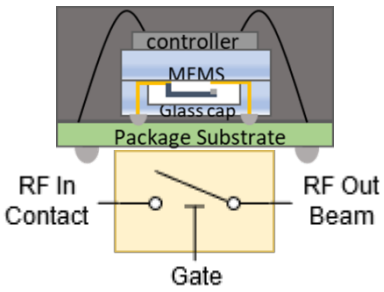
Product Overview

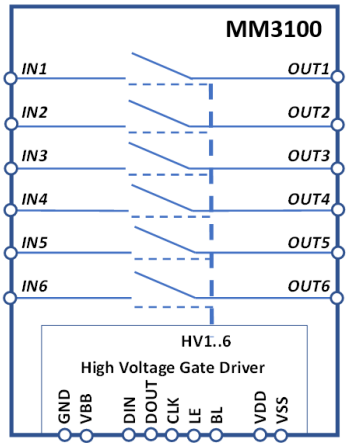
Description

The MM3100 device is a high-power, normally open (NO), six channel Single Pole Single Throw (SPST) micro-mechanical switch for RF and microwave switch applications. The MM3100 is based on Menlo's Ideal Switch® technology and is capable of 25W power transfer. Each channel provides ultra-low on-state insertion loss and high off-state isolation from DC to over 3.0GHz with industry leading cycle life. Gate drivers and control logic are provided internally. Each channel can be individually controlled by the serial-to-parallel interface. The flexibility of six SPST channels enables implementation of different signal topologies such as dual SP3T, triple SP2T, or 2 x 3 matrix.

Features

- DC to over 3.0 GHz Frequency Range.
- 25W (CW) to 300MHz, 200W (Pulsed) Max Power Handling.
- Low On-State Insertion Loss, typical 0.5dB @ 3.0GHz.
- 18dB Isolation @ 3GHz.
- Low On-State Resistance 1.0Ω typical.
- Standoff Voltage > 100V across input to output.
- Switching Time 8.5µs typical.
- High Reliability > 3 Billion Switching Operations.
- Integrated driver eliminates need for an external gate driver.
- 6mm x 6mm BGA Package.





Applications

- High-Power Tunable Resonators and Filters
- Broadband Power Amplifier Impedance Matching
- Electronically Steerable Antennas and Phase Shifters
- Automated Test and Measurement Systems

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM3100 should be restricted to the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM3100 is a Class 0 ESD device. When handling the MM3100, observe precautions as with any other ESD-sensitive device. Do not exceed the voltage ratings specified in Table 1.

Power Sequencing

The following power sequence is recommended:

- Power-Up: Apply V_{DD}, set all inputs to known state with no signal on switches, apply V_{BB}.
- Power-Down: Power off signal on switches, remove V_{BB}, remove all inputs, remove V_{DD}.

The high-voltage supply (V_{BB}) may be applied and removed as required when V_{DD} is present. V_{BB} should not be allowed to float during operation or create a hot switch event.

Table 1. Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (V_{DD})	—	7.5	V_{DC}
High Voltage Gate Supply (V_{BB})	—	90	V_{DC}
Driver Logic Input Levels	-0.3	V_{DD}+0.3	V
Open State Voltage INx to OUTx[2]	-100	100	V
On-State DC Carry Voltage[3]	0	13	V_{DC}
Off-State Output Voltage to GND[4]	0	50	V_{DC}
AC/DC Carry Current per Channel[5]	—	1.0	A
Total Carry Current Across All Channels[5]	—	2.0	A
Storage Temperature Range[6]	-65	+150	°C
ESD Rating HBM Driver Pins[7]	—	500	V
ESD Rating HBM RF I/O Pins[8 9]	—	150	V
Mechanical Shock[10]	—	500	G
Vibration[11]	—	500	Hz

Notes:

1. All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied in the on-state.
2. This also applies to ESD events. This is a Class 0 device.
3. Voltage a given channel can carry above which unintended de-actuation may occur with V_{BB} at 80V.
4. Voltage on the output of a given channel above which unintended actuation may occur.
5. With case temperature ≤ 85°C.
6. See section Storage and Shelf Life for more information on shelf and floor life.
7. Driver pins include: CLK, LE, DIN, DOUT, BL, V_{BB}, V_{DD}.
8. RF I/O pins include: IN1 to IN6, OUT1 to OUT6.
9. RF I/O pins must not be allowed to electrically float during switch operation. See section Floating Node Restrictions for details on avoiding floating nodes.
10. See JESD22-B104 for mechanical shock test methodology at 1.0ms, half-sine, 5 shocks/axis, 6 axis.
11. See JESD22-B103 for vibration test methodology at 3.1G and 30min/cycle, 1 cycle/axis, 3 axis.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Conditions
Driver Logic Supply Voltage	V_{DD}	4.5	5.5	V_{DC}	
High Voltage Gate Bias	V_{BB}	78	82	V_{DC}	
Operating Temperature Range		-40	+85	ºC	Ambient

Electrical Characteristics

All specifications in Table 3 are valid over full V_{BB} range and full operating temperature range with operating frequency range of DC to 3.0GHz.

Table 3. RF Characteristics

Parameter	Minimum	Typical	Max	Unit
CW Power / Channel [1] [2]	—	—	25	W
Peak Power / Channel @ 10% Duty Cycle [3]	—	—	200	W
Insertion Loss @ 3.0GHz	—	0.5	—	dB
Input / Output Return Loss @ 3.0GHz	—	15	—	dB
Input to Output Isolation @ 3.0GHz	—	18	—	dB
Adjacent Channel Isolation @ 3.0GHz [4]				
Both Channels Closed	—	25	—	dB
One Channel Open	—	30	—	dB
Third-Order Output Intercept (IP3)	—	85	—	dBm
Second Harmonic (H2) [5]	—	130	—	dBc
Third Harmonic (H3) [5]	—	140	—	dBc

Notes:

1. Maximum allowable Continuous Wave Power below 2.0MHz is 1.0W.
2. 25W maximum @ 300MHz. See section Thermal and Power Handling Considerations for maximum power vs frequency.
3. Duty Cycle based on 10µs period.
4. See section Adjacent Channel Isolation for more information regarding isolation measurements.
5. Measured at 2.0GHz fundamental frequency and 35dBm input power.

All specifications are valid over full temperature and voltage range unless otherwise noted.

Table 4. DC and AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
On / Off Switching and Settling Time[1]				
Turn on time	—	8.5	16	µs
Turn off time	—	2.5	6	µs
Full Cycle Frequency	—	—	10	kHz
On/Off Channel Operations[2]	3B	—	—	Cycle
On/Off Channel Operations[3] (Hot Switched)				
20dBm	—	100M	—	Cycle
25dBm	—	10M	—	Cycle
30dBm	—	0.3M	—	Cycle
Off-State Input-Output Leakage @ 100V	—	470	—	fA
On-State Resistance[4]	—	1.0	3.0	Ω
Off-State Capacitance (C_{IO})[5]	—	45	—	fF
Channel to Channel Off-State Capacitance (Coff)[6]				
In1 – In2	—	40	—	fF
In1 – In6	—	2	—	fF

Notes:

1. Settling time to within 0.05dB of final value.
2. Predicted number of operation cycles as observed on a sample size of 75 units, 10kHz cycle rate, and room temperature with Hot Switch Restrictions.
3. Point at which 50% of the population of tested channels failed. Hot switched operations, 500MHz CW RF signal, measured at 10kHz cycling rate at room temperature. See section Switch Reliability Test Results.
4. Measured at 1A, DC.
5. Capacitance between input and output pins measured at 1MHz at room temperature.
6. Capacitance between channel inputs measured at 1MHz at room temperature.

Table 5. Driver DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
High Voltage Gate Bias VBB Current (I_{BB})	—	—	0.1	mA
Driver Logic Supply V_{DD} Current in standby (I_{DD})	—	10	50	µA
Driver Input (D_{IN}) @ V_{DD}=5.0V				
High-Level Logic Voltage V_{IH}	3.5	5.0	5.3	V
Low-Logic Input Voltage V_{IL}	-0.3	—	0.8	V
High-Logic Input Current I_{IH}	—	—	1	µA
Driver Output (D_{OUT}) V_{DD}=4.5V				
High-Level Logic Output V_{OH} [1]	4	—	—	V
Low-Level Logic Output V_{OL} [2]	—	—	0.1	V

Notes:

1. V_{OH} measured at IDOUT = +0.1mA.
2. V_{OL} measured at IDOUT = -0.1mA.

Table 6. Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	—	—	5	MHz
Clock Width High and Low t_{WL},t_{WH}	100	—	—	ns
Data Setup Time before Clock Rises t_{SU}	50	—	—	ns
Data Hold Time after Clock Rises t_H	50	—	—	ns
Latch Enable Pulse Width t_{WLE}	100	—	—	ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	50	—	—	ns

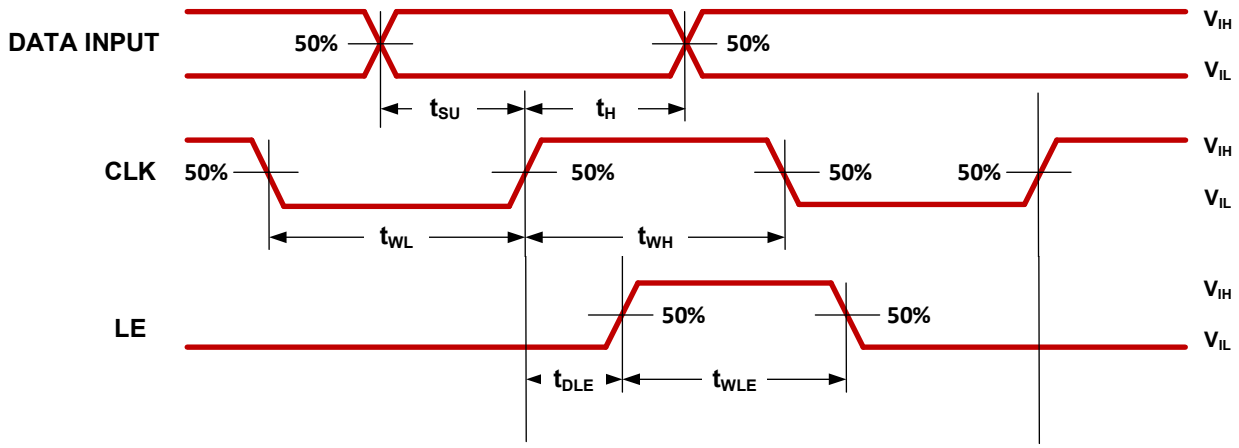
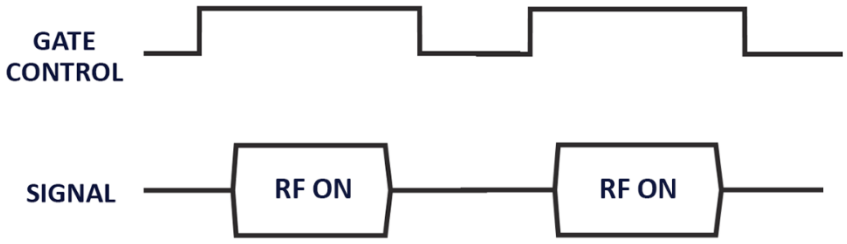


Figure 1. Driver Interface Timing Diagram

Hot Switch Restrictions

The MM3100 is not intended for hot switching applications and care should be taken to ensure that switching occurs at less than 0.5V difference between the input and output. In addition, keep the voltage on the output below 6V when closing the switch.



If the MM3100 is used in hot switching applications, the number cycling operations of the device will be degraded. See section Switch Reliability Test Results and Figure 13 for more information.

Floating Node Restrictions

RF I/O pins must not be allowed to electrically float during switch operation and therefore require some form of a DC path to ground to prevent charge accumulation. DC paths can be an inductor or high-value resistance that serves as a discharge path. Floating node examples and recommendations include:

- Unused RF I/O pins: resistively terminate or tie to ground.
- Series capacitance coupling between RF pins: shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Typical Design Considerations

When using the MM3100, exercise care to maintain certain voltage levels on the switch, depending on its state.

- To avoid **Hot Switching** when opening or closing the switch, the MM3100 Input and Output always need to be within 0.5V of each other. See section Hot Switch Restrictions for more details.
- To avoid **unintended de-actuation** of a closed switch, the voltage on the output can be no greater than the 'On-State DC Carry Voltage'.

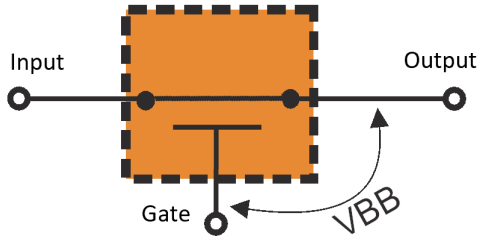


Figure 2. Closed Switch Gate (V_{BB}) to Output Voltage Considerations

- To avoid **unintended actuation** of an open switch, the output must be kept below the 'Off-State Output Voltage to GND'.
- To ensure that the switch is able to actuate, the voltage on the output must be kept below 6V when closing the switch.

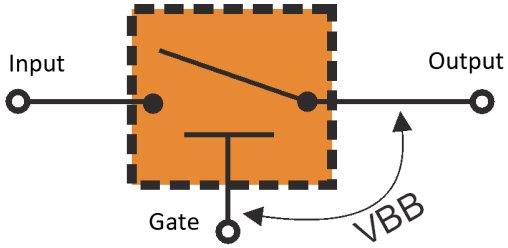


Figure 3. Open Switch Gate (V_{BB}) to Output Voltage Considerations

Thermal and Power Handling Considerations

In high-power operation, the case temperature of the MM3100 should not be allowed to exceed 85°C. Self-heating of the device, due to internal power dissipation, will elevate the case temperature over and above ambient temperature. Self-heating is a function of the applied power and signal frequency.

As an empirical example, an internal power dissipation of 0.9W resulted in a 40°C rise in case temperature. With an ambient temperature of 45°C (85°C - 40°C) and an insertion loss of -0.15dB at 300MHz, the allowable power handling can be estimated as:

$$\text{Power Handling} = \text{Max. Power Dissipation} / (1\text{-}10^{\wedge(\text{Insertion Loss}/10)})$$
$$= 0.9 / 0.034$$
$$= 26.5\ \text{W}$$

Additionally, since the MM3100 device is very linear, insertion loss is approximated as:

$$\text{Insertion Loss} = (-1.764\text{E-}10) * \text{frequency (Hz)} - 0.1087$$

Given these relationships, a convenient graph of Maximum Power Handling versus Frequency with a 40°C rise in case temperature is shown in Figure 4 below.

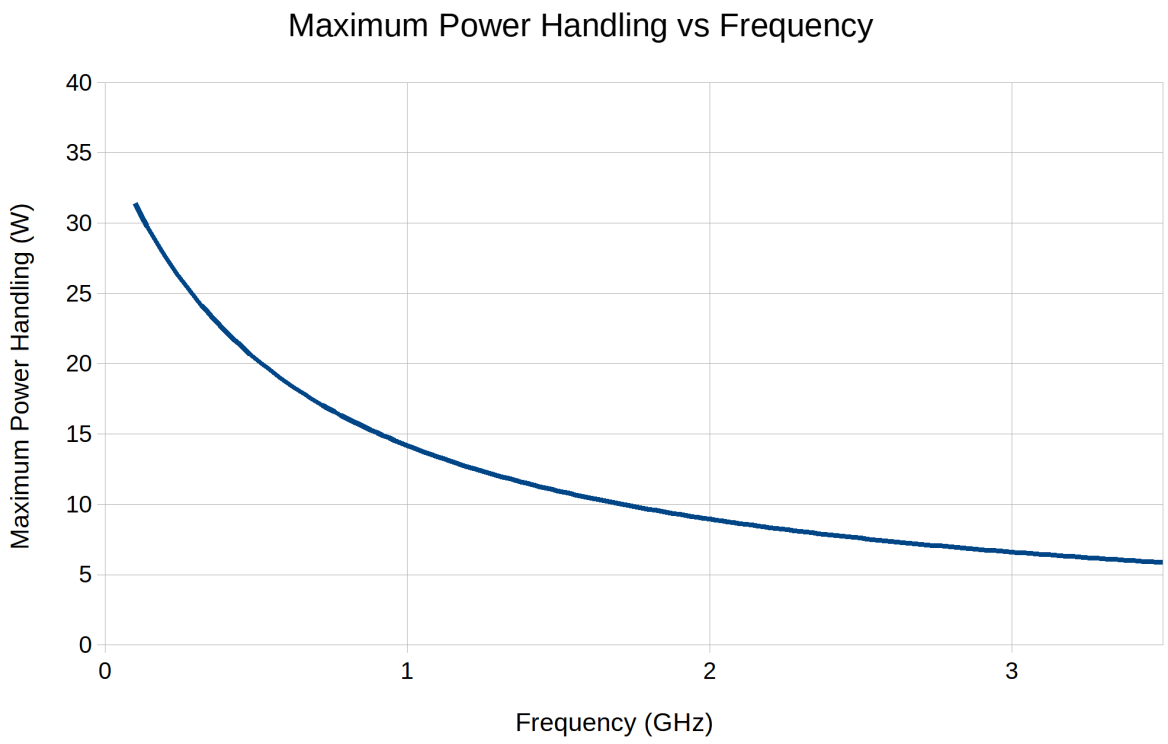


Figure 4. Maximum Power Handling versus Frequency at Ambient 45°C

Functional Block Diagram

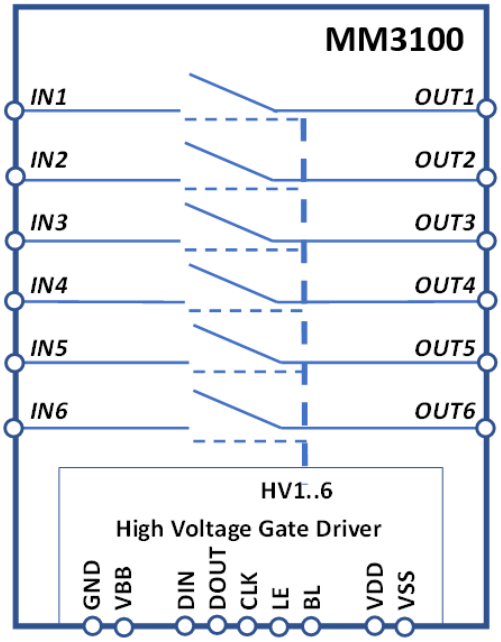


Figure 5. Functional Block Diagram

49-Lead BGA Package Pinout

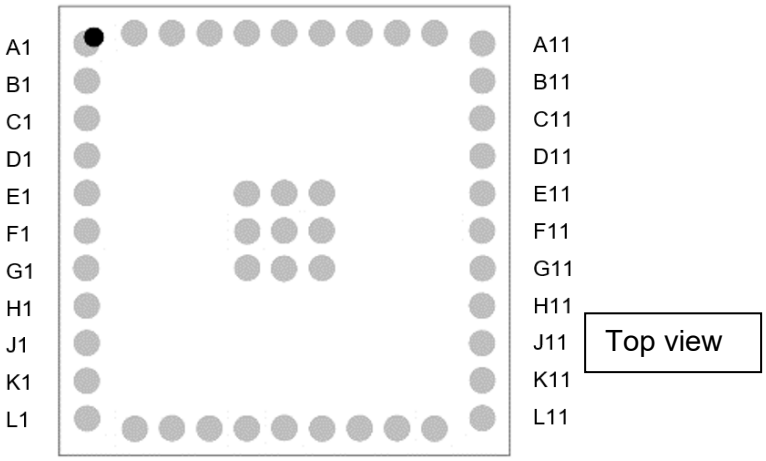


Figure 6. Top View Pin Layout

Dot indicates pin 1. See Table 7 Detailed Pin Description for detailed pin description.

Table 7. Detailed Pin Description

Pin Number	Pin Name	Description
GND	A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	Ground Reference, internal shield
VBB	G1	Gate Bias High-Voltage Supply
VDD	F11	Driver Logic Supply
VSS	G11	Supply Voltage Return
IN1	K1	Input (Contact 1)
IN2	L3	Input (Contact 2)
IN3	L5	Input (Contact 3)
IN4	L7	Input (Contact 4)
IN5	L9	Input (Contact 5)
IN6	K11	Input (Contact 6)
OUT1	B1	Output (Beam 1)
OUT2	A3	Output (Beam 2)
OUT3	A5	Output (Beam 3)
OUT4	A7	Output (Beam 4)
OUT5	A9	Output (Beam 5)
OUT6	B11	Output (Beam 6)
DIN	E1	Driver Serial Data Input
DOUT	H1	Driver Serial Data Output
CLK	H11	Driver Clock Input
LE	E11	Driver Latch Input
BL	D1	All Channels Off
N/C	F1, D11	Do Not Connect

EVK Performance

Typical performance as measured on the MM3100EVK evaluation board.

Adjacent Channel Isolation

Adjacent channel (Ch) isolation is defined for the MM3100 in two ways:

1. Both channels closed: measured between Ch 3 Output and Ch 4 input. This particular combination is the worst case for channel-to-channel isolation.
2. Second channel open: measured between Ch 3 Output and Ch 4 input, with Ch 3 Closed and Ch 4 open.

Measurements are done at 3.0 GHz with all ports terminated with 50Ω during measurement as shown in Figure 7. Increasing channel physical separation increases isolation for the two cases as follows:

1. Both channels closed:
   - Second adjacent channel performance is typically 8 dB better than adjacent channel performance (example: Ch 2 – Ch 4).
   - Third adjacent channel performance is typically 15 dB better than adjacent channel performance (example: Ch 1 – Ch 4).
2. Second channel open:
   - Second adjacent channel performance is typically 13 dB better than adjacent channel performance (example: Ch 2 – Ch 4).
   - Third adjacent channel performance is typically 17 dB better than adjacent channel performance (example: Ch 1 – Ch 4).

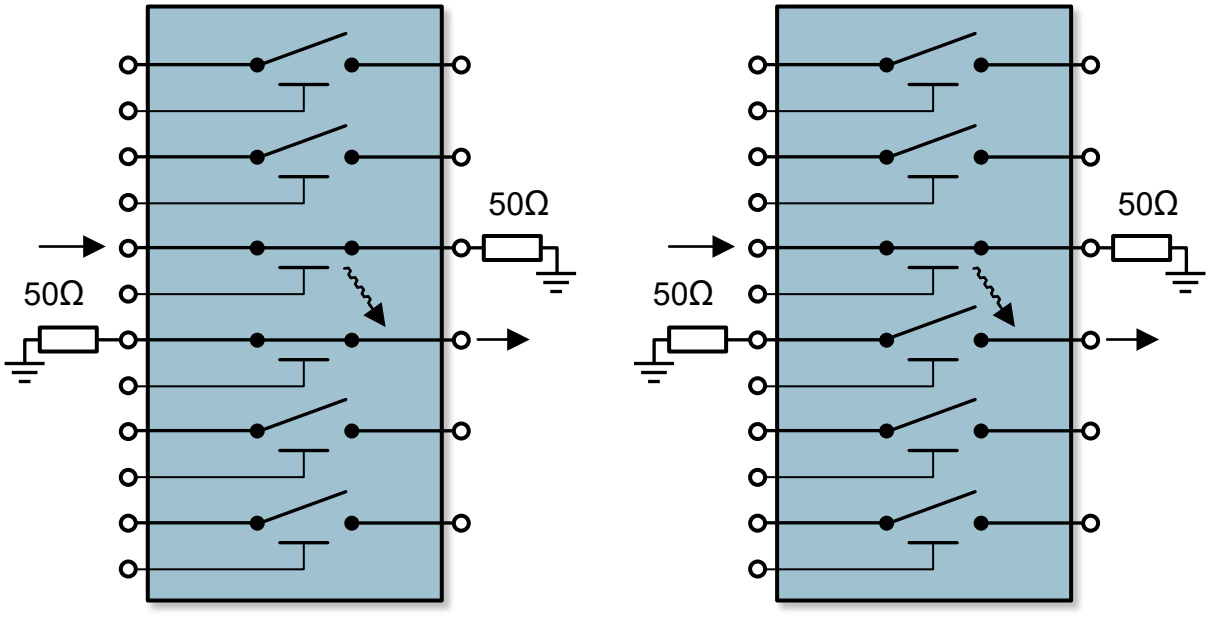


Figure 7. Adjacent Channel Isolation Measurement

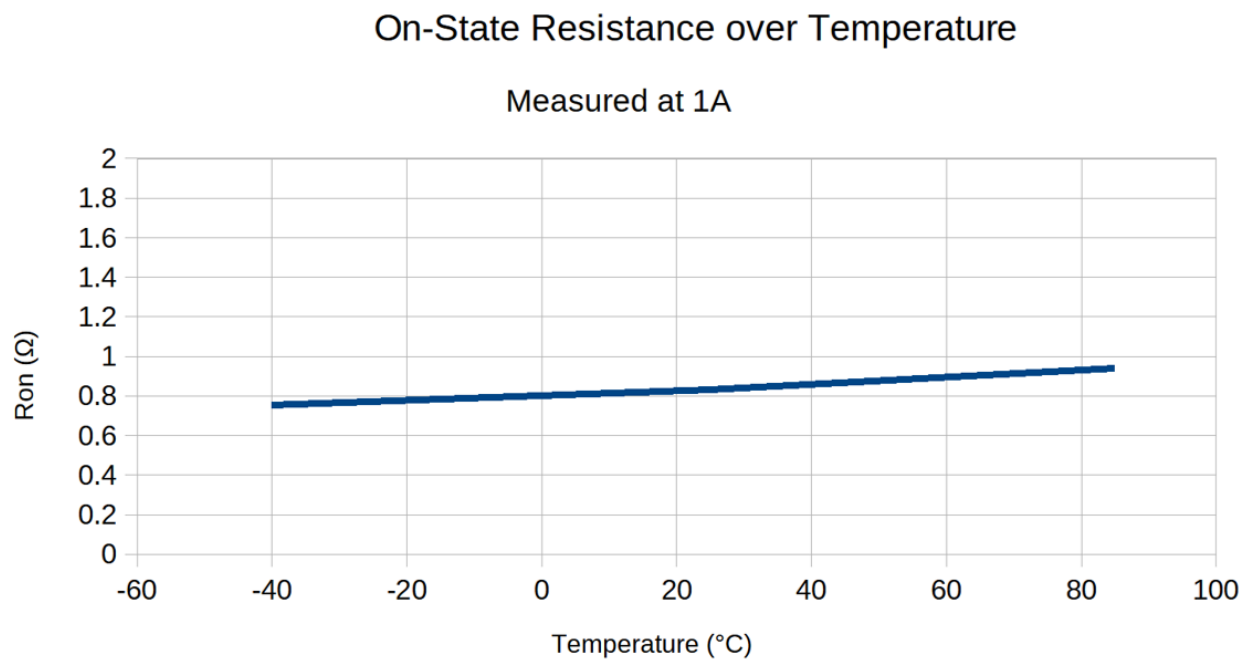


Figure 8. On-State Resistance over Temperature

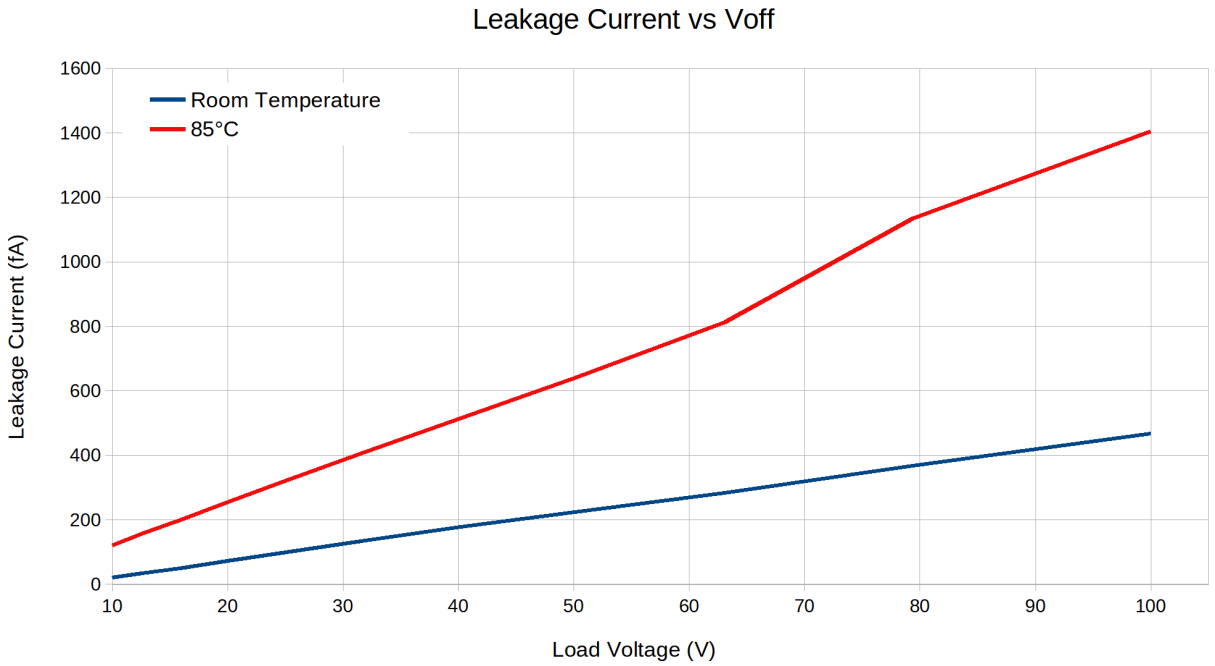


Figure 9. Off-State Input-Output Leakage Current vs V_{OFF}

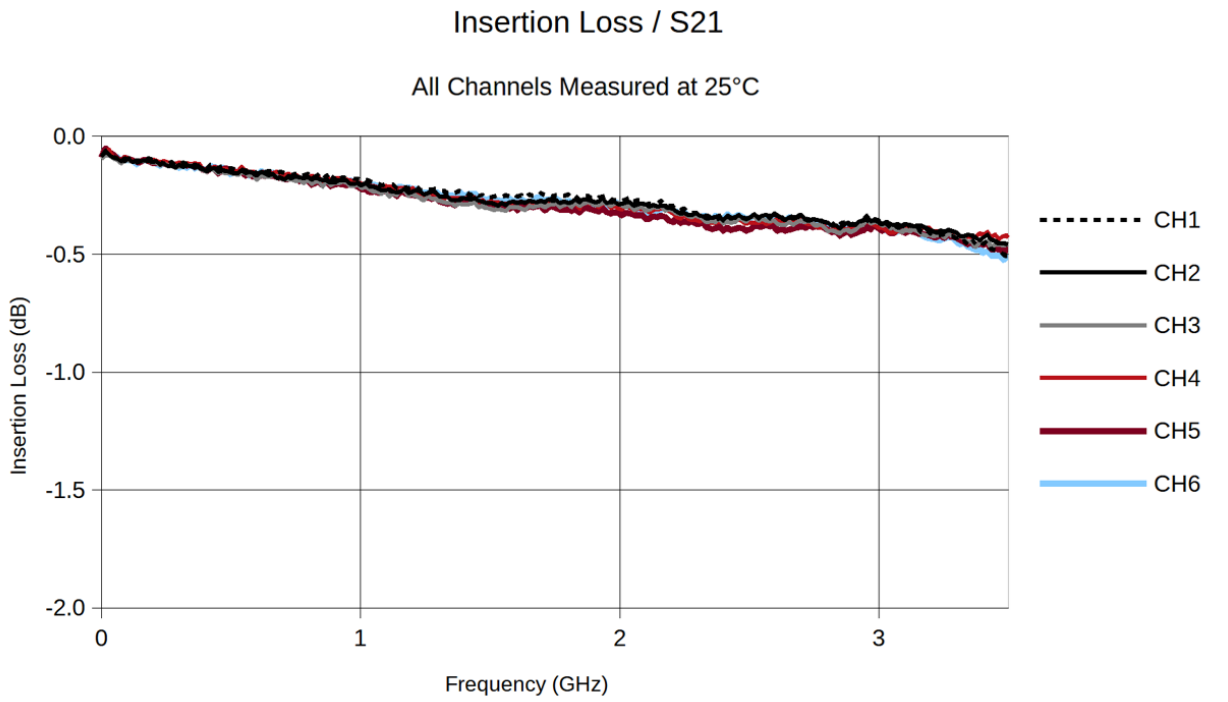


Figure 10. Typical Channel Insertion Loss vs Frequency (S_{21})

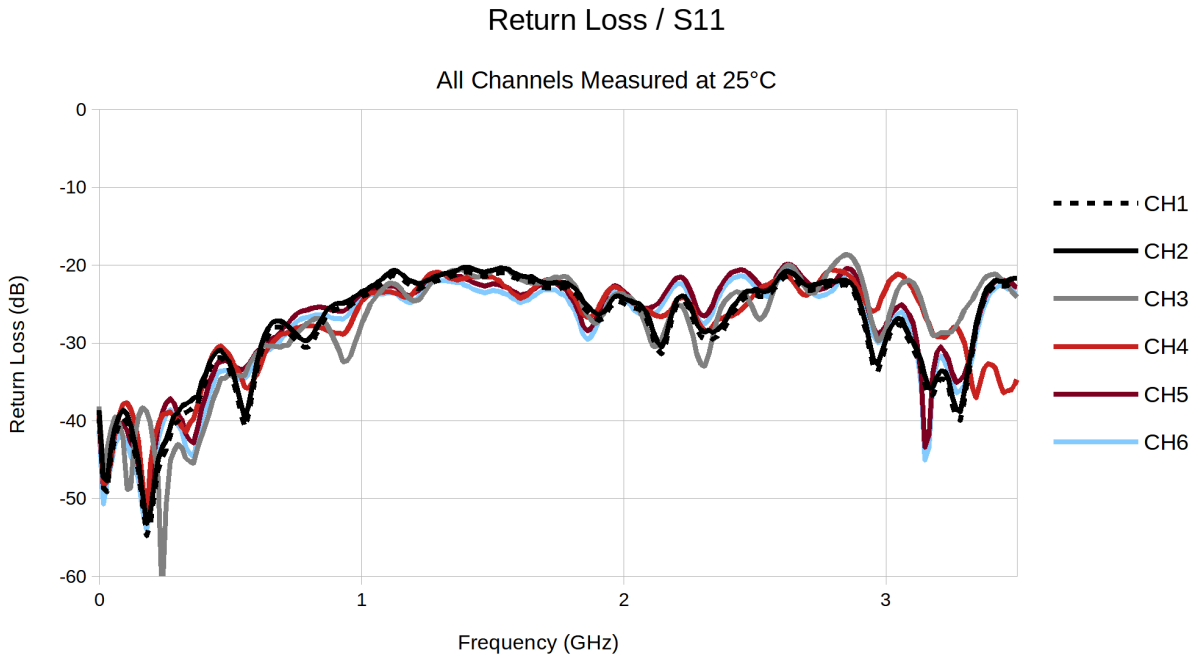


Figure 11. Typical Return Loss vs Frequency (S_{11})

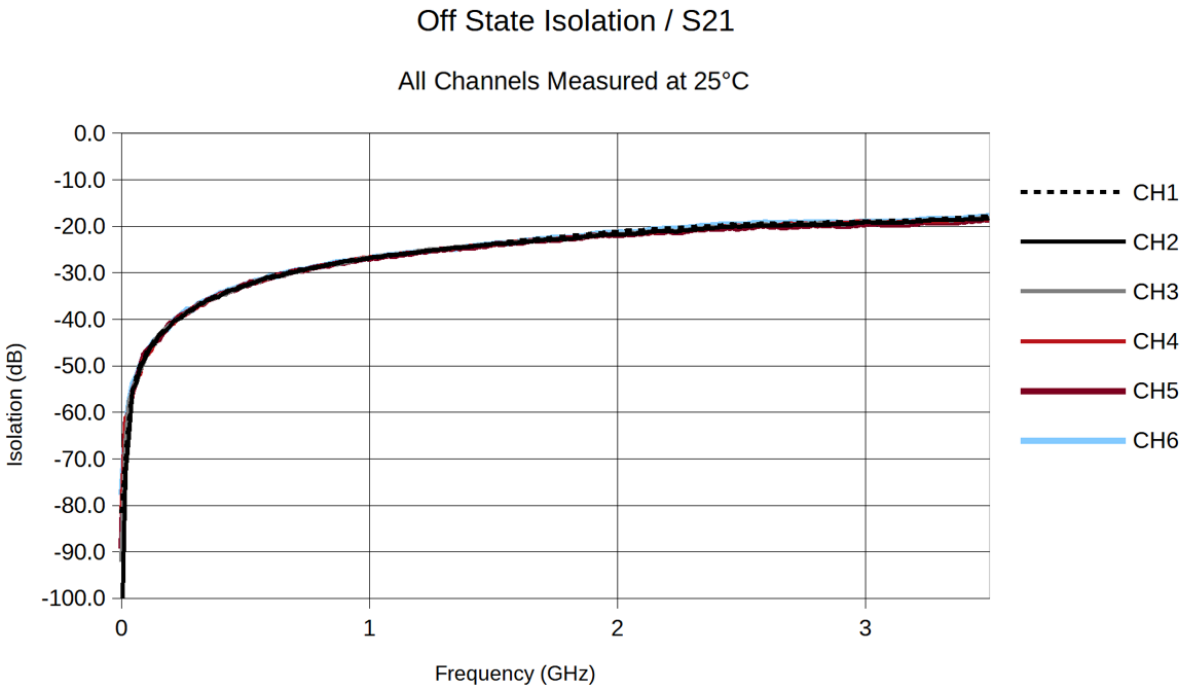


Figure 12. Typical Input to Output Isolation vs Frequency (S_{21} with channel off / open)

Switch Reliability Test Results

Hot switched actuation cycling reliability per channel test results are plotted below from 20dBm to 30dBm.

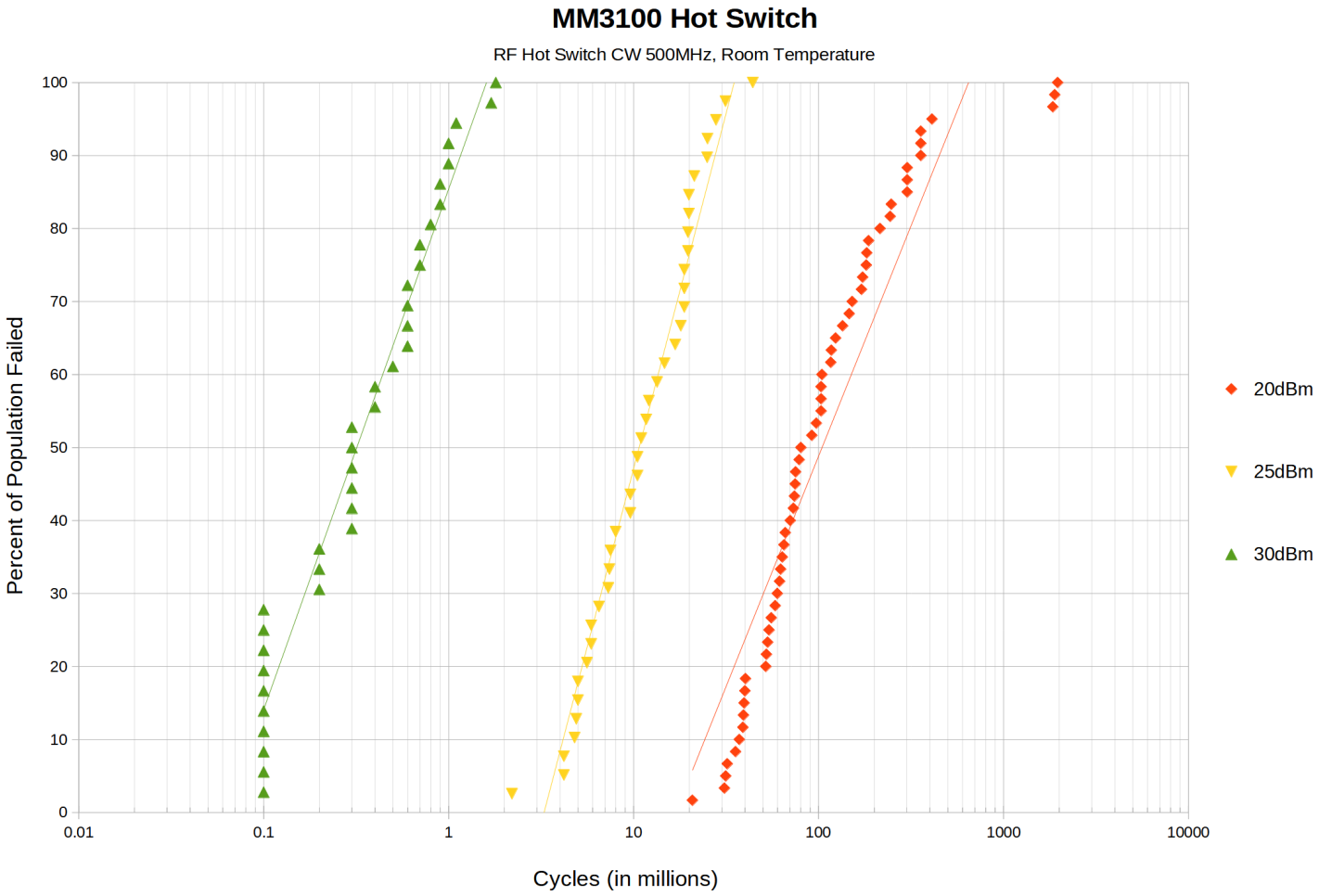


Figure 13. Hot Switch Endurance Test Results

High-Voltage Gate Driver Control

Operating Description

The integrated high-voltage gate driver is controlled through a serial-to-parallel interface that drives the high-voltage gate lines of the channel. Channel control data is shifted into a 10-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 14.

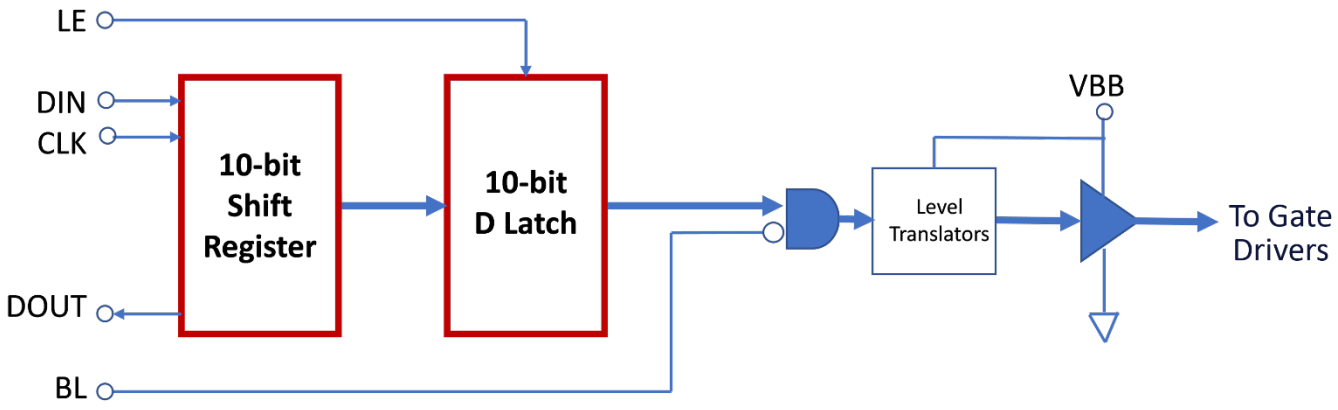


Figure 14. High-Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- A 10-bit data byte is serially loaded into shift register bits 1-to-10 on the positive edge of CLK. Shift order is MSB first starting with bit 10.
- Parallel data from the shift register is transferred to the high-voltage gate output buffers through a 10-bit D latch when the latch enable input LE is logically high. It is recommended that LE be held low while data is being shifted into the register.
- The MM3100 uses only six of the ten data bits latched for channel control. Bits 1 through 6 correspond to high-voltage gate lines HV1 through HV6 respectively. Bits 7, 8, 9, and 10 are unused bits; we recommend you set these to a logical “0”. Data bits set to logical “1” close the corresponding channel to On and “0” open the channel to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case, it is recommended to load 10-bit words consisting of four unused bits and six channel control bits so that each data packet controls one device.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically high. The pin should be logically low for normal operation.

Table 8. Truth Function Table

	Inputs				Shift Register		High-Voltage Output HVx	
Function	**Data**	**CLK**	**LE**	**BL**	**1**	**2 10**	**1**	**2 3 10**
All off (blank)	X	X	X	H	*	*…*	L	L L - - - - L
Load Shift Register	H/L	↑	L	L	H/L	*…*	*	* * - - - - *
Latched	X	X	L	L	*	*…*	*	* * - - - - *
Transfer	H/L	X	H	L	H/L	*…*	H/L	* * - - - - *

Notes:

H = High logic level

L = Low logic level

X = Don't care logic level

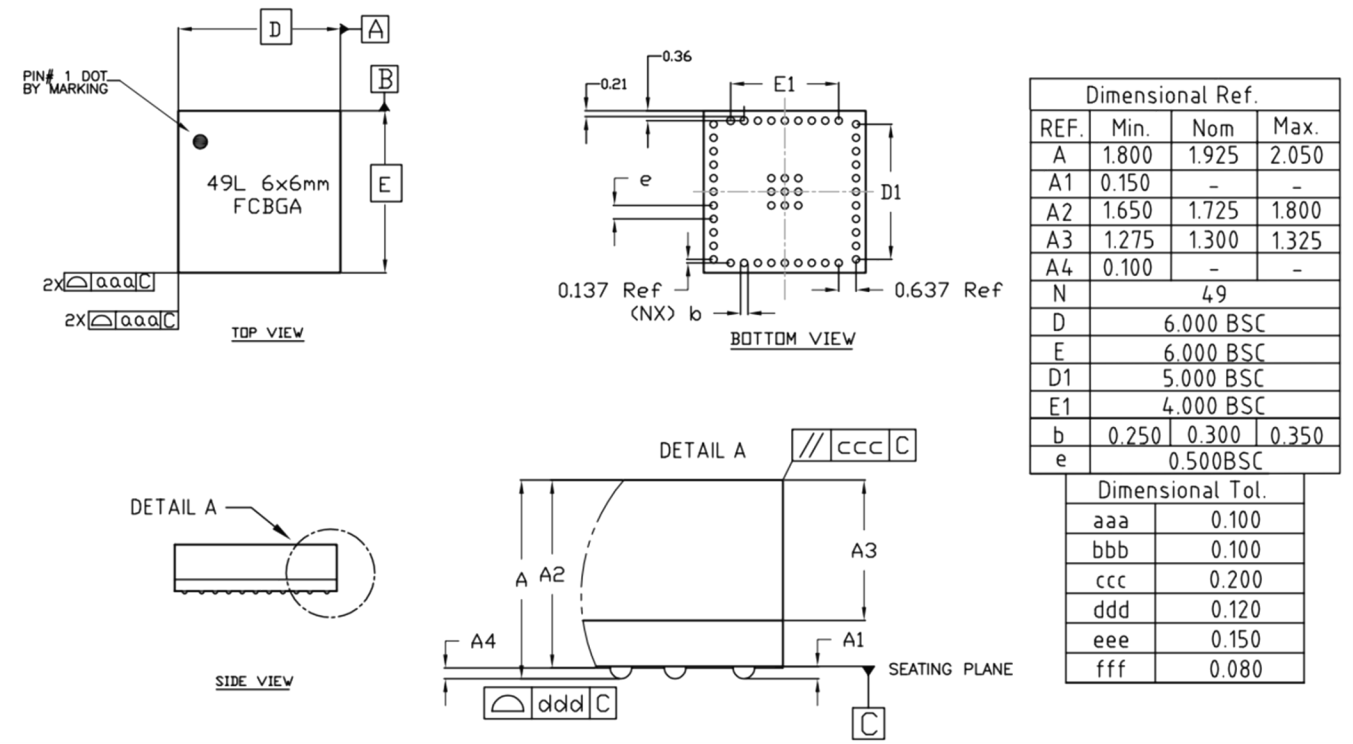
↑ = Low to high logic transition

* = Dependent on the previous stage's state before the last CLK or last LE high

HVx corresponds to high-voltage gate drivers where only HV1..6 are used. A high level closes the switch.

Package Drawing

49 Lead Ball Grid Array 0.30mm Ball, 0.50mm Pitch



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.800	1.925	2.050
A1	0.150	-	-
A2	1.650	1.725	1.800
A3	1.275	1.300	1.325
A4	0.100	-	-
N	49		
D	6.000 BSC		
E	6.000 BSC		
D1	5.000 BSC		
E1	4.000 BSC		
b	0.250	0.300	0.350
e	0.500BSC		

Dimensional Tol.	
aaa	0.100
bbb	0.100
ccc	0.200
ddd	0.120
eee	0.150
fff	0.080

Figure 15. Package Drawing

Recommended PCB Layout and SMT Parameters

- PCB pad pattern diagram is shown in Figure 16.
- Connect RF Ground node (floating shield inside the package) to RF Signal Ground.
- Open space around the package can have grounded thru holes.
- 20 micron (µm) thick solder mask.
- Type 3 or higher solder paste with no clean flux.
- Component placement force not to exceed 100 grams.

Recommended PCB Pad Pattern

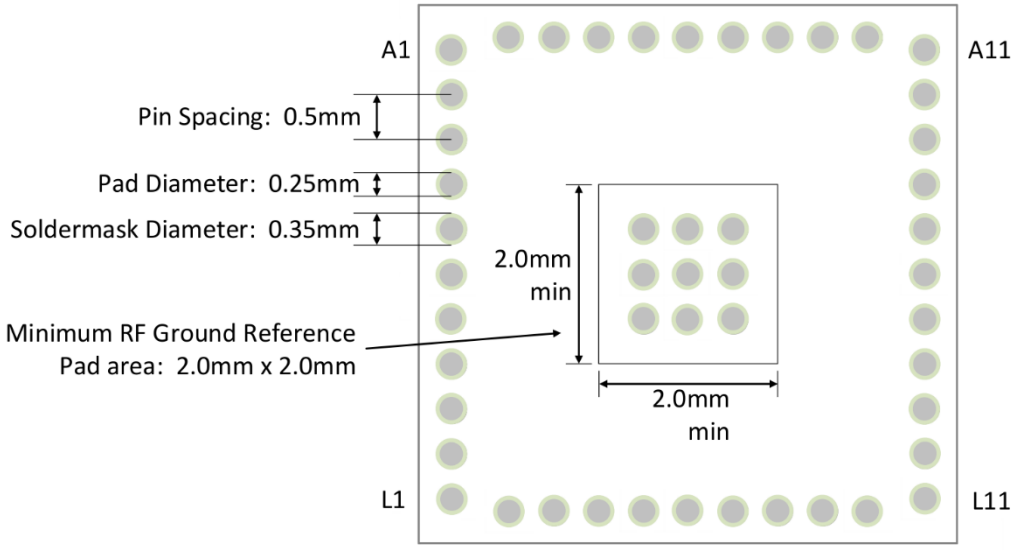


Figure 16. Recommended PCB Pad Pattern

Recommended Solder Reflow Profile

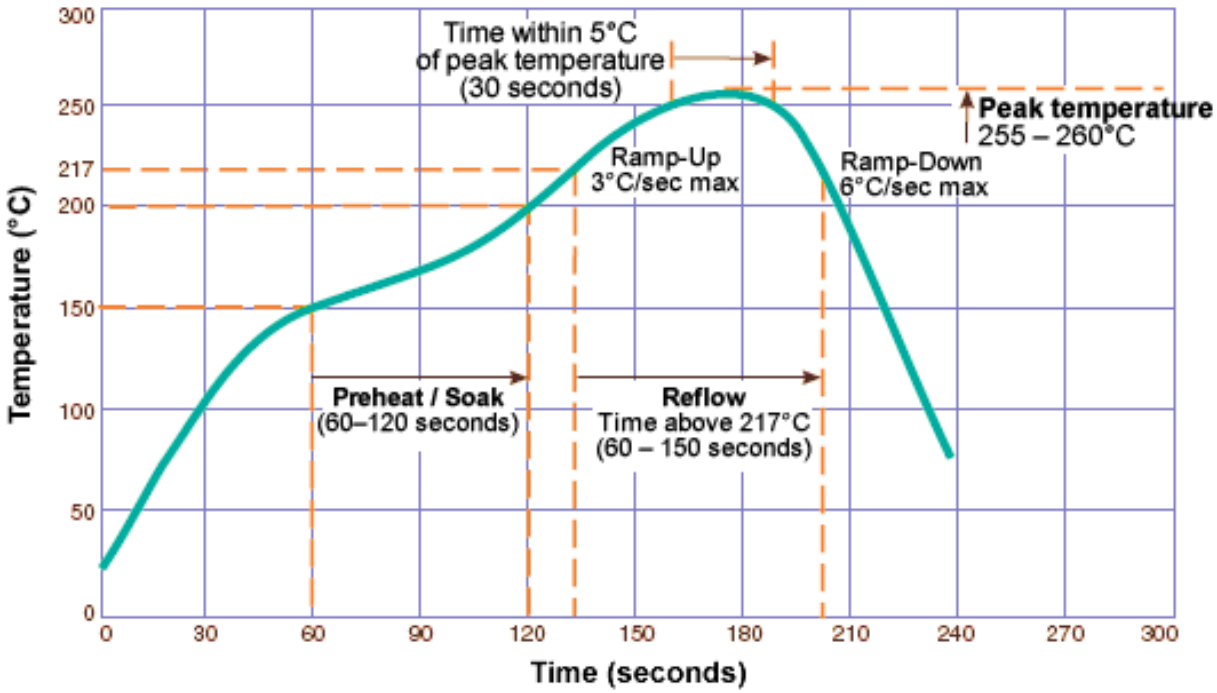


Figure 17. Reflow Profile

Follow MSL-3 (Moisture Sensitivity Level) handling precautions specified in IPC/JEDEC J-STD-020.

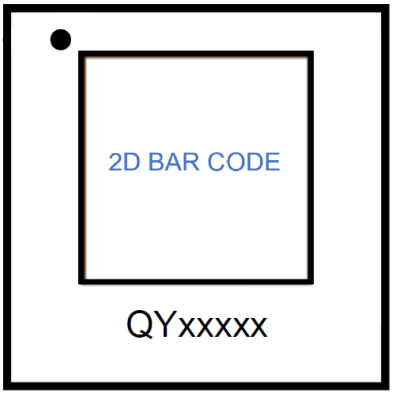
Storage and Shelf Life

Under typical industry storage conditions (≤30°C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date.
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less.

Package Marking Information

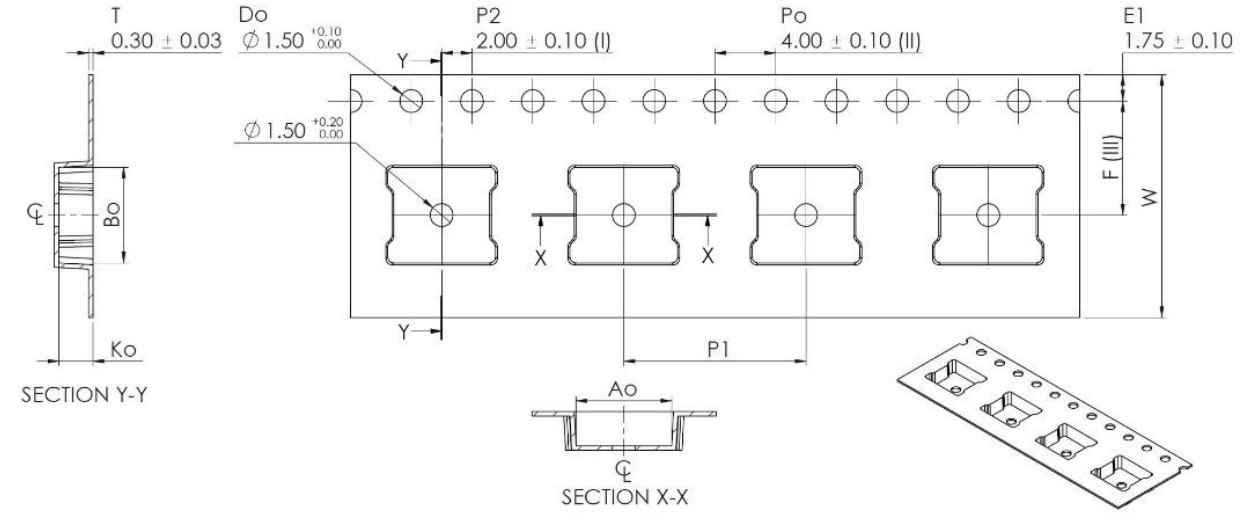
The MM3100 package marking and nomenclature are shown in Figure 18.



Dot ● = Pin 1 Indicator

Figure 18. Package Marking Drawing

Package Materials Information



Ao	6.30	+/- 0.10
Bo	6.30	+/- 0.10
Ko	2.25	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.00	+0.30 / -0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 19. Tape and Reel Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package Description	Temp Range	Device Marking[1]
MM3100-00NDB	DC-3GHz - 6xSPST - 6mm x 6mm BGA, Industrial Temp	-40°C to +85°C	QYxxxxx
MM3100-00NDB-TR	DC-3GHz - 6xSPST - 6mm x 6mm BGA, Industrial Temp, Tape and Reel (Qty 250)[2]	-40°C to +85°C	QYxxxxx
MM3100EVK	Evaluation board for MM3100, DC-3GHz - 6xSPST - 6mm x 6mm BGA		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is a placeholder for a 5-digit numerical code.
2. 250pcs standard tape and reel increment.

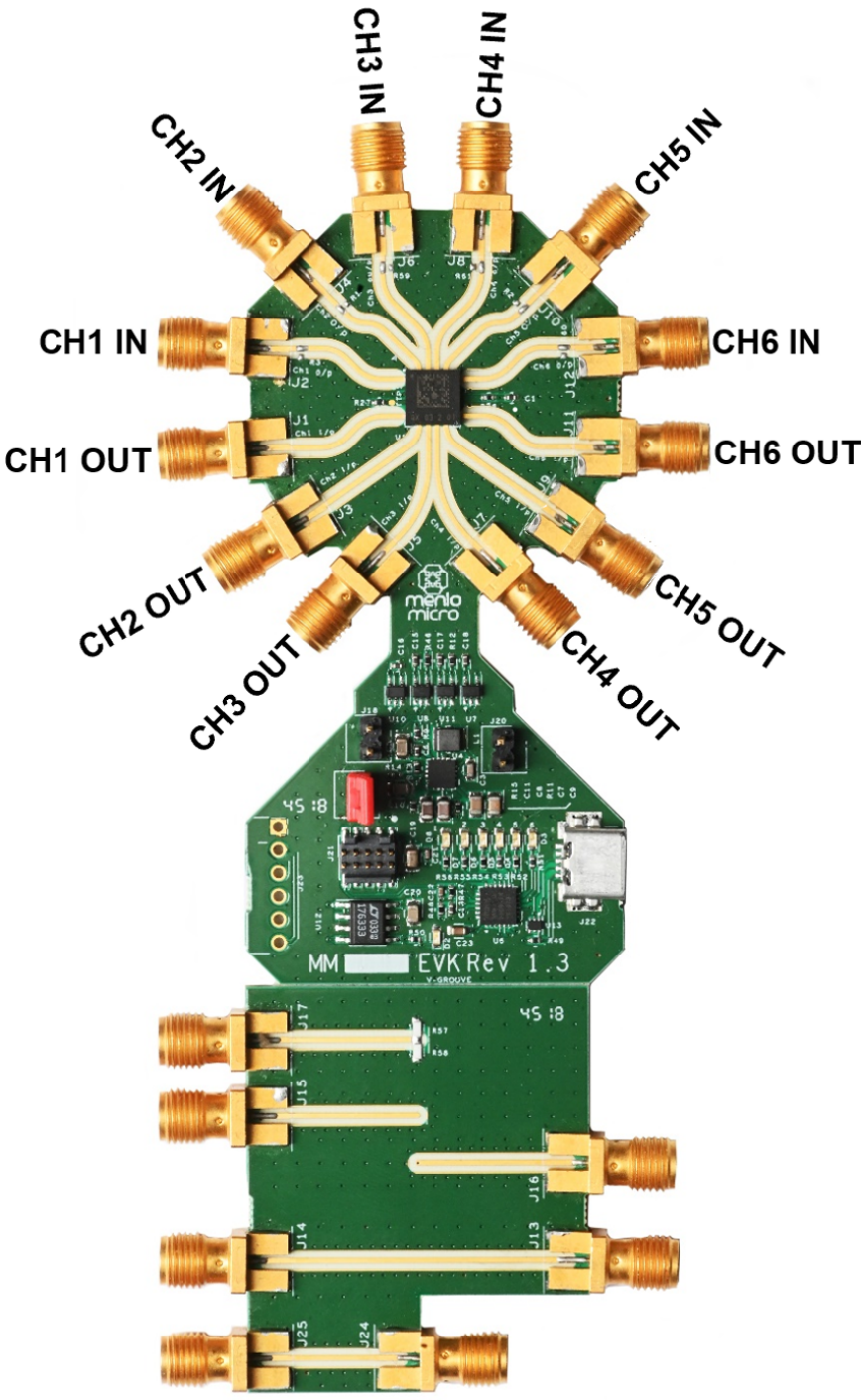


Figure 20. Evaluation Kit (EVK)

Important Information

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