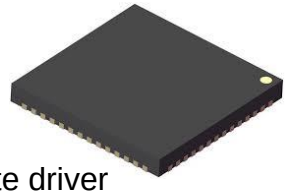
Preliminary Datasheet

MM5600 - 40 Gbps DPDT Differential Switch with Integrated Driver

Product Overview

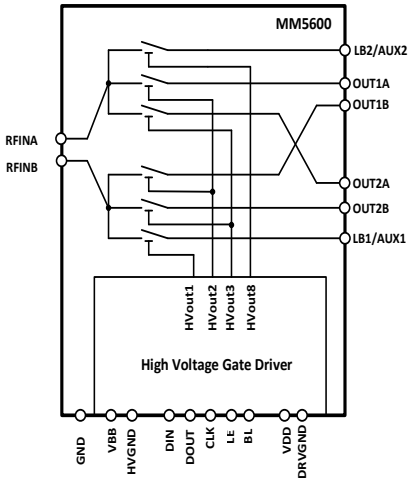
Description

Menlo Micro has developed a DPDT switch for high-speed differential signal switching. The MM5600 is based on Menlo's Ideal Switch™ technology and can operate for digital signals up to 40 Gbps or RF signals up to 20 GHz for high-performance applications. The MM5600 has low insertion loss, fast switching speed, internal ESD diodes, and can operate with greater than three billion switching cycles. The MM5600's integrated driver is controlled by a serial-to-parallel interface that drives the high voltage gate lines of the switches. The design also offers two separate single-ended ports and a considerable 90% reduction in size when compared with comparable EM relay solutions. An external +5 V_{DC} logic supply and high voltage +89 V_{DC} bias source is required for operation of the internal switch driver.



Features

- DC to 20 GHz range, up to 40 Gbps
- Low Insertion Loss
- Integrated driver eliminates requirement for an external gate driver
- Independently controlled dual loopback ports
- High Reliability: Greater than 3 billion switching operations



Applications

- Differential High-Speed Switching
- ATE-Device Interface Boards
- High-Speed Computer Peripheral Interfaces

Markets

- Differential Component Testing
- Differential Signal Routing
- Test and Measurement

Electrical Characteristics

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM5600 should be restricted to the limits indicated in Table 2 recommended operating conditions listed below.

Electrostatic Discharge (ESD) Safeguards

When handling the MM5600, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Susceptibility to Latch-Up

The following power sequence is recommended to avoid latch-up.

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, remove all inputs, remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present.

Table 1 Absolute Maximum Ratings [1]

Parameter	Minimum	Maximum	Unit
Max RF Input Power @ 6 GHz Single Ended		+33	dBm
DC Current Rating / Switch		250	mA
Hot Switching Current @ 0.5 V [2]		10	mA
Driver Voltage Supply VDD	-0.5	+6	V
High Voltage Gate Driver Supply VBB		+100	V
Driver Logic Input Levels	-0.5	VDD+0.5	V
Operating Temperature Range	-40	+85	ºC
Storage Temperature Range	-65	+150	ºC
Reflow Soldering (Pb Free) Peak temp		260	C
Reflow Soldering Time at Peak		30	Sec

[1] All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition).
[2] Exceeding this specification may reduce cycle lifetime.

ESD Rating HBM Driver Pins[3]		750	V
ESD Rating HBM RF I/O Pins[4]		2000	V
Mechanical Shock		TBD	G
Vibration		TBD	Hz

Table 2 DC and AC Electrical Specifications

All specifications valid over full VBB range and operating temperature range unless otherwise noted.

Parameter	Minimum	Typical	Maximum	Unit
Operating Frequency Range				
Differential DPDT mode	DC		20	GHz
Single Ended mode	DC		12	GHz
Max RF Power @ 3 GHz[5]			33	dBm
Insertion Loss				
Differential mode @ 20 GHz		4.5		dB
Single Ended mode @ 12 GHz		2.5		
Input / Output Return Loss				
Differential mode @ 20 GHz		10		dB
Single Ended mode @ 12 GHz		10		
Isolation				
Differential mode @ 20 GHz		20		dB
Single Ended mode @ 12 GHz		23		
Signal Integrity				
Differential Crosstalk		TBD		dB

[3] Driver pins include: CLK, BL, LE, DIN, DOUT, VBB, VDD.
[4] RF I/O pins include: RFINA, RFINB, OUT1A, OUT1B, OUT2A, OUT2B, LB1/AUX1, LB2/AUX2.
[5] Single Ended only 50 Ohms Measured at +85ºC.

Third-Order Intercept Point (IP3)[6]		95		dBm
Second Harmonic (H2)[7]		-130		dBc
Third Harmonic (H3)[8]		-130		dBc
On / Off Switching Time				
Turn on time		8	15	µs
Turn off time		2	5	
Settling Time				
Settling time: on		8.5	16	µs
Settling time: off		2.5	6	
On / Off Switch Operations	$3x10^9$	$30x10^9$		Cycles
DC Steady State Switch Carry Current			250	mA
Off-State Leakage Current at 30 V_{DC}		10		
Off-State Leakage Current at 3.3V_{DC}[9]		1		nA
On-State Resistance (R_{On})		1.2		Ω
Driver Logic Supply Voltage (V_{DD})	4.5	5.0	5.5	V
Driver Logic Supply Current (I_{DD})[10]			4	mA
Driver Input				
High-Level Logic Voltage V_{IH}	VDD-0.9V		VDD	V
Low-Logic Input Voltage V_{IL}	0		0.9	V
High-Logic Input Current I_{IH}			10	uA
Low-Logic Input Current I_{IL}			-350	uA
Driver Output				
High-Level Logic Output V_{OH}[11]	VDD – 1V			V
Low-Level Logic Output V_{OL}[12]			1	

[6] Measured at +25ºC and 37dBm input power.
[7] Measured at 900MHz fundamental frequency and 30 dBm input power.
[8] Measured at 900MHz fundamental frequency and 30 dBm input power.
[9] Not measured but guaranteed by design.
[10] Measured at Fclk = 8 MHz, LE = LOW.
[11] V_{OH} measured at ID_{OUT} = -0.1 mA.
[12] V_{OL} measured at ID_{OUT} = -0.1 mA.

High-Voltage Bias Supply Voltage (V_{BB})[13]	88	89	90	V_{DC}
High-Voltage Bias Supply Current (I_{BB})[14]			TBD	uA

[13] Note that High-Voltage Bias must be applied to VBB. It is not part of the integrated driver.
[14] Measured at V_{BB} = 100V and no load.

Table 3 Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	0		8	MHz
Clock Width High and Low t_{WL},t_{WH}	62			ns
Data Setup Time before Clock Rises t_{SU}	15			ns
Data Hold Time after Clock Rises t_H	30			ns
Latch Enable Pulse Width t_{WLE}	80			ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	35			ns
Latch Enable Setup Time before Clock Rises t_{SLE}	40			ns
Delay Time Clock to Data Low to High t_{DLH}			110	ns
Delay Time Clock to Data High to Low t_{DHL}			110	ns
All Logic Inputs t_r, t_f			5	ns

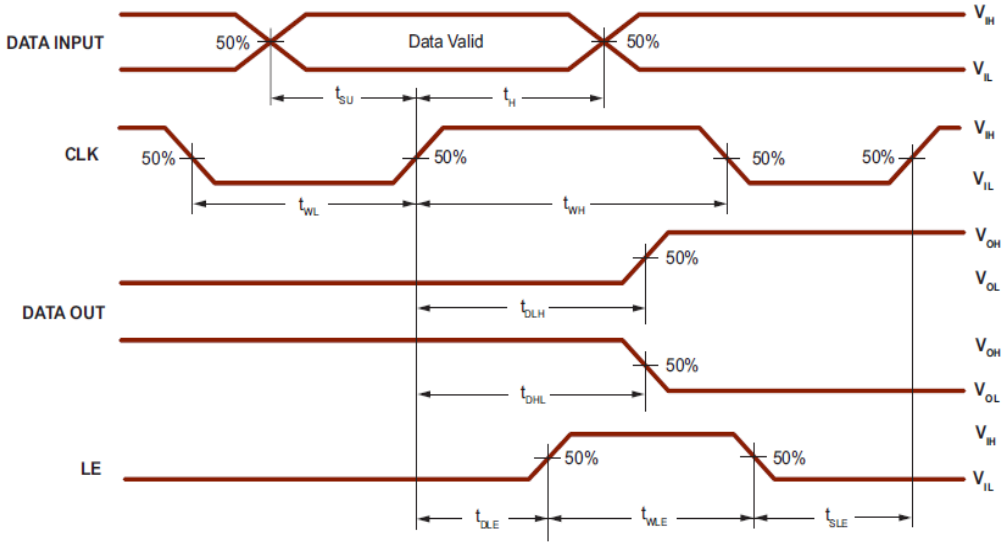


Figure 1: Driver Interface Timing Diagram

Functional Block Diagram

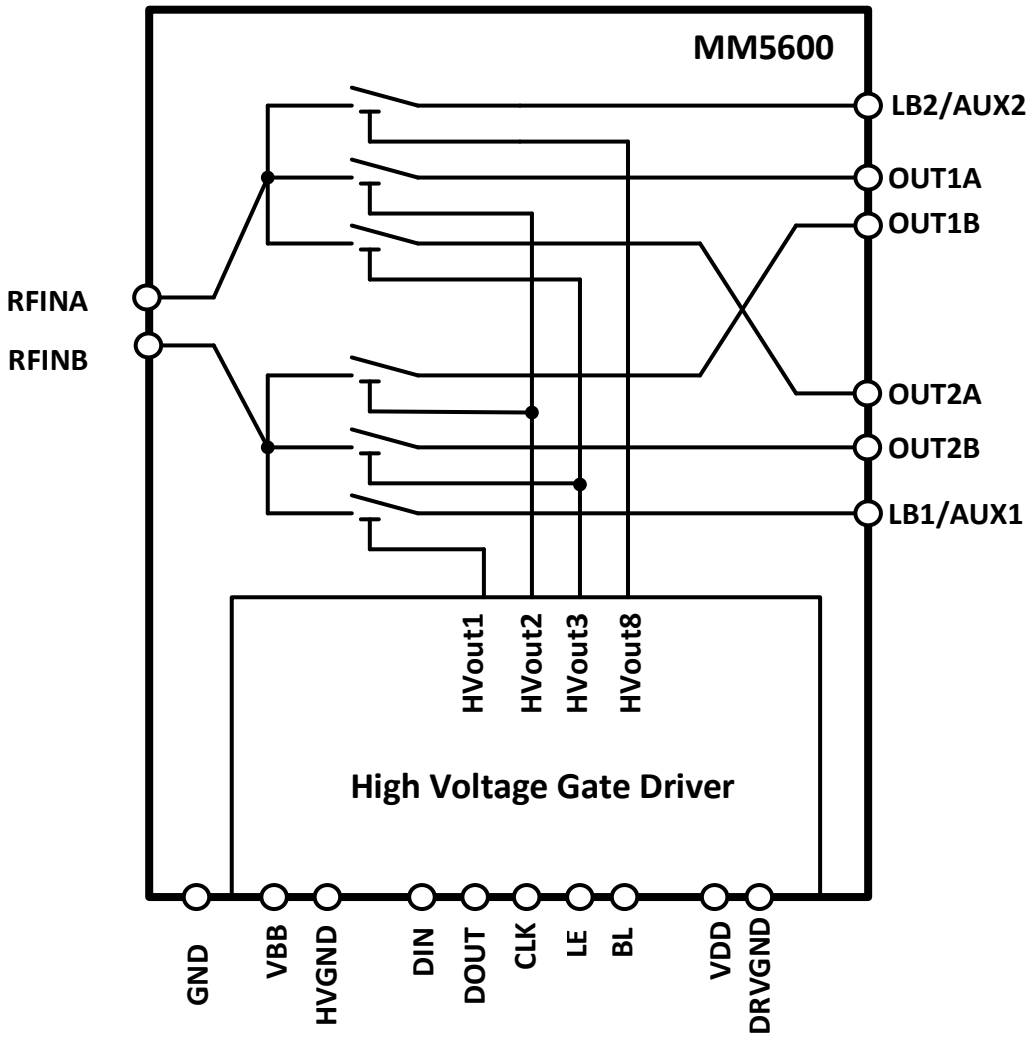


Figure 2: Functional Block Diagram

Package / Pinout Information

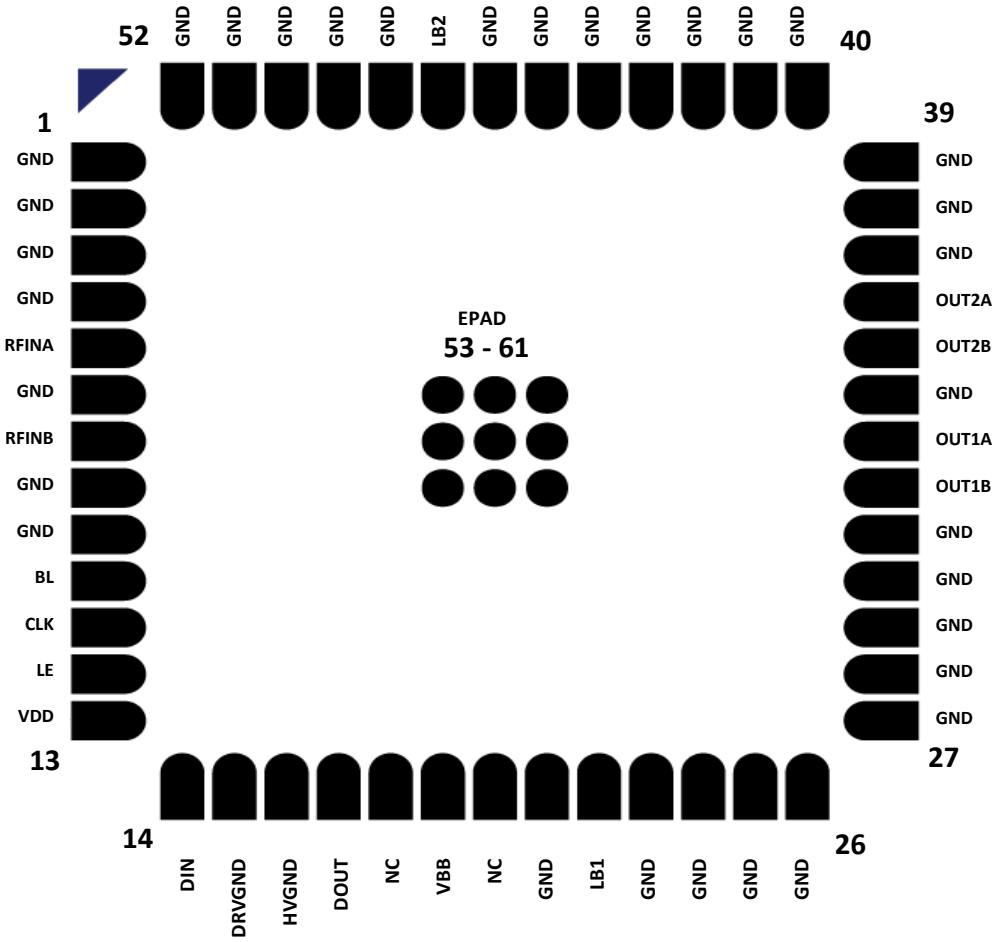


Figure 3: Top-Down Pin Layout

See Table 4 below for detailed pin description.

Table 4 Detailed Pin Description

Pin #	Pin Name	Description
1,2,3,4,6,8,9,21,23,24,25,26,27,28,29,30,31,34,37,38,39,40,41,42,43,44,45,46,48,49,50,51,52	GND	RF Ground
53,54,55,56,57,58,59,60,61	EPAD	Tie these pins to GND
15	DRVGND	Driver Ground
16	HVGND	High Voltage Ground
11	CLK	Clock
10	BL	Blank
12	LE	Latch Enable
18,20	NC	No Connect
14	DIN	Data In
17	DOUT	Data Out
19	V_{BB}	High Voltage Supply
13	V_{DD}	Logic Supply Voltage
5	RFINA	Differential Input A
7	RFINB	Differential Input B
33	OUT1A	Differential Output 1A
32	OUT1B	Differential Output 1B
36	OUT2A	Differential Output 2A
35	OUT2B	Differential Output 2B
22	LB1/AUX1	Single-ended Output 1
47	LB2/AUX2	Single-ended Output 2

RF Performance

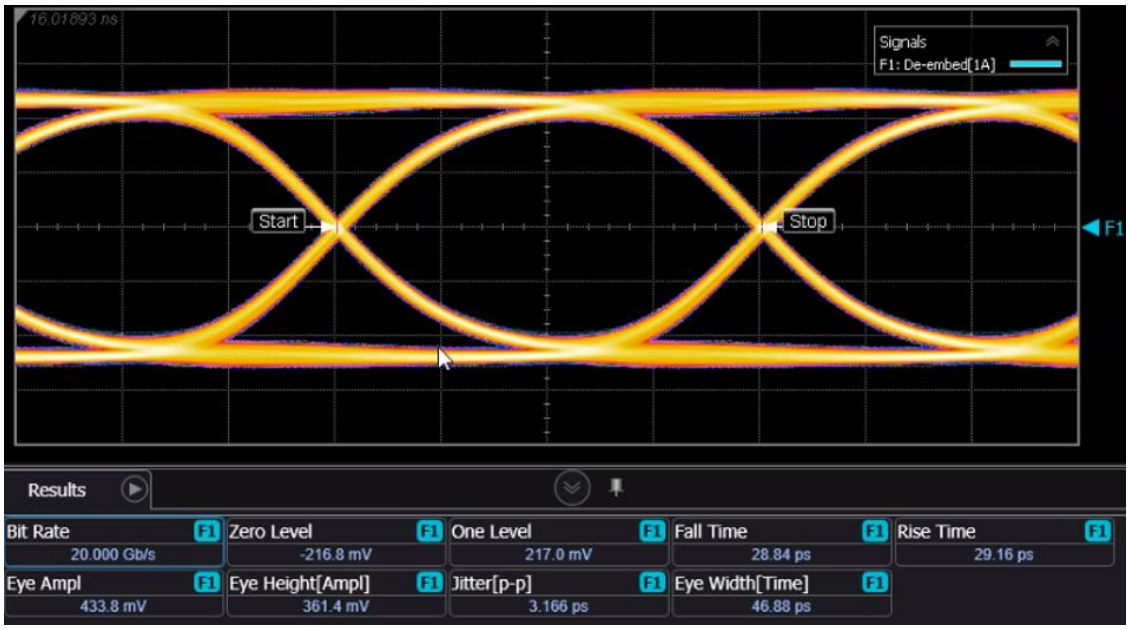
RF Performance – Differential Operation

TBD

Signal Integrity Performance (Measured)

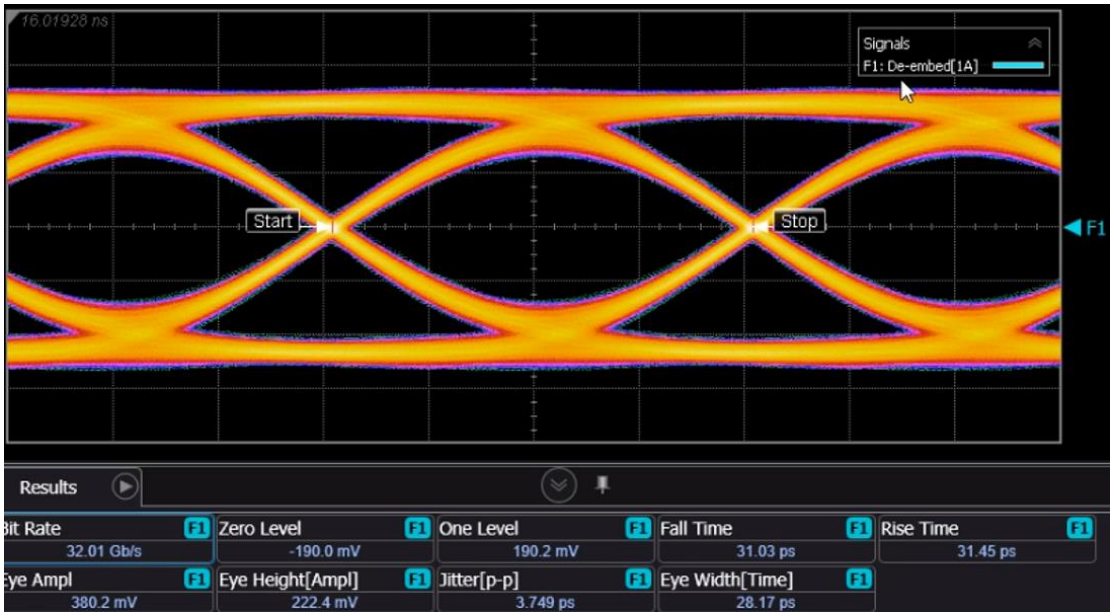
Test conditions for measurements below are:

- 2^{15}-1 PRBS signal
- PRBS output is 500mVp-p
- RF connector and RF traces are de-embedded
- Measured single-ended on MM5130 EVK



Test Cases	Bit rate	Eye Height	Eye Width	Jitter (Peak to Peak)	Rise Time (10%-90%)	Fall Time (90%-10%)
Baseline	19.965 Gbps	440.0 mV	48.16 ps	1.999 ps	14.99 ps	14.33 ps
MM5130 EVK	20.000 Gbps	361.4 mV	46.88 ps	3.166 ps	29.16 ps	28.84 ps

20 Gbps Eye Diagram, single-ended



Test Cases	Bit rate	Eye Height	Eye Width	Jitter (Peak to Peak)	Rise Time (10%-90%)	Fall Time (90%-10%)
Baseline	31.990 Gbps	441.0 mV	28.435 ps	2.709 ps	14.31 ps	13.405 ps
MM5130 EVK	32.000 Gbps	222.4 mV	28.17 ps	3.166 ps	31.45 ps	31.03 ps

32 Gbps Eye Diagram, single-ended

High Voltage Gate Driver Control

Operating Description

The integrated high voltage gate driver is controlled through a serial-to-parallel interface that drives the high voltage gate lines of the switches. Switch control data is shifted into an 8-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 3 below.

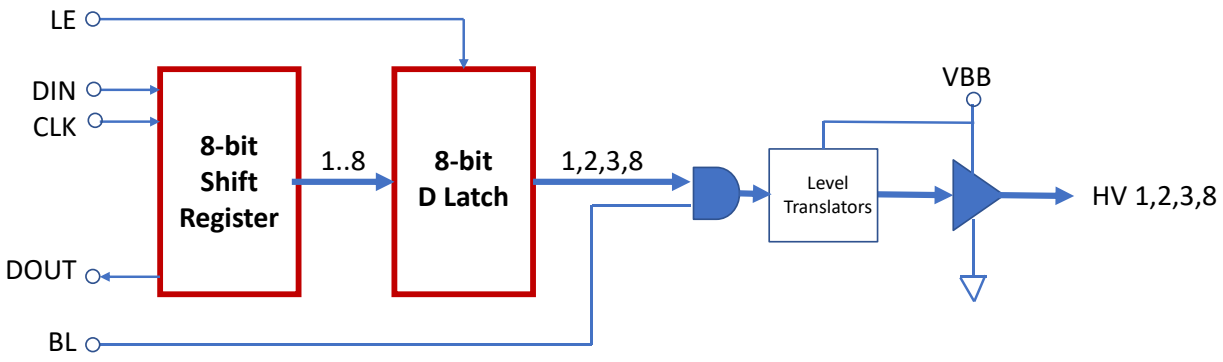


Figure 4: High Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- An 8-bit data byte is serially loaded into shift register bits 1-to-8 on the positive edge of CLK. Shift order is MSB first starting with bit 8.
- Parallel data from the shift register is transferred to the high voltage gate output buffers through an 8-bit D latch when the latch enable input LE is logically high. Transparent mode occurs when LE is held high while shifting data into the shift register.
- The MM5600 uses only four of the eight data bits latched for switch control. Bits 1, 2, and 3 and 8 correspond to high voltage gate lines HV1, HV2, HV3, and HV8 respectively. Bits 4,5,6 and 7 are not used. Data bits set to logical “1” close the corresponding switch to On and “0” open the switch to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 8-bit bytes consisting of 4 dummy bits and 4 switch control bits so that each byte controls one switch.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically low. The pin should be logically high for normal operation.
- Pins BL and LE have internal 20K ohm pull-up resistors to VDD. If blanking is not used, BL may be unconnected.

Table 5 *Truth Function Table*

	Inputs				Shift Register		High Voltage Output HVx
Function	**Data**	**CLK**	**LE**	**BL**	**1**	**2…8**	**1 2 3 - - - - 8**
All off (blank)	**X**	**X**	**X**	**L**	*	*…*	**L L L - - - - L**
Load Shift Register	**H/L**	↑	**L**	**H**	**H or L**	*…*	*** - - - - *
Latched	**X**	**X**	**L**	**H**	*	*…*	*** - - - - *
Transfer	**H/L**	**X**	**H**	**H**	**H/L**	*…*	**H/L** * * - - - - *

Note:

H = High logic level

L = Low logic level

X = Don't care logic level

↑ = Low to high logic transition

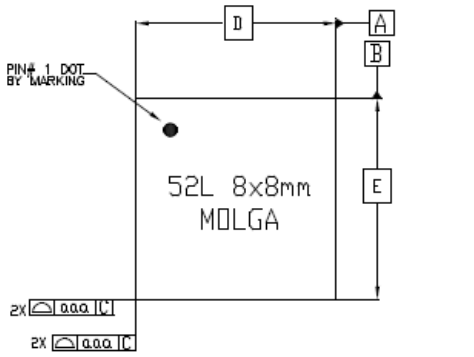
* = Dependent on the previous stage's state before the last CLK or last LE high

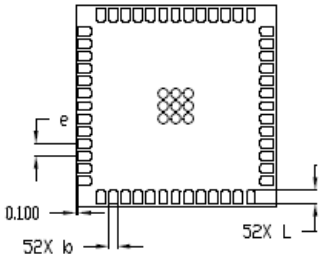
Each switch is individually controllable. In Table 6 below, primary usage states are highlighted in **bold**. Multiple branches may be closed simultaneously, however RF performance is not specified for such states. Note that On= Closed, Off = Open.

Table 6 Applied Gate Voltage vs. RF Switch States

HV1	HV2	HV3	HV8	RFINA – OUT1A	RFINA – OUT2A	RFINA – LB1/AUX1	RFINB – OUT1B	RFINB – OUT2B	RFINB – LB2/AUX2
0	**0**	**0**	**VBB**	**Off**	**Off**	**Off**	**Off**	**Off**	**On**
0	**0**	**VBB**	**0**	**Off**	**On**	**Off**	**Off**	**On**	**Off**
0	**VBB**	**0**	**0**	**On**	**Off**	**Off**	**On**	**Off**	**Off**
VBB	**0**	**0**	**0**	**Off**	**Off**	**On**	**Off**	**Off**	**Off**
0	0	0	0	Off	Off	Off	Off	Off	Off
Other valid states									
0	0	VBB	VBB	Off	On	Off	Off	On	On
0	VBB	0	VBB	On	Off	Off	On	Off	On
0	VBB	VBB	0	On	On	Off	On	On	Off
VBB	0	0	VBB	Off	Off	On	Off	Off	On
VBB	0	VBB	0	Off	On	On	Off	On	Off
VBB	VBB	0	0	On	Off	On	On	Off	Off
VBB	VBB	0	VBB	On	Off	On	On	Off	On
VBB	VBB	VBB	0	On	On	On	On	On	Off
VBB	VBB	VBB	VBB	On	On	On	On	On	On
0	VBB	VBB	VBB	On	On	Off	On	On	On
VBB	0	VBB	VBB	Off	On	On	Off	On	On

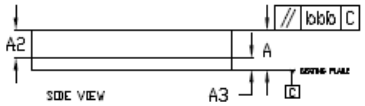
Package Layout





Dimensional Tol.	
aaa	0.100
bbb	0.100

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.505	1.580	1.655
A2	1.075	1.100	1.125
A3	0.430	0.480	0.530
D		8.000 BSC	
D1	-	-	-
E		8.000 BSC	
E1	-	-	-
b	0.300	0.350	0.400
L	0.390	0.550	0.600
e		0.500 BSC	



SIDE VIEW

Package Options and Ordering Information

Part Number	ECCN	Package	Temperature Range
MM5600-01	EAR99	DC-40Gbps - DPDT - 8mm x 8mm LGA (for semi test/ATE applications)	
MM5600-EVK1	EAR99	Evaluation board for MM5600 (differential crossover mode, w/Southwest connector-QTY-8) DC-40Gbps - DPDT - 8mm x 8mm BGA	
MM5600-EVK2	EAR99	Evaluation board for MM5600 (DPDT single-ended mode, w/Southwest connector-QTY-8) DC-40Gbps - DPDT - 8mm x 8mm LGA	

Important Information

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