



Preliminary Datasheet

MM5600 - 40 Gbps DPDT Differential Switch with Integrated Driver

Product Overview

Description

Menlo Micro has developed a DPDT switch for high-speed differential signal switching. The MM5600 is based on Menlo's Ideal Switch™ technology and can operate up to 40 Gbps for digital signaling applications, or high-performance RF applications up to 20 GHz. The MM5600 has low insertion loss, fast switching speed, internal ESD diodes, and can operate with greater than three billion switching cycles.

The MM5600's integrated driver is controlled by a serial-to-parallel interface that drives the high voltage gate lines of the switches. The design also offers two separate single-ended ports and a considerable 90% reduction in size when compared with comparable EM relay solutions. An external +5 VDC logic supply and high voltage +89 VDC bias source is required for operation of the internal switch driver.

Features

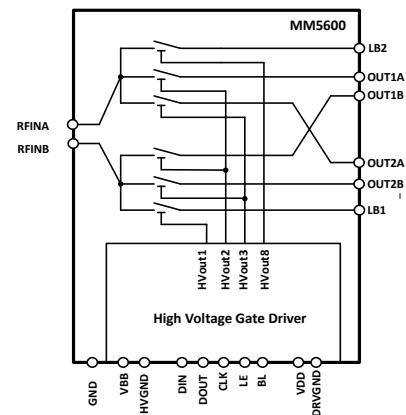
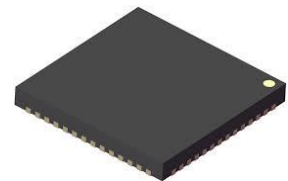
- DC to 20 GHz range, up to 40 Gbps
- Low Insertion Loss
- Integrated driver eliminates the requirement for an external gate driver
- Independently controlled dual loopback ports
- High Reliability: Greater than 3 billion switching operations

Applications

- Differential High-Speed Switching
- ATE-Device Interface Boards
- High-Speed Computer Peripheral Interfaces

Markets

- Differential Component Testing
- Differential Signal Routing
- Test and Measurement



Electrical Characteristics

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM5600 should be restricted to the limits indicated in the recommended operating conditions listed in Tables 2 through 5 below.

Electrostatic Discharge (ESD) Safeguards

When handling the MM5600, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Susceptibility to Latch-Up

The following power sequence is recommended to avoid latch-up.

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, remove all inputs, remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present.

Table 1 Absolute Maximum Ratings ¹

Parameter	Minimum	Maximum	Unit
Max RF Input Power @ 6 GHz Single Ended		+33	dBm
DC Current Rating / Switch		250	mA
Hot Switching Current @ 0.5 V ^{2 3}		10	mA
Driver Voltage Supply VDD	-0.5	+6	V
High Voltage Gate Driver Supply VBB		+100	V
Driver Logic Input Levels	-0.5	VDD+0.5	V
Operating Temperature Range	-40	+85	°C
Storage Temperature Range	-65	+150	°C
ESD Rating HBM Driver Pins ⁴		750	V
ESD Rating HBM RF I/O Pins ⁵		2000	V
Mechanical Shock		TBD	G
Vibration		TBD	Hz

¹ All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition).

² For hot-switching, differential voltage across switch terminals must be less than or equal to 0.5 V and each switch port must be within +/-0.5 V of RF ground.

³ RF pins must not be allowed to electrically float during switch operation. See section *Floating Node Restrictions* for details on avoiding floating nodes.

⁴ Driver pins include: CLK, BL, LE, DIN, DOUT, VBB, VDD.

⁵ RF I/O pins include: RFINA, RFINB, OUT1A, OUT1B, OUT2A, OUT2B, LB1, LB2.

DC and AC Electrical Specifications

All specifications valid over full VBB range and operating temperature range unless otherwise noted.

Table 2 RF Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Operating Frequency Range				
Single-Ended mode	DC		12	GHz
Differential mode	DC		20	
Max RF Power @ 3 GHz⁶			33	dBm
Insertion Loss				
Single-Ended mode @ 12 GHz		2.5		dB
Input / Output Return Loss				
Single-Ended mode @ 12 GHz		6		dB
Isolation				
Single-Ended mode @ 12 GHz		23		dB
Third-Order Intercept Point (IP3)⁷		95		dBm
Second Harmonic (H2)⁸		-130		dBc
Third Harmonic (H3)⁹		-130		dBc

Signal Integrity Differential Performance

Test conditions for the differential eye-diagram performance measurements are listed below:

- Test pattern: $2^{15}-1$ NRZ
- Differential RF input amplitude: 1000 mVpp
- Measurements performed at 32 Gbps and 40 Gbps
- Tests performed at ambient temperature
- RF connector, traces, and cables are de-embedded
- Testing performed on MM5600 EVK

⁶ Single Ended only 50 Ohms Measured at +85°C.

⁷ Measured at +25°C and 37dBm input power.

⁸ Measured at 2 GHz fundamental frequency and 33 dBm input power.

⁹ Measured at 2 GHz fundamental frequency and 33 dBm input power.

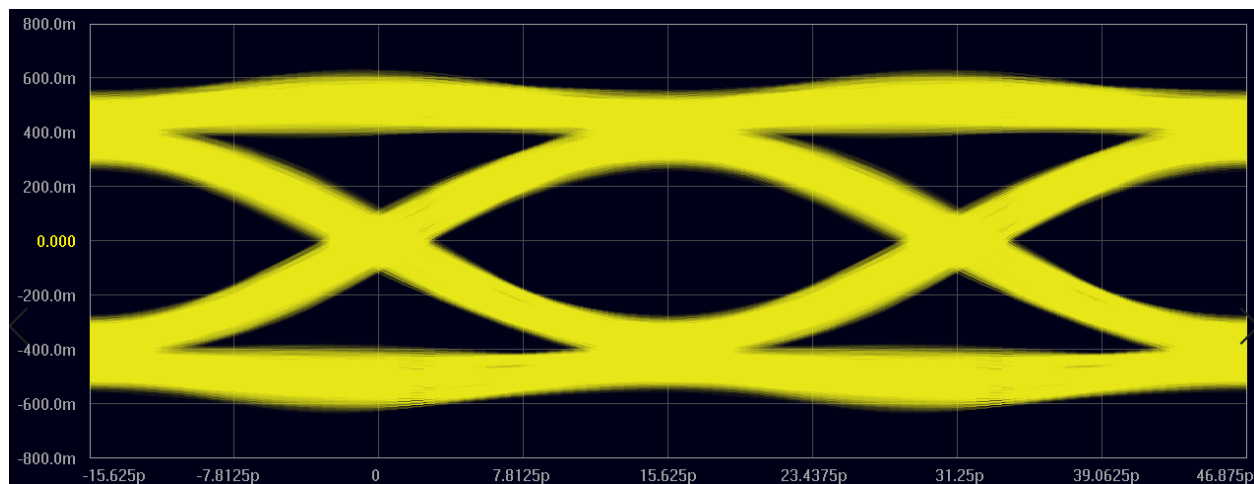


Figure 1 32 Gbps OUT1 ON Eye Diagram

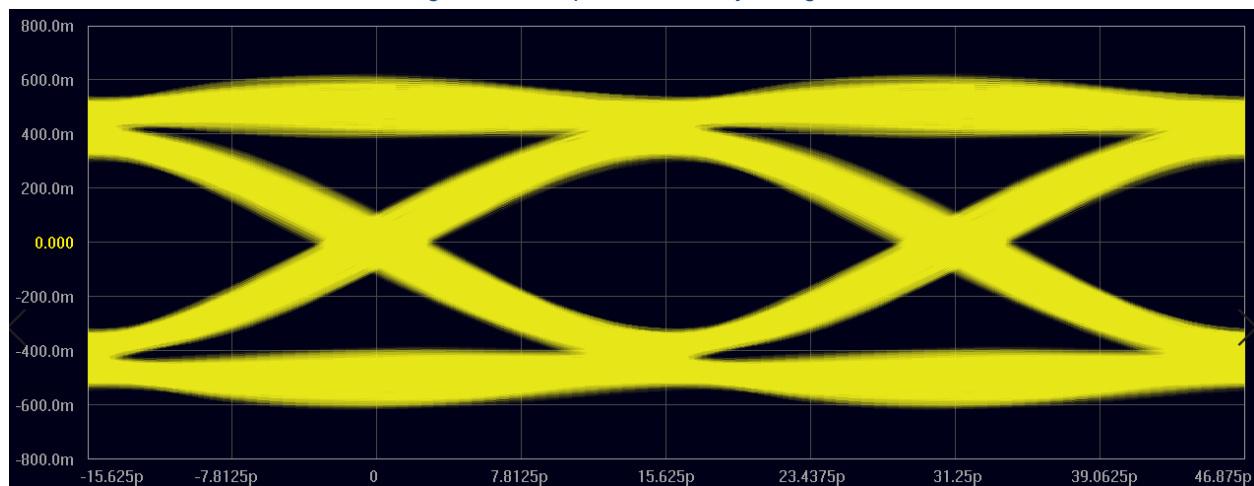


Figure 2 32 Gbps OUT2 ON Eye Diagram

Channel	Bit rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Jitter _{p-p} (ps)	Rise Time (ps)	Fall Time (ps)
OUT1	32	484.5	23.3	5.96	23.8	23.9
OUT2	32	538.1	23.2	5.86	23.4	23.5

Figure 3 32 Gbps Eye-Diagram Measurements

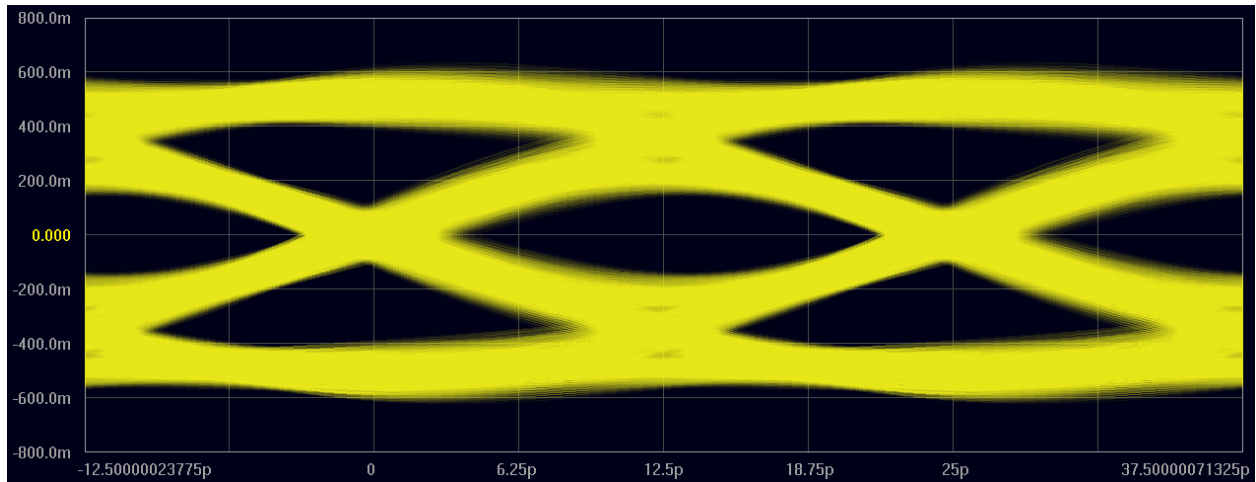


Figure 4 40 Gbps OUT1 ON Eye Diagram

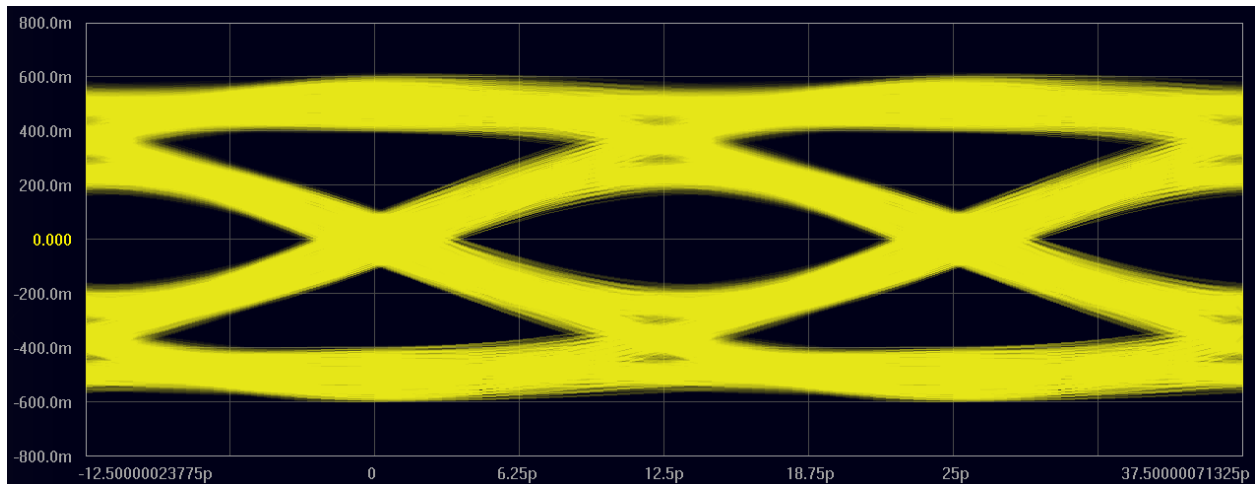


Figure 5 40 Gbps OUT2 ON Eye Diagram

Channel	Bit rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Jitter _{p-p} (ps)	Rise Time (ps)	Fall Time (ps)
OUT1	40	127.8	16.4	6.95	19.7	19.7
OUT2	40	167.6	15.9	6.72	19.4	19.5

Figure 6 40 Gbps Eye-Diagram Measurements



Figure 7 Single-ended Insertion Loss / S21

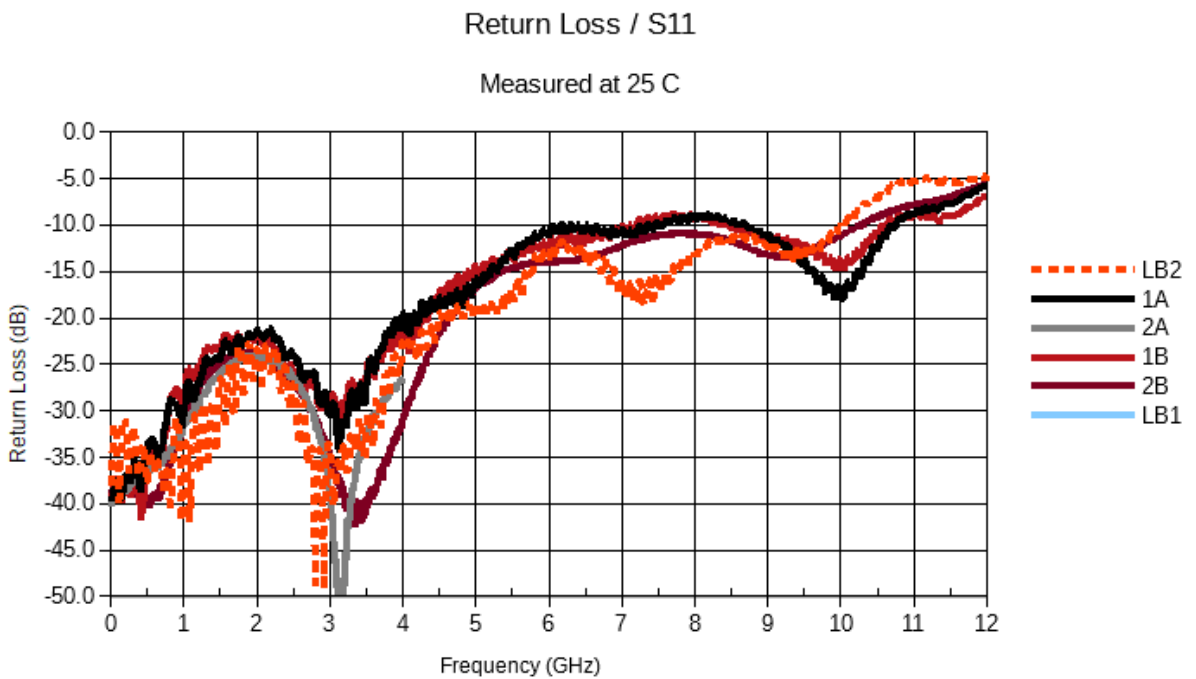


Figure 8 Single-ended Return Loss / S11

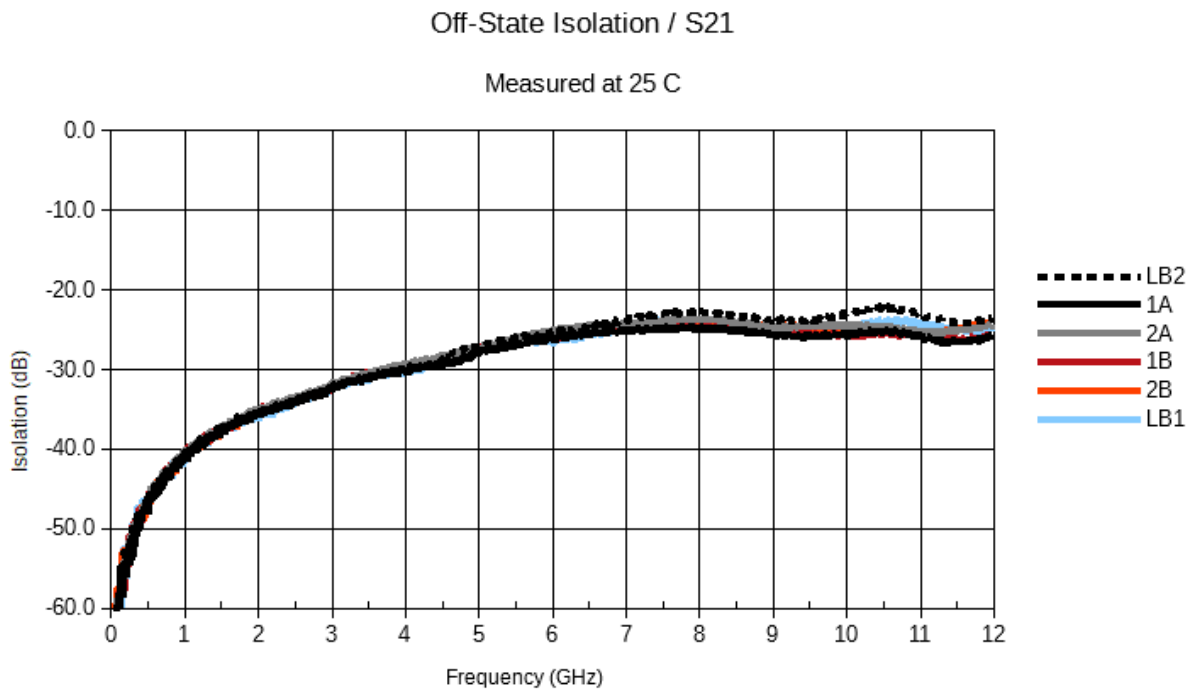


Figure 9 Single-ended Isolation / S21

Table 3 DC and AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
On / Off Switching Time				
Turn on time		8	15	μ s
Turn off time		2	5	
Settling Time				
Settling time: on		8.5	16	μ s
Settling time: off		2.5	6	
On / Off Switch Operations	3×10^9	30×10^9		Cycles
DC Steady State Switch Carry Current			250	mA
Off-State Leakage Current at 30 V_{DC}	3			
Off-State Leakage Current at 3.3V_{DC}¹⁰		1		nA
On-State Resistance (R_{on})		1.2	3.0	Ω
Off-State Resistance (R_{off})	12 G			Ω
Driver Logic Supply Voltage (V_{DD})	4.5	5.0	5.5	V
Driver Logic Supply Current (I_{DD})¹¹			4	mA
Driver Input				
High-Level Logic Voltage V _{IH}	VDD-0.9V		VDD	V
Low-Logic Input Voltage V _{IL}	0		0.9	V
High-Logic Input Current I _{IH}			10	μ A
Low-Logic Input Current I _{IL}			-350	μ A
Driver Output				
High-Level Logic Output V _{OH} ¹²	VDD – 1V			V
Low-Level Logic Output V _{OL} ¹³			1	
High-Voltage Bias Supply Voltage (V_{BB})¹⁴	88	89	90	V _{DC}
High-Voltage Bias Supply Current (I_{BB})¹⁵			TBD	μ A

¹⁰ Not measured but guaranteed by design.¹¹ Measured at F_{clk} = 8 MHz, LE = LOW.¹² V_{OH} measured at I_{DOUT} = -0.1 mA.¹³ V_{OL} measured at I_{DOUT} = -0.1 mA.¹⁴ Note that High-Voltage Bias must be applied to V_{BB}. It is not part of the integrated driver.¹⁵ Measured at V_{BB} = 100V and no load.

Hot Switch Restrictions

The MM5600 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V. Further, the voltage at the switch terminals must be within +/-0.5 V relative to RF ground.

Floating Node Restrictions

RF pins must not be allowed to electrically float during switch operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples are:

- Unconnected RF pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats RF pin, shunt with DC path to ground.

See Menlo Micro application note **Avoiding Floating Nodes** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Table 4 Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	0		8	MHz
Clock Width High and Low t_{WL}, t_{WH}	62			ns
Data Setup Time before Clock Rises t_{SU}	15			ns
Data Hold Time after Clock Rises t_H	30			ns
Latch Enable Pulse Width t_{WLE}	80			ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	35			ns
Latch Enable Setup Time before Clock Rises t_{SLE}	40			ns
Delay Time Clock to Data Low to High t_{DLH}			110	ns
Delay Time Clock to Data High to Low t_{DHL}			110	ns
All Logic Inputs t_r, t_f			5	ns

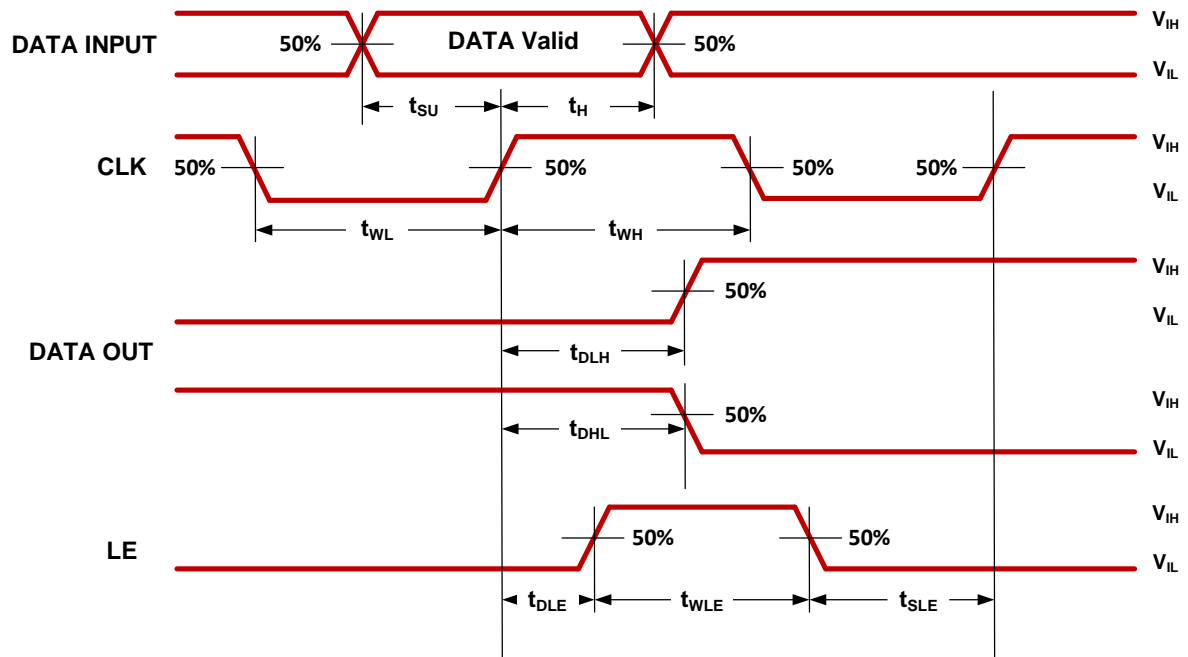


Figure 10: Driver Interface Timing Diagram

Functional Block Diagram

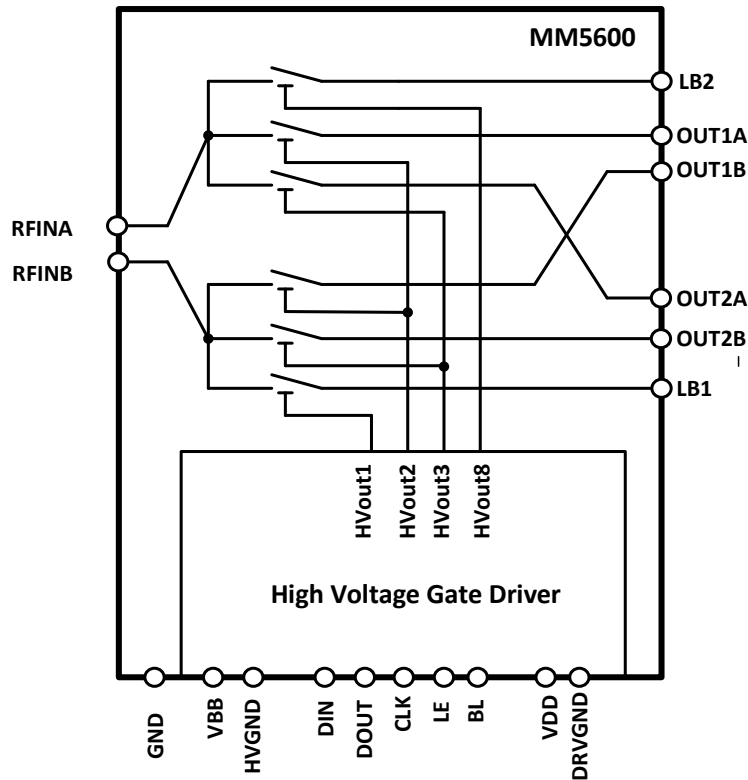


Figure 11: Functional Block Diagram

Package / Pinout Information

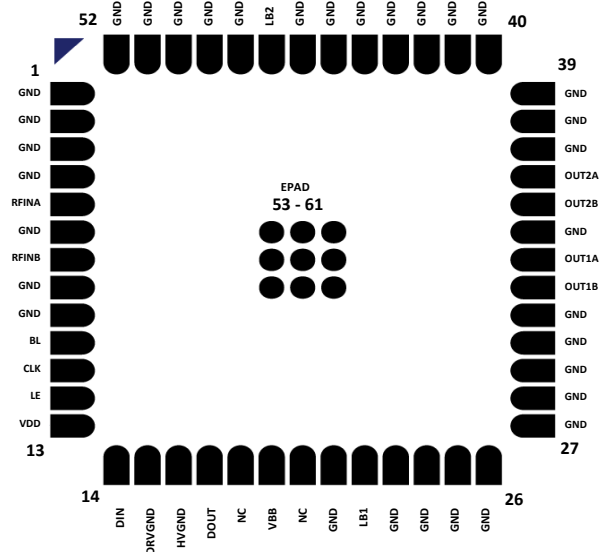


Figure 12: Top-Down Pin Layout

See Table 5 below for detailed pin description.

Table 5 Detailed Pin Description

Pin #	Pin Name	Description
1,2,3,4,6,8,9,21,23,24,25,26,27,28,29,30,31, 34,37,38,39,40,41,42,43,44,45,46,48,49,50, 51,52	GND	RF Ground
53,54,55,56,57,58,59,60,61	EPAD	Tie these pins to GND
15	DRVGND	Driver Ground
16	HVGND	High Voltage Ground
11	CLK	Clock
10	BL	Blank
12	LE	Latch Enable
18,20	NC	No Connect
14	DIN	Data In
17	DOUT	Data Out
19	V _{BB}	High Voltage Supply
13	V _{DD}	Logic Supply Voltage
5	RFINA	Differential Input A
7	RFINB	Differential Input B
33	OUT1A	Differential Output 1A
32	OUT1B	Differential Output 1B
36	OUT2A	Differential Output 2A
35	OUT2B	Differential Output 2B
22	LB1	Single-ended Output 1
47	LB2	Single-ended Output 2

High Voltage Gate Driver Control

Operating Description

The integrated high voltage gate driver is controlled through a serial-to-parallel interface that drives the high voltage gate lines of the switches. Switch control data is shifted into an 8-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 13 below.

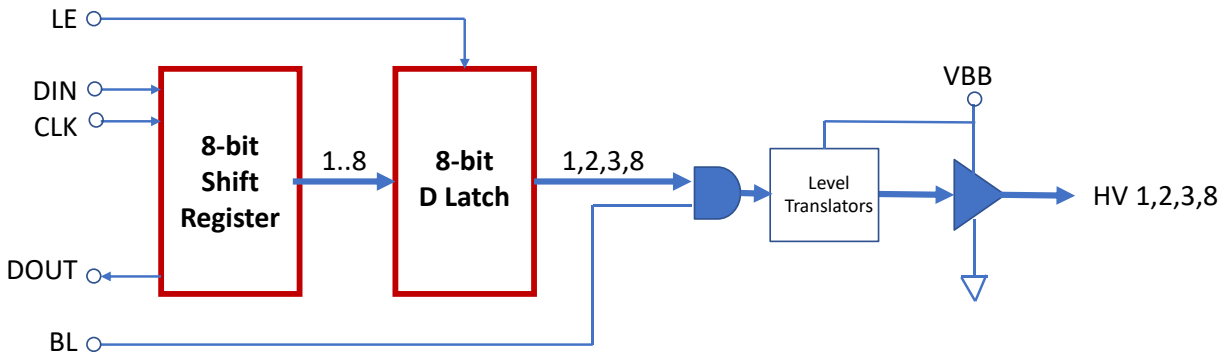


Figure 13: High Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- An 8-bit data byte is serially loaded into shift register bits 1-to-8 on the positive edge of CLK. Shift order is MSB first starting with bit 8.
- Parallel data from the shift register is transferred to the high voltage gate output buffers through an 8-bit D latch when the latch enable input LE is logically high. Transparent mode occurs when LE is held high while shifting data into the shift register.
- The MM5600 uses only four of the eight data bits latched for switch control. Bits 1, 2, and 3 and 8 correspond to high voltage gate lines HV1, HV2, HV3, and HV8 respectively. Bits 4, 5, 6 and 7 are not used. Data bits set to logical “1” close the corresponding switch to On and “0” open the switch to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 8-bit bytes consisting of 4 dummy bits and 4 switch control bits so that each byte controls one switch.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically low. The pin should be logically high for normal operation.
- Pins BL and LE have internal 20K ohm pull-up resistors to VDD. If blanking is not used, BL may be unconnected.

Table 6 Truth Function Table

Function	Inputs				Shift Register		High Voltage Output HVx			
	Data	CLK	LE	BL	1	2...8	1	2	3	4...8
All off (blank)	X	X	X	L	*	*...*	L	L	L	----L
Load Shift Register	H/L	↑	L	H	H/L	*...*	*	*	*	----*
Latched	X	X	L	H	*	*...*	*	*	*	----*
Transfer	H/L	X	H	H	H/L	*...*	H/L	*	*	----*

Note:

H = High logic level

L = Low logic level

X = Don't care logic level

↑ = Low to high logic transition

* = Dependent on the previous stage's state before the last CLK or last LE high

Each switch is individually controllable. In Table 7 below, primary usage states are highlighted in **bold**. Multiple branches may be closed simultaneously, however RF performance is not specified for such states. Note that On= Closed, Off = Open.

Table 7 Applied Gate Voltage vs. RF Switch States

HV1	HV2	HV3	HV8	RFINA - OUT1A	RFINA - OUT2A	RFINA - LB1	RFINB - OUT1B	RFINB - OUT2B	RFINB - LB2
0	0	0	VBB	Off	Off	Off	Off	Off	On
0	0	VBB	0	Off	On	Off	Off	On	Off
0	VBB	0	0	On	Off	Off	On	Off	Off
VBB	0	0	0	Off	Off	On	Off	Off	Off
0	0	0	0	Off	Off	Off	Off	Off	Off
Other valid states									
0	0	VBB	VBB	Off	On	Off	Off	On	On
0	VBB	0	VBB	On	Off	Off	On	Off	On
0	VBB	VBB	0	On	On	Off	On	On	Off
VBB	0	0	VBB	Off	Off	On	Off	Off	On
VBB	0	VBB	0	Off	On	On	Off	On	Off
VBB	VBB	0	0	On	Off	On	On	Off	Off
VBB	VBB	0	VBB	On	Off	On	On	Off	On
VBB	VBB	VBB	0	On	On	On	On	On	Off
VBB	VBB	VBB	VBB	On	On	On	On	On	On
0	VBB	VBB	VBB	On	On	Off	On	On	On
VBB	0	VBB	VBB	Off	On	On	Off	On	On

Package Drawing

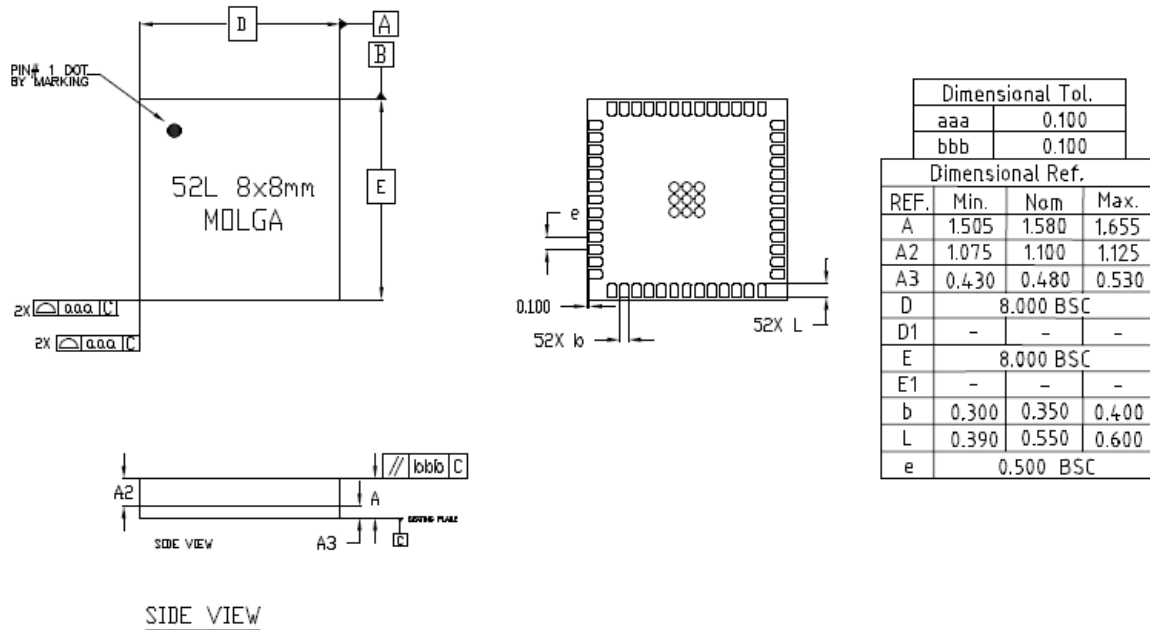


Figure 14 Package Drawing

Recommended PCB Layout

- PCB lands should be as shown in the pad pattern diagram
- Connect GND pins (floating shield inside the package) to RF Signal Ground
- Open space around the package can have grounded thru holes
- ENIG (Electroless Nickel Immersion Gold) pad surface finish
- 20 micron (μm) thick solder mask
- Type 3 or higher solder paste with no clean flux
- Component placement force not to exceed 100 grams

Recommended Solder Reflow Profile

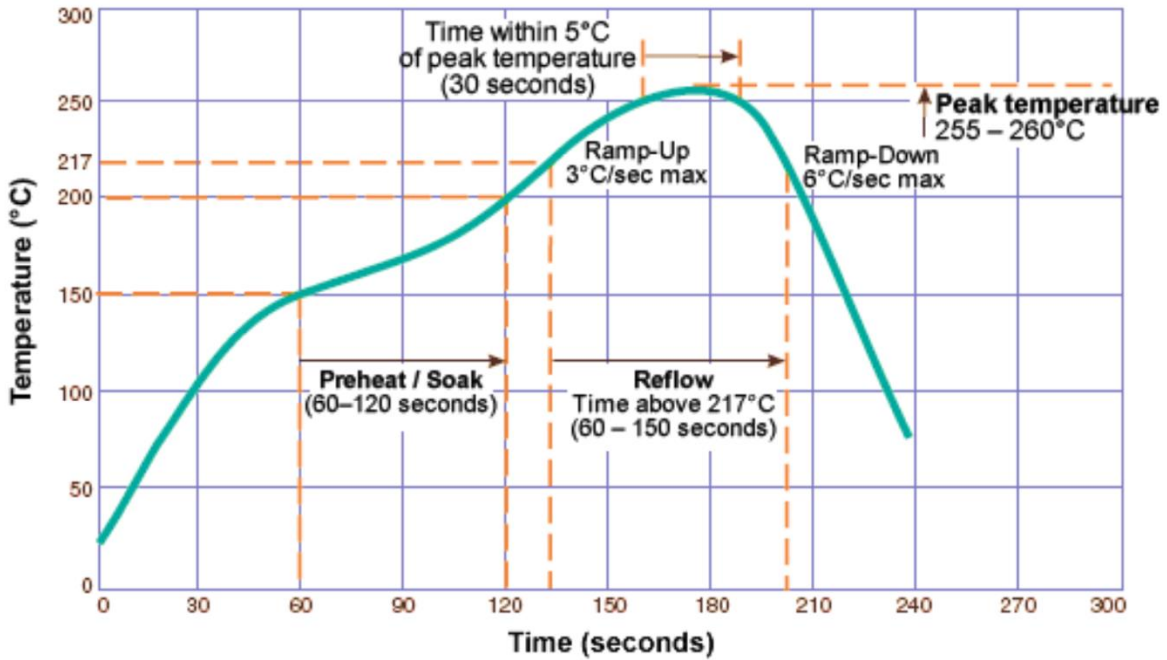


Figure 15 Reflow Profile

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.



Package Options and Ordering Information

Part Number	ECCN	Package	Temperature Range
MM5600-01	EAR99	DC-20GHz/40Gbps - DPDT - 8mm x 8mm LGA (for semi test/ATE applications)	-40°C to +85°C
MM5600-EVK1	EAR99	Evaluation board for MM5600 (differential DPDT, w/Southwest SMA connector-QTY-8) DC-20GHz/40Gbps - 8mm x 8mm LGA	
MM5600-EVK2	EAR99	Evaluation board for MM5600 (single-ended mode, w/Rosenberger SMA connector-QTY-8) DC-12GHz - 8mm x 8mm LGA	

Important Information

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Contact Information

Please contact Menlo Micro for the latest specifications, additional product information, test and evaluation boards, product samples, worldwide sales and distribution locations:

Internet: www.menlomicro.com

E-mail: sales@menlomicro.com

For product technical questions and application information: support@menlomicro.com.