MM5620

POWERED BY ideal switch®

64 Gbps Dual DP3T Switch with Loopback

RoHS COMPLIANT

Product Overview

Description

The MM5620 is a differential dual DP3T switch supporting the high-speed differential signal switching required in the latest PCIe Gen 5, Gen 6, SerDes, and other standards. The MM5620 is based on Menlo's Ideal Switch® technology and can operate at 64 Gbps with a bandwidth of 20 GHz for high-performance applications. The MM5620 has low insertion loss, fast switching speed, and can operate with greater than 3 billion switching cycles. The MM5620 system-in-package (SiP) solution fully integrates the switch driver and charge pump controlled through SPI or GPIO interfaces by a host processor. In addition, integrated loopback capacitors provide significant board footprint reduction for high-volume production test solutions. The MM5620 switch provides high data rate for full high-speed differential data applications with unprecedented levels of parallel testing for space-constrained final test and probe test. Applications include chip testing for smartphones, graphics, and network processors, as well as microprocessor, accelerator, and high-speed memory products.

Features

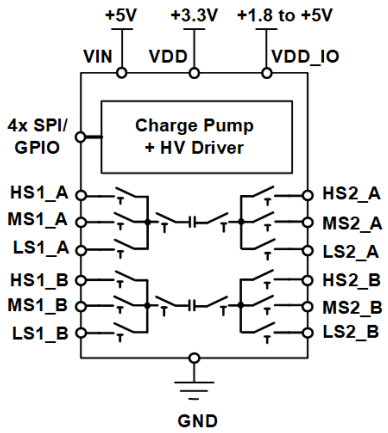
- DC to 20 GHz range
- Dual 2 Form C, DP3T (differential mode) with Loopback Mode
- Normally Open, Reflective actuator
- Low Insertion Loss: -1.5 dB @ 16 GHz
- Integrated charge pump and driver eliminates the requirement for external biasing and driver circuitry
- Built-in AC Coupling Capacitors
- Fully controllable ports for low, medium, and high data rate signal routing
- High Reliability: Greater than 3 billion switching operations
- 8.2 x 8.2 mm LGA Package

Markets

- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Test
- Compliance and Loopback Test

Applications

- High-Speed Data Digital Component Testing
- Optical-Electrical Module Testing
- High-Speed Signal Routing
- ATE Device Interface Boards
- Optical-Electrical Module Testing
- Differential Switch Matrices



Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM5620 should be restricted to the limits indicated in the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM5620 is a Class 0 ESD device. When handling the MM5620, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
DC Supply Voltage	V_{DD}	-0.3	3.6	V
I/O Supply Voltage	V_{DD_IO}	-0.3	5.5	V
Charge Pump Input	V_{IN}	-0.3	5.5	V
Driver Logic Input Levels		-0.3	V_{DD_IO} + 0.3	V
Max Input Voltage Level (RF Pins)[4,8]		—	3.3	V
Hot Switching Voltage @ 0.5 V[1, 2]		-0.5	0.5	V
Storage Temperature Range[3]		-65	150	ºC
ESD Rating HBM RF Pins[4]		—	150	V
ESD Rating HBM Control and Power Pins[5]		—	2000	V
ESD Rating HBM VPP Pin		—	500	V
Mechanical Shock[6]		—	500	G
Vibration[7]		—	500	Hz

Notes:

1. For hot-switching, differential voltage across switch terminals must be less than or equal to 0.5 V and each switch port must be within +/-0.5 V of RF ground. See section Hot Switch Restrictions.
2. RF pins must not be allowed to electrically float during switch operation. See section Floating Node Restrictions for details on avoiding floating nodes.
3. See section Storage and Shelf Life more information on shelf and floor life.
4. RF pins include: HS1_x, HS2_x, MS1_x, MS2_x, LS1_x, LS2_x.
5. Control and power pins include: VIN, VDD, VDD_IO, PULL_UP, FLT_MODE, FLTB, FLIP_BIT, SCK/CTL1, MOSI/CTL2, MISO/CTL3, SSB/CTL4, CP_EN.
6. See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis.
7. See JESD22-B103 for vibration test methodology at 3.1 G and 30min/cycle, 1 cycle/axis, 3 axis.
8. Maximum RF input power is 20dBm into 50 ohms.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Charge Pump Power Supply	V_{IN}	4.75	5.5	V	
Driver Logic Supply Voltage	V_{DD}	3.0	3.6	V	
Logic Reference Level (VDD_IO)	V_{DD_IO}	1.71	5.25	V	
Operating Temperature	T_A	-40	85	°C	Ambient
Switch Cycle Frequency		—	100	Hz	

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted. Operating with all analog and digital GND pins connected to system ground (0 V).

Table 3. RF Performance Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Operating Frequency Range		DC	—	20	dB	
Differential Insertion Loss						
HS1 to HS2	SDD_{21}	—	1.5	—	dB	@ 16GHz, De-Embedded
MS1 to MS2		—	2.0	—	dB	@ 16GHz, De-Embedded
LS1 to LS2		—	3.0	—	dB	@ 3GHz, Not De-Embedded
HS1 to MS1		—	1.4	—	dB	@ 16GHz, De-Embedded
HS2 to MS2		—	1.4	—	dB	
HS1 to LS1		—	2.9	—	dB	@ 6 GHz, Not De-Embedded
HS2 to LS2		—	2.9	—	dB	
MS1 to LS1		—	3.1	—	dB	
MS2 to LS2		—	3.1	—	dB	
Differential Return Loss						
HS1 to HS2	SDD_{11}	—	28	—	dB	@ 16GHz, De-Embedded
MS1 to MS2		—	23	—	dB	@ 16GHz, De-Embedded
LS1 to LS2		—	27	—	dB	@ 3GHz, Not De-Embedded
HS1 to MS1		—	13	—	dB	@ 16 GHz, Not De-Embedded
HS2 to MS2		—	12	—	dB	
HS1 to LS1		—	23	—	dB	@ 6 GHz, Not De-Embedded
HS2 to LS2		—	23	—	dB	
MS1 to LS1		—	25	—	dB	
MS2 to LS2		—	25	—	dB	

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Differential Isolation	SDD_{12}					
HS1 to HS2		—	67	—	dB	@ 16GHz, De-Embedded
MS1 to MS2		—	47	—	dB	@ 16GHz, De-Embedded
LS1 to LS2		—	56	—	dB	@ 3GHz, Not De-Embedded
HS1 to MS1		—	41	—	dB	@ 16GHz, De-Embedded
HS2 to MS2		—	40	—	dB	
HS1 to LS1		—	49	—	dB	@ 6 GHz, Not De-Embedded
HS2 to LS2		—	49	—	dB	
MS1 to LS1		—	50	—	dB	
MS2 to LS2		—	50	—	dB	

Signal Integrity Differential Performance

Test conditions for the differential PAM4 eye-diagram performance measurements are listed below:

- Analyzed with Physical Layer Test System (PLTS) 2023
- Peak to peak input amplitude: 500 mVpp
- Measurements performed at 64 Gbps
- Signal path: (Figure 1) HS1 to HS2, (Figure 2) MS1 to MS2
- Tests performed at ambient temperature

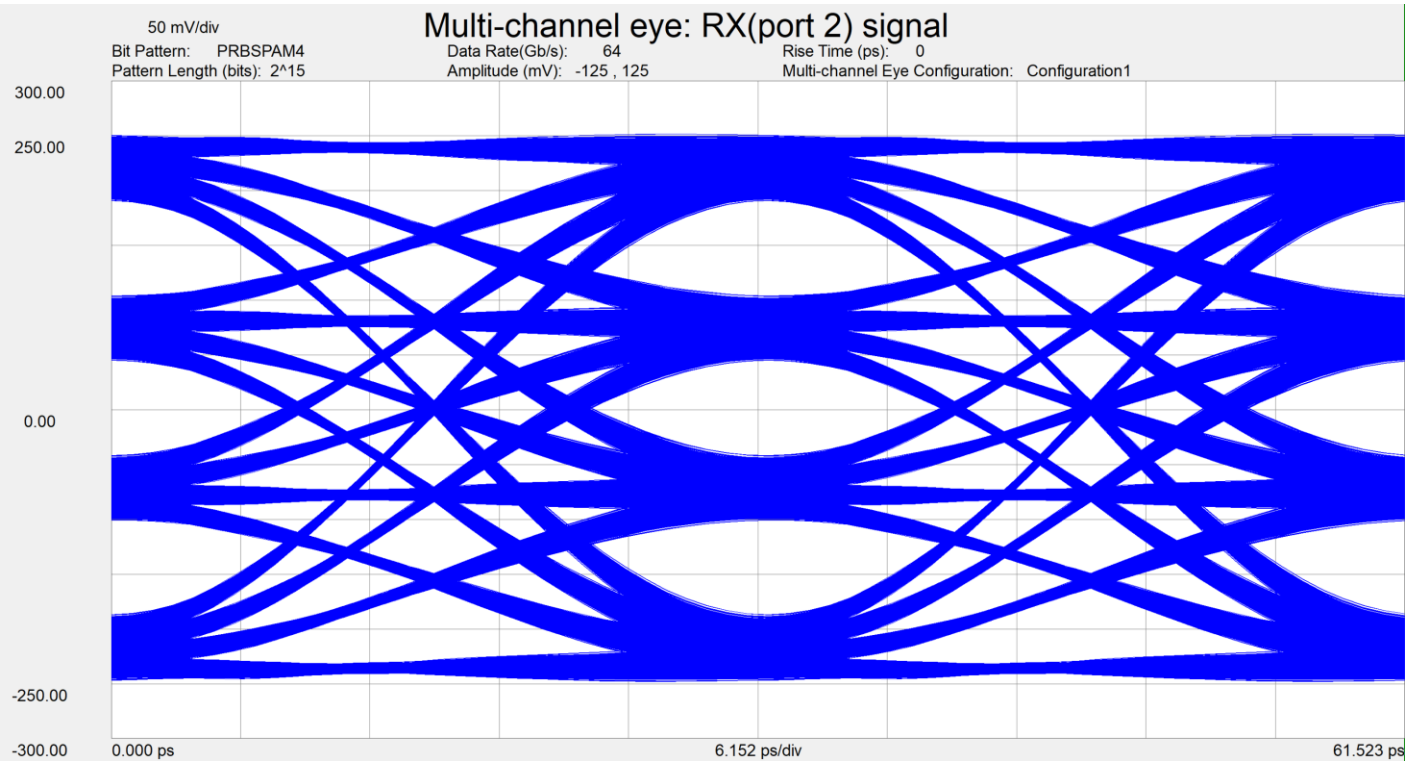


Figure 1. HS1-HS2 Differential PAM4 Eye Diagram

Table 4. HS1-HS2 Differential PAM4 Eye-Diagram Performance

Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	64	83.6	11	10.2
1/2	64	84.2	13	8.5
2/3	64	84.2	11	10.4

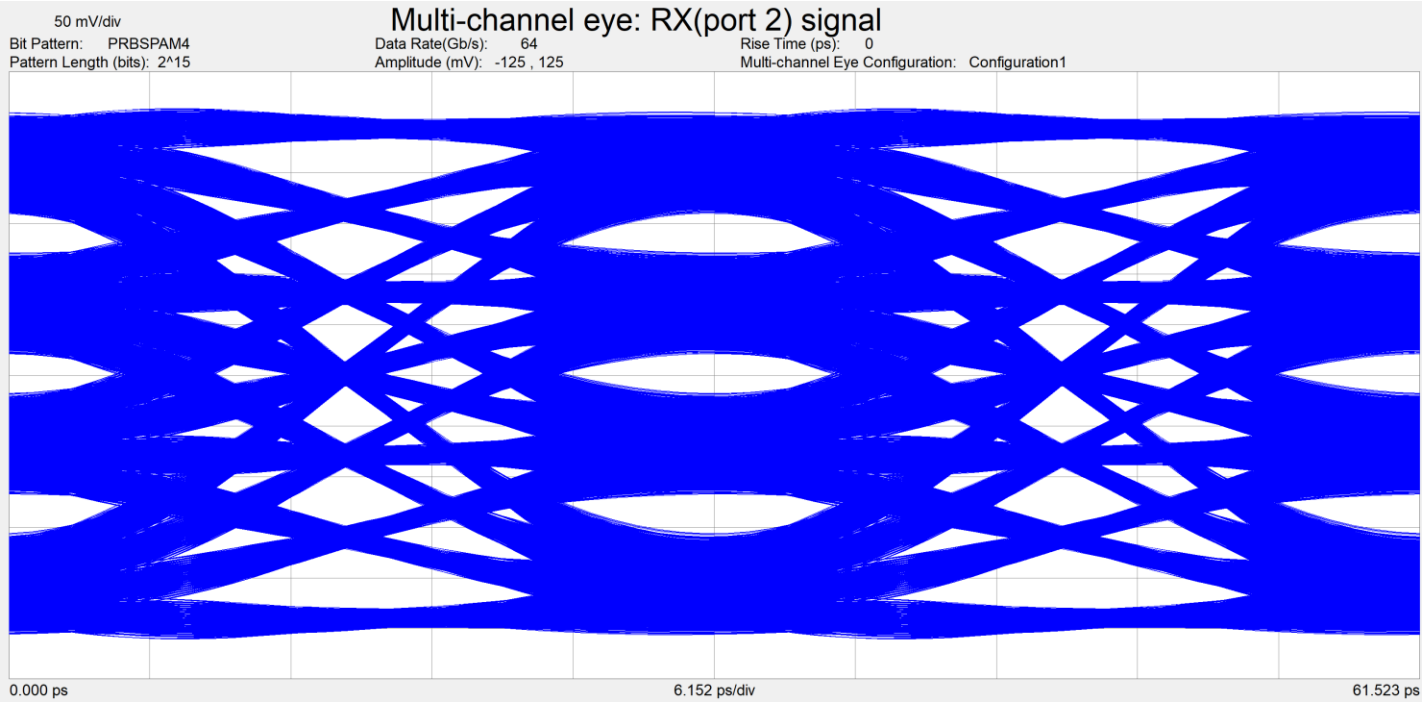


Figure 2. MS1-MS2 Differential PAM4 Eye Diagram

Table 5. MS1-MS2 Differential PAM4 Eye-Diagram Performance

Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	64	35.8	7	15.65
1/2	64	35.9	9	17.34
2/3	64	36.0	7	16.45

Table 6. Switch DC and AC Electrical Characteristics[1]

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
On / Off Switching						Includes settling time.
Settling time: on		—	26.5	—	µs	
Settling time: off		—	9	—	µs	
On / Off Switch Operations[2]		3x10^9	—	—	Cycles	Specified at 25°C ambient.
Off-State Leakage Current at 30V_{DC}		—	7	60	nA	
On-State Resistance[3]	R_{ON}	—	1.7	4.0	Ω	Specified for all DC-coupled paths.

Notes:

1. DC measurements were performed in single-ended configuration.
2. Predicted number of operation cycles as observed on a sample size of 75 units, 100Hz cycle rate, and room temperature with Hot Switch Restrictions.
3. Measured at 30mA, DC.

Table 7. Power Supply Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Charge Pump Power Supply	V_{IN}	4.75	5.0	5.5	V	
VIN Current (Dynamic)[1]	I_{VIND}	—	1.7	2.75	mA	SPI mode, All CH switching at 100Hz
VIN Quiescent Current	I_{VINQ}	—	1.65	2.25	mA	Charge Pump On, All I/O and Channels Static
Low Voltage Logic Supply	V_{DD}	3.0	3.3	3.6	V	
VDD UVLO Rising Threshold	$UVLO_{RISE}$	2.77	—	2.95	V	
VDD UVLO Falling Threshold	$UVLO_{FALL}$	2.72	—	2.90	V	
Low Voltage Digital Current[1]	I_{DD}	—	520	700	µA	SPI mode, All CH Switching at 100Hz
Low Voltage Digital Quiescent Current	I_{DDQ}	—	480	550	µA	Charge Pump On, All I/O & Channels Static
Low Voltage Digital Sleep Mode Current	$I_{DDSLEEP}$	—	<1	10	µA	Charge Pump Off, SPI and Inputs in Static State
Logic Reference Level	V_{DD_IO}	1.71	—	5.25	V	
I/O Logic Supply Current	I_{DD_IOQ}	—	<10	50	uA	All Channels Switching at 100Hz

Notes:

1. Specification is obtained by characterization.

Table 8. Digital Interface AC and DC Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Logic I/O Level High	I/O_{VH}	0.7 x V_{DD_IO}	—	V_{DD_IO}	V	
Logic I/O Level Low	I/O_{VL}	0	—	0.3 x V_{DD_IO}	V	
Logic I/O Hysteresis (SCK only)[1]	I/O_{VH}	—	0.25	—	V	
Digital Input Capacitance	C_{IN}	—	2	5	pF	
SDO Load Capacitance[2] [3]	C_{SDO}	—	—	10	pF	
SDO Source Current @ VDD_IO[1]:	I_{SDOH}					VOUT = 0.8 x VDD_IO
5 V		180	290	—	mA	
3.3V		75	140	—	mA	
1.8V		20	35	—	mA	
SDO Sink Current @ VDD_IO[1]:	I_{SDOL}					VOUT = 0.2 x VDD_IO
5.0 V		140	260	—	mA	
3.3 V		65	140	—	mA	
1.8 V		20	40	—	mA	
Pull down resistor at SDI, SCK, SSB, CP_EN, FLIP_BIT, MODE, and FLT_MODE pins	R_{PD}	120	200	280	kΩ	SSB pull down is only in GPIO mode
CP_EN pin toggle low time	T_{TOGGLE}	500	—	—	ns	Minimum time CP_EN has to be held low to restart the IC from fault condition
FLTB pin max sink current[1]		65	140	—	mA	FLTB = GND VDD_IO=3.3V

Notes:

1. Specification is obtained by characterization.
2. Specification is for design guidance only.
3. SDO load capacitance = input capacitance of SDI pin + trace capacitance from SDO to SDI

Table 9. Digital Interface Timing Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
SPI Clock Frequency	SCK	—	—	33	MHz	
SDI Valid to SCK Setup Time[1]	t_{SU}	2	—	—	ns	
SDI Valid to SCK Hold Time[1]	t_{HD}	5	—	—	ns	
SCK High Time[1]	t_{HI}	15.5	—	—	ns	
SCK Low Time[1]	t_{LO}	15.5	—	—	ns	
SSB Pulse Width[1]	t_{CSH}	15	—	—	ns	
LSB SCK to SSB High[1]	t_{CSHLD}	15	—	—	ns	
SSB Low to SCK High[1]	t_{CSSU}	15	—	—	ns	
SDO Propagation Delay from SCK Falling Edge[1]	t_{SDOH}	10	—	—	ns	
SDO Output Valid after SSB Low[1]	t_{CSDO}	20	—	—	ns	
SSB Inactive to SDO High Impedance[1]	t_{SDOZ}	—	—	10	ns	

Notes:

1. Specification is obtained by characterization.

Table 10. Charge Pump and Driver Specifications

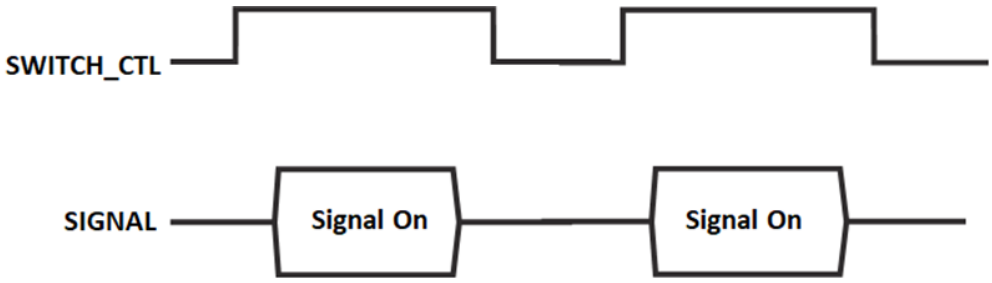
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Power-On-Reset[1]	POR	—	1.25	2.5	ms	Time for logic input signals to be considered valid after application of VIN and VDD.
Start-Up Time	T_{ST}	—	20	33	ms	CP_EN=1 (CPEN bit=1) to VPP rises to 90% of set value

Notes:

1. Specification is for design guidance only.

Hot Switch Restrictions

The MM5620 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V. Further, the voltage at the switch terminals must be within +/-0.5 V relative to signal ground.



Floating Node Restrictions

RF pins must not be allowed to electrically float during switch operation and therefore require some form of DC path to ground to prevent charge accumulation. The MM5620 uses the superport configuration for improved high frequency performance. See Menlo Micro application note ***Avoiding Floating Nodes*** for a detailed explanation of the hazard conditions to avoid and recommended solutions.

Functional Block Diagram

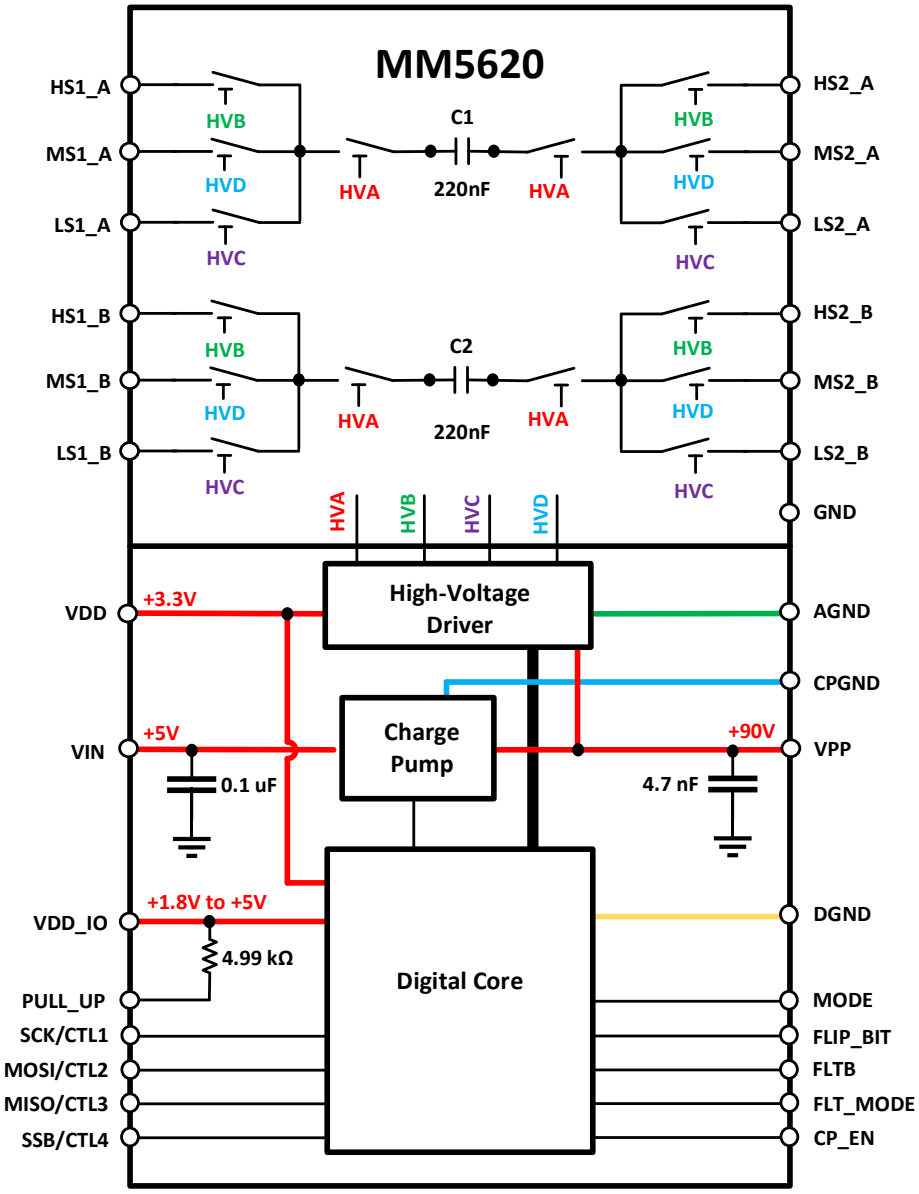


Figure 3. Functional Block Diagram

Note: C1 and C2 are 220 nF internal capacitors.

Package / Pinout Information

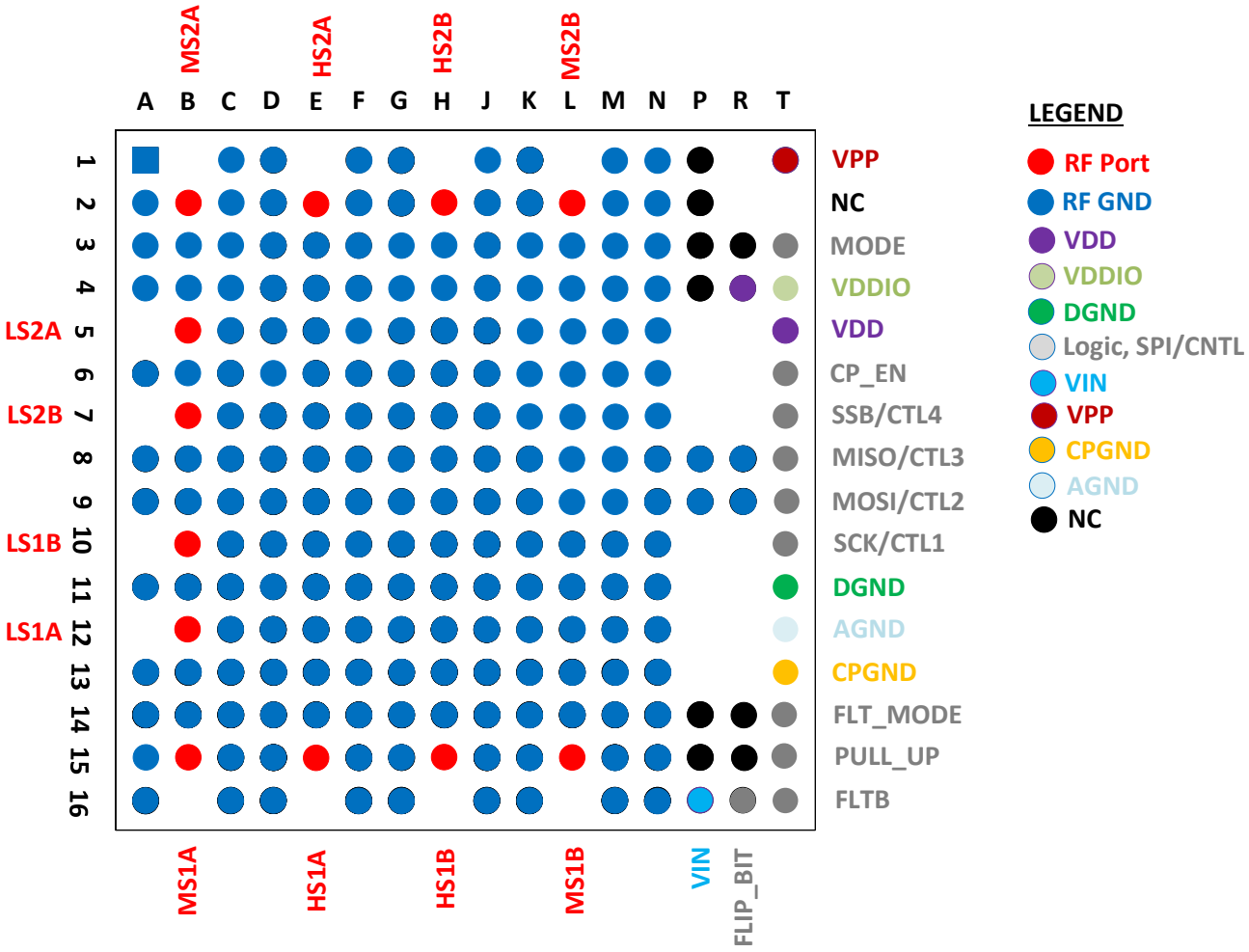


Figure 4. Package Pinout (Top View/As Mounted)

See Table 11 for detailed pin descriptions.

Table 11. Detailed Pin Description

Pin Name	Pin #	Description
HS1A	E15	Port 1A of the high-speed signal path. Can be used as an input or an output.
HS1B	H15	Port 1B of the high-speed signal path. Can be used as an input or an output.
MS1A	B15	Port 1A of the medium-speed signal path. Can be used as an input or an output.
MS1B	L15	Port 1B of the medium-speed signal path. Can be used as an input or an output.
LS1A	B12	Port 1A of the low-speed signal path. Can be used as an input or an output.
LS1B	B10	Port 1B of the low-speed signal path. Can be used as an input or an output.
HS2A	E2	Port 2A of the high-speed signal path. Can be used as an input or an output.
HS2B	H2	Port 2B of the high-speed signal path. Can be used as an input or an output.
MS2A	B2	Port 2A of the medium-speed signal path. Can be used as an input or an output.
MS2B	L2	Port 2B of the medium-speed signal path. Can be used as an input or an output.
LS2A	B5	Port 2A of the low-speed signal path. Can be used as an input or an output.
LS2B	B7	Port 2B of the low-speed signal path. Can be used as an input or an output.
SCK/CTL1	T10	Clock input in SPI mode; RF channel control in GPIO mode. Has an internal pull-down resistor.
MOSI/CTL2	T9	SPI data input (SDI) in SPI mode; RF channel control in GPIO mode. Has an internal pull-down resistor.
MISO/CTL3	T8	SPI data output (SDO) in SPI mode; RF channel control in GPIO mode. Has an internal pull-down resistor.
SSB/CTL4	T7	Chip select in SPI mode; RF channel control in GPIO mode. Has an internal pull-up resistor in SPI mode, and an internal pull-down resistor in GPIO mode.

Pin Name	Pin #	Description
FLT_MODE	T14	Fault Mode select in GPIO mode. Fault Mode is disabled if high. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
FLTB	T16	Fault indicator in GPIO and SPI modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when a fault is detected. Can be left open if not used. Pull-up voltage must be ≤ VDD_IO.
FLIP_BIT	R16	This pin has an internal pull-down resistor. In SPI mode, this pin should be tied to VDD_IO. In GPIO mode FLIP_BIT should be tied to GND. Refer to Table 12 for more information.
MODE	T3	Logic level input to switch inputs between SPI and GPIO modes. MODE = 0 is SPI mode. MODE=1 is GPIO mode.
CP_EN	T6	Charge pump enable pin in GPIO mode. Pull-up to VDD_IO to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
VDD	R4, T5	3.3 V nominal input to digital logic and internal level translators. Bypass with a low ESR 1 µF ceramic capacitor.
VDD_IO	T4	For 3.3 V nominal digital I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). Bypass with a low ESR 1 µF ceramic capacitor if separate from VDD.
PULL_UP	T15	Connect this pin directly to the FLTB. Has a built-in 4.99 kΩ resistor to VDD_IO.
DGND	T11	Digital ground, should be connected to PCB ground.
VIN	P16	Connect to 5 V power supply. Bypass with a low ESR 1 µF ceramic capacitor.
CPGND	T13	Charge pump ground, should be connected to PCB ground.
VPP	T1	High-voltage (90V) charge pump output. Leave this pin unconnected.
AGND	T12	Analog ground, should be connected to PCB ground.

Pin Name	Pin #	Description
GND	A1,C1,D1,F1,G1,J1,K1,M1,N1, A2,C2,D2,F2,G2,J2,K2,M2,N2, A3,B3,C3,D3,E3,F3,G3,H3,J3,K3,L3,M3,N3, A4,B4,C4,D4,E4,F4,G4,H4,J4,K4,L4,M4,N4, C5,D5,E5,F5,G5,H5,J5,K5,L5,M5,N5, A6,B6,C6,D6,E6,F6,G6,H6,J6,K6,L6,M6,N6, C7,D7,E7,F7,G7,H7,J7,K7,L7,M7,N7, A8,B8,C8,D8,E8,F8,G8,H8,J8,K8,L8,M8,N8, P8,R8, A9,B9,C9,D9,E9,F9,G9,H9,J9,K9,L9,M9,N9, P9,R9, C10,D10,E10,F10,G10,H10,J10,K10,L10, M10,N10, A11,B11,C11,D11,E11,F11,G11,H11,J11, K11,L11,M11,N11, C12,D12,E12,F12,G12,H12,J12,K12,L12, M12,N12, A13,B13,C13,D13,E13,F13,G13,H13,J13, K13,L13,M13,N13, A14,B14,C14,D14,E14,F14,G14,H14,J14, K14,L14,M14,N14, A15,C15,D15,F15,G15,J15,K15,M15,N15, A16,C16,D16,F16,G16,J16,K16,M16,N16	Connect to common ground. These pins are internally connected to the RF ground reference.

RF Performance

Typical device performance, measured on MM5620 EVK at room temperature.

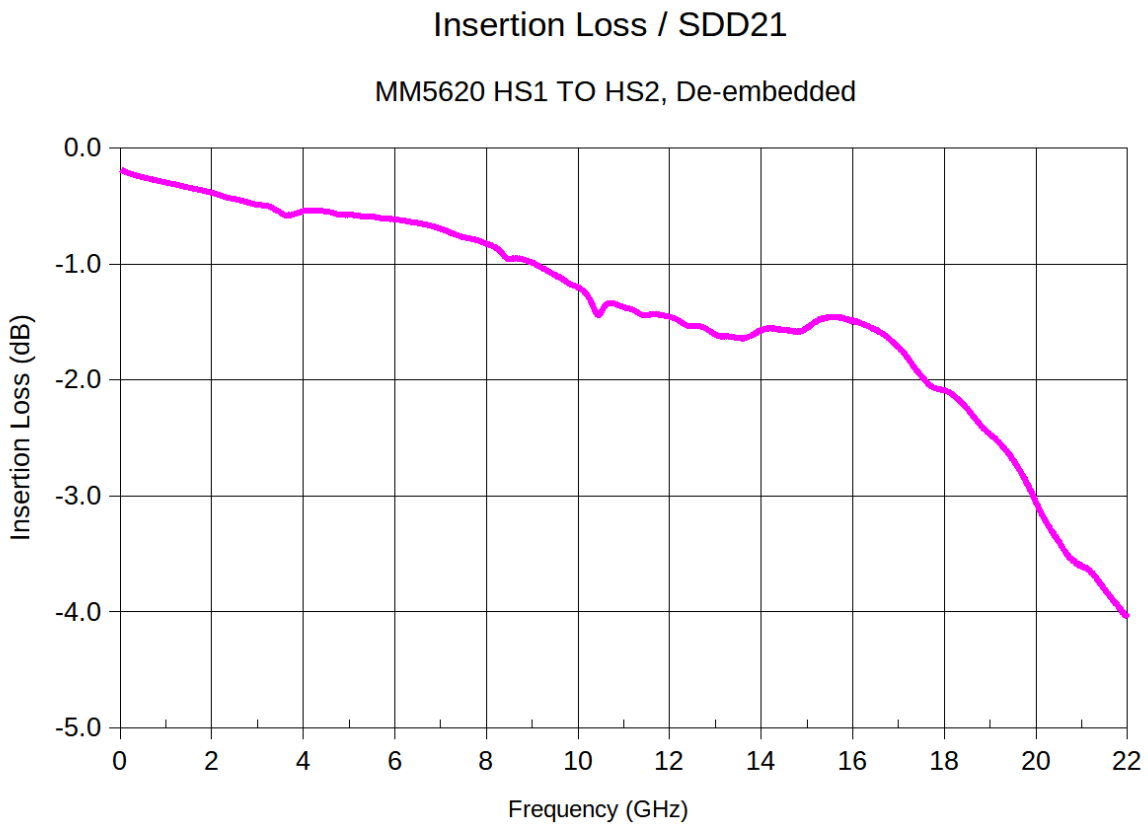


Figure 5. Insertion Loss/SDD21

Figure 6. Return Loss/SDD11

The return loss performance from 8 to 14 GHz can be improved by optimizing the PCB launch to the MM5620 device. Please contact your local Menlo Micro sales support for further information.

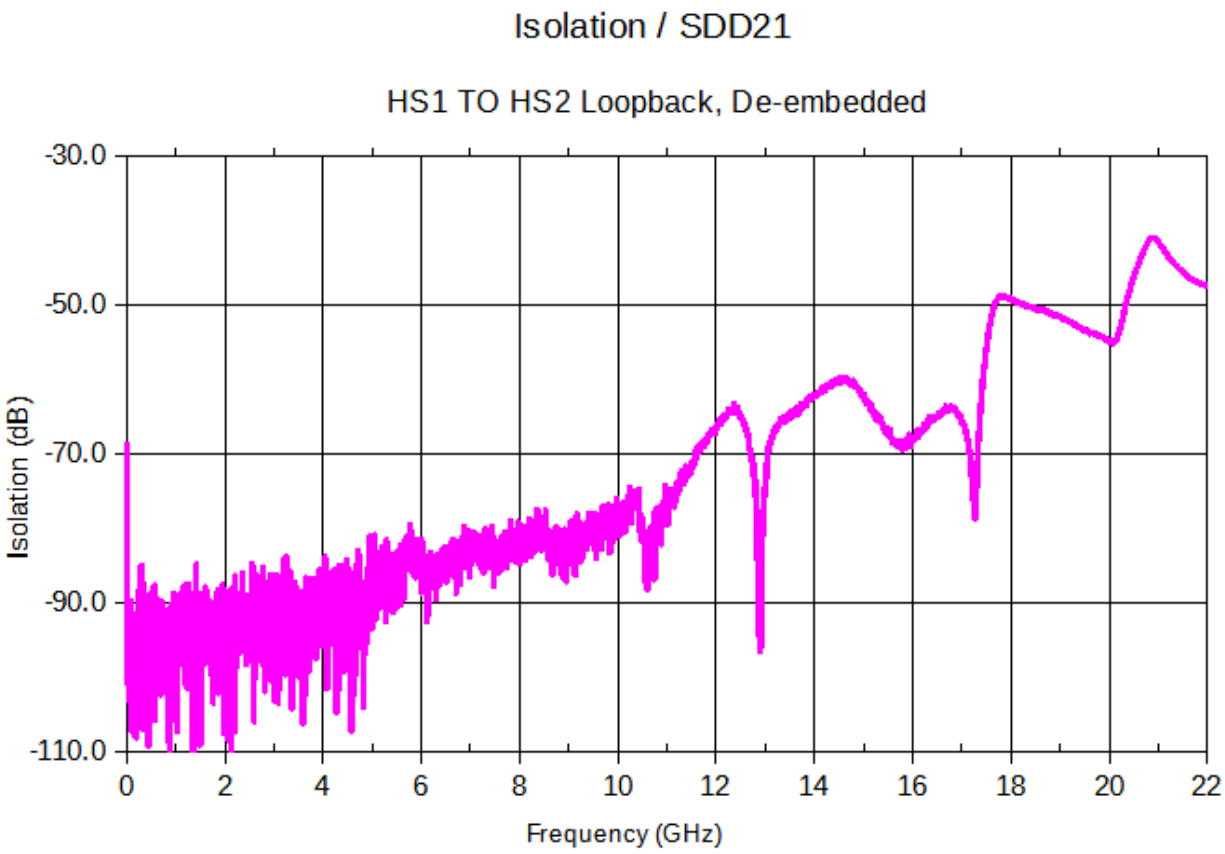


Figure 7. Isolation/SDD21

Programming

Communication Interface

The MM5620 has two modes of operation; **SPI (serial)** and **GPIO (Parallel)**, selected by the **MODE** input pin.

All the SPI pins (except SSB pin), the FLIP_BIT and the MODE pin have an internal pull-down resistor to ensure that no digital input pins is left floating.

The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is CTL4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

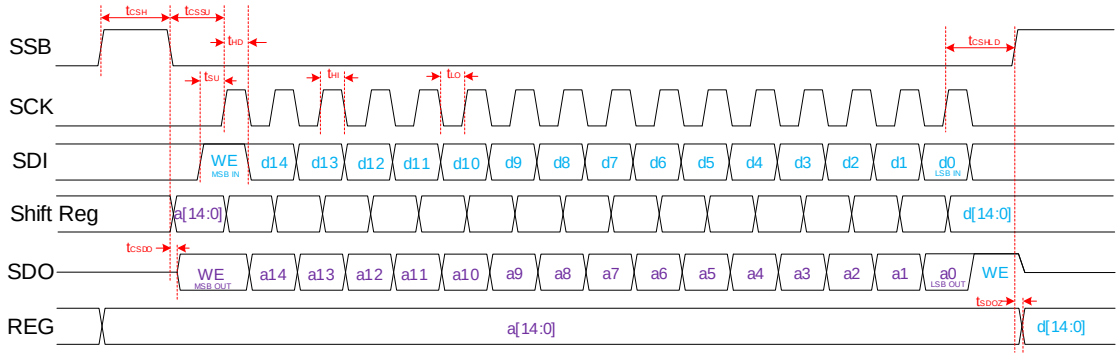


Figure 8. SPI Timing Diagram

Serial Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus (see Daisy Chain Operation, Figure 11., Figure 12, and Figure 13). The SPI works at any frequency up to a maximum of 33 MHz and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

SPI Interface Mode

SPI timing diagrams are provided in Figure 8 through Figure 13 In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data (DN) to

Target, while Target passes its previous (DN-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

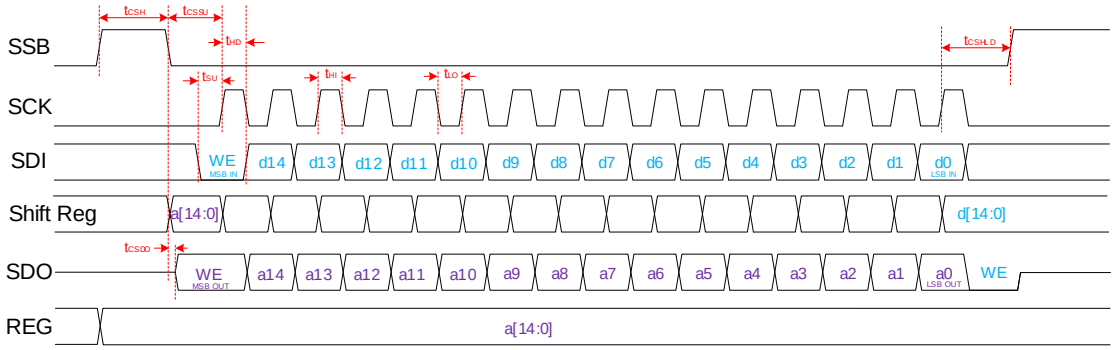


Figure 9. SPI Read Only (1 IC, No Daisy Chain)

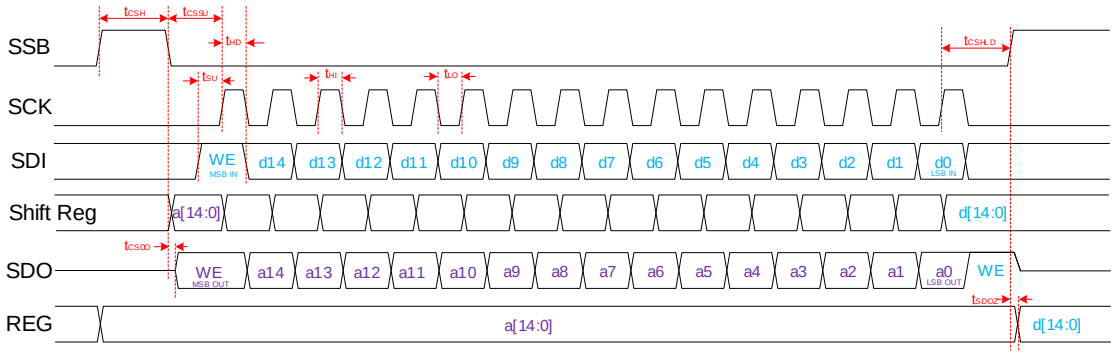


Figure 10. SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the SDO pin while clocking the SCK pin. Register STATE holds the state of the 4 internal high-voltage outputs and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high.

Register CONTROL holds four control bits (CPEN, VPPCOMP, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high. In SPI mode, the CP_EN and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	0	0	**HVD**	**HVC**	**HVB**	**HVA**
bit7							bit 0

bit 7: **Low**
Set this bit low.
bit 6: **Low**
Set this bit low.
bit 5: **Low**
Set this bit low.
bit 4: **Low**
Set this bit low.
bit 3: **HVD**
1 = HVD Output is Enabled (High)
0 = HVD Output is Disabled (Low)
bit 2: **HVC**
1 = HVC Output is Enabled (High)
0 = HVC Output is Disabled (Low)
bit 1: **HVB**
1 = HVB Output is Enabled (High)
0 = HVB Output is Disabled (Low)
bit 0: **HVA**
1 = HVA Output is Enabled (High)
0 = HVA Output is Disabled (Low)

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit7							bit 0

bit 7: WR_EN
- 1 = Enable write mode
- 0 = Disable Write mode (read only)

bit 6: FSTAT (see Note 1 below)
- 1 = VPP OR VDD Fault status = faulted
- 0 = VPP OR VDD Fault status = NOT faulted

bit 5: SLEEP
- 1 = SLEEP mode active (all analog circuits disabled)
- 0 = SLEEP mode inactive (all analog circuits enabled)

bit 4: FLTMODE
- 1 = Fault Mode Disabled (shutdown Disabled)
- 0 = Fault Mode Enabled (shutdown Enabled)

bit 3: VPPCOMP
- 1 = VPP under-voltage comparator is disabled.
- 0 = VPP under-voltage comparator is active.

bit 2: Do Not Care
- This bit can be set to either state without effecting performance.

bit 1: CPEN
- 1 = Charge Pump is enabled
- 0 = Charge Pump is disabled

bit 0: Do Not Care
- This bit can be set to either state without effecting performance.

Notes:

1. After this bit is set high, it must be written to 0 to clear the fault. If fault mode is enabled, CPEN must be toggled to restart the charge pump. See Fault Conditions for more information.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the MISO of one chip to the MOSI of the next chip in the chain, as shown in Figure 11. SPI timing diagrams with daisy-chained devices are provided in Figure 12 and Figure 13.

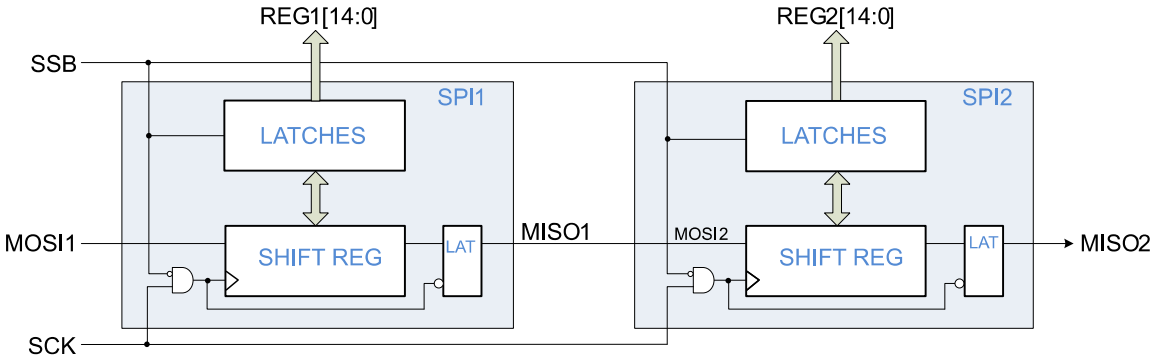


Figure 11. SPI with 2 ICs Daisy-Chained

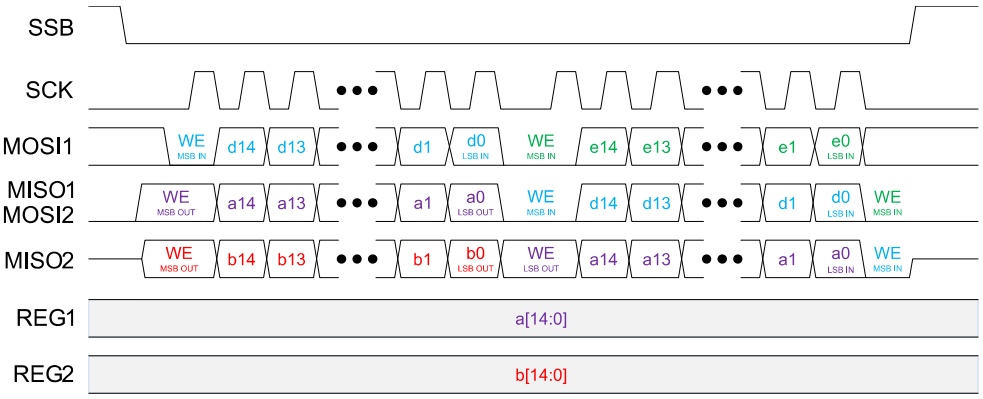


Figure 12. SPI Read Only (2 ICs Daisy-chained)

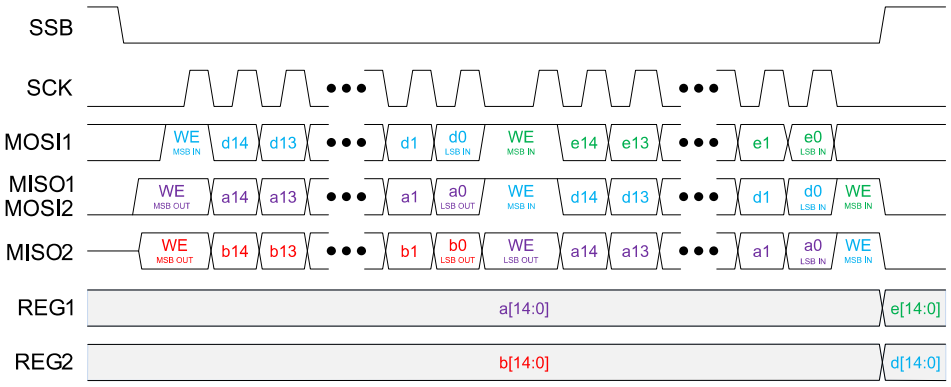


Figure 13. SPI Read & Write (2 ICs Daisy-Chained)

GPIO Communication

MODE = 1 and FLIP_BIT = 0 activates the GPIO (General Purpose Input Output or Parallel) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs, as described in Table 11. Detailed Pin Description. Valid switch states are listed here.

Table 12. State Table in GPIO Mode

Input Signals				Switch State
CTL4	CTL3	CTL2	CTL1	
0	0	0	0	ALL OFF (OPEN)
0	0	1	1	HS1 – HS2
0	1	0	1	LS1 – LS2
0	1	1	0	HS1 – LS1 and HS2 – LS2
1	0	0	1	MS1 – MS2
1	0	1	0	HS1 – MS1 and HS2 – MS2
1	1	0	0	MS1 – LS1 and MS2 – LS2
1	1	1	1	ALL ON (CLOSED)

Fault Conditions

There are two comparators that can signal a fault condition - VDD under voltage fault and VPP under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO.

Note: The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP_EN pin is set low.

The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than $UVLO_{RISE}$ and VPP goes higher than V_{EN}). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below $UVLO_{FALL}$ or VPP goes below VPP_{DIS}, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared and the FSTAT bit remains latched high until it is cleared via a SPI write. If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the internal high-voltage outputs are all set low (all switches open) and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to restart the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

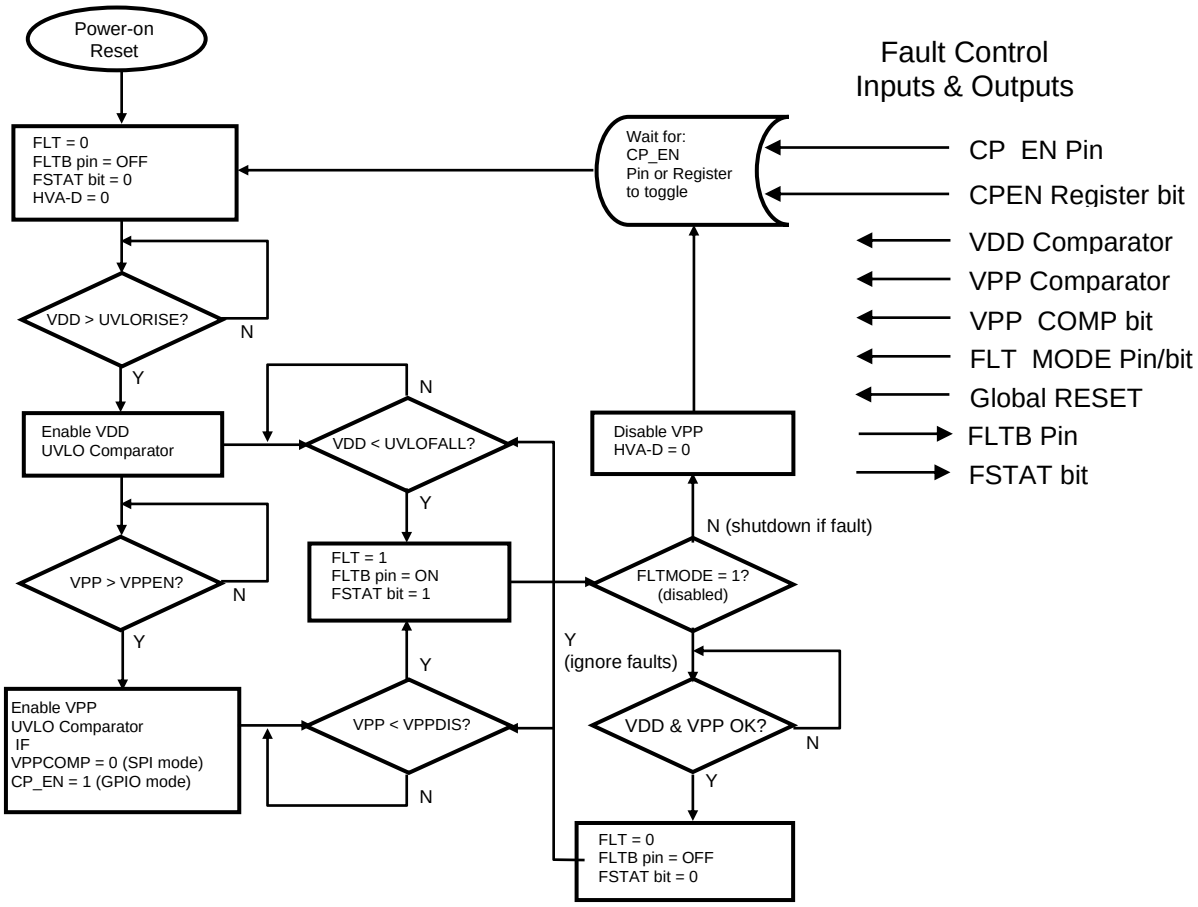


Figure 14. Flowchart for Fault

Notes:

1. The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2. VDD_IO is not monitored unless it is connected to VDD.
3. VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP_EN pin is low In GPIO mode.

Application Circuit Diagram

Figure 15, Figure 16, and Figure 17 show a few MM5620 application diagrams. For additional applications, refer to the MM5620 Application Notes.

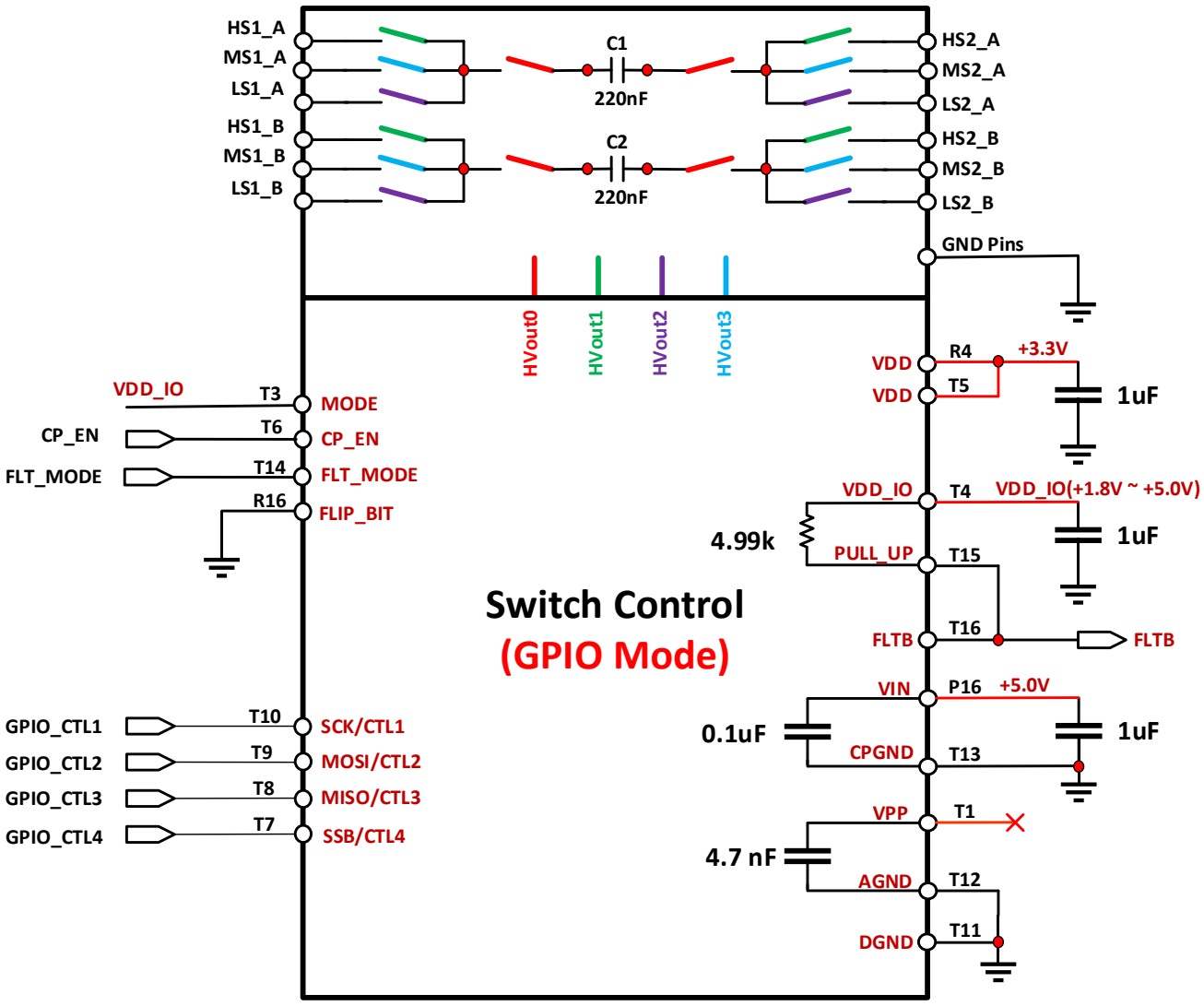


Figure 15. External Circuits for GPIO Mode

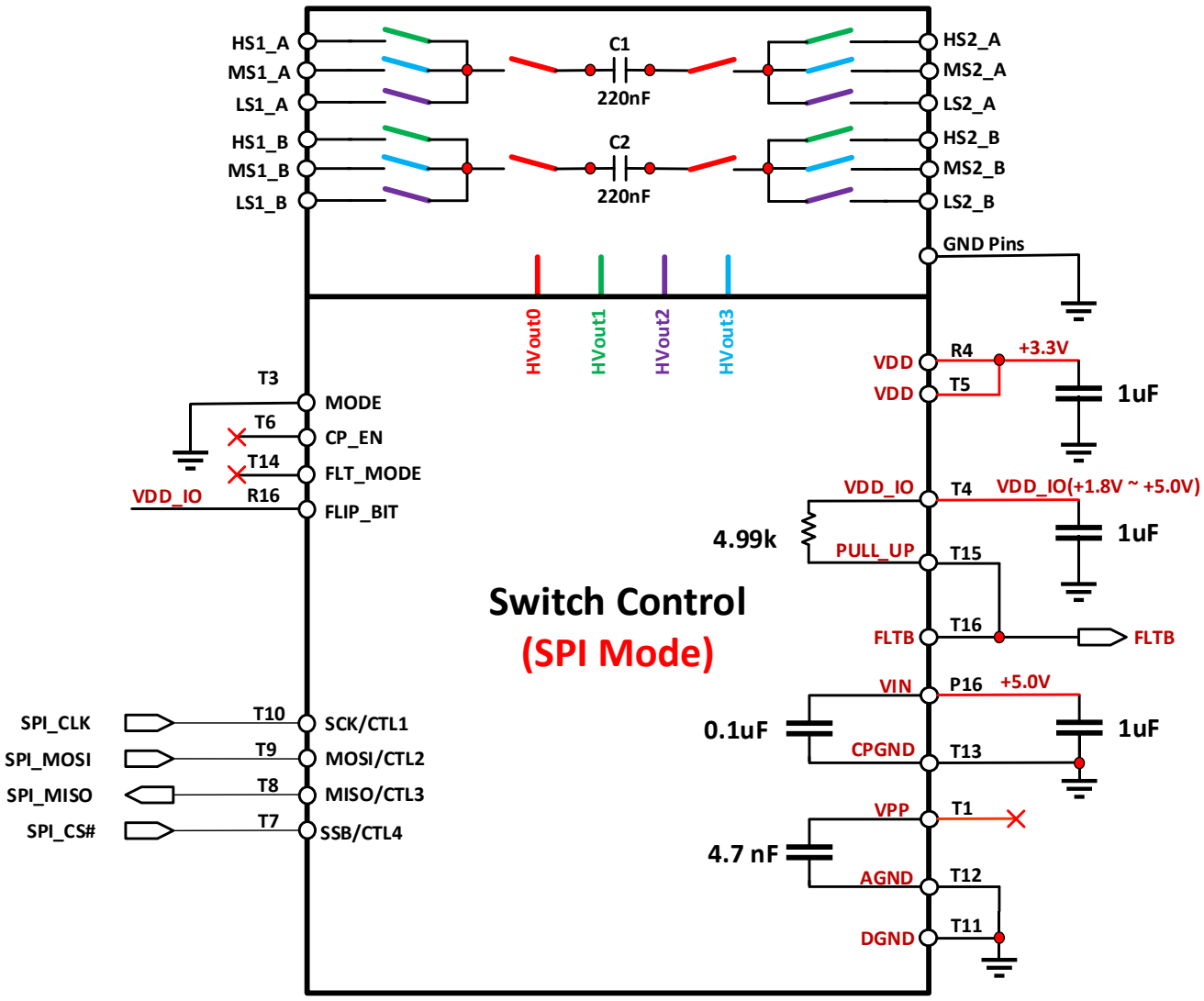


Figure 16. External Circuits for SPI Mode

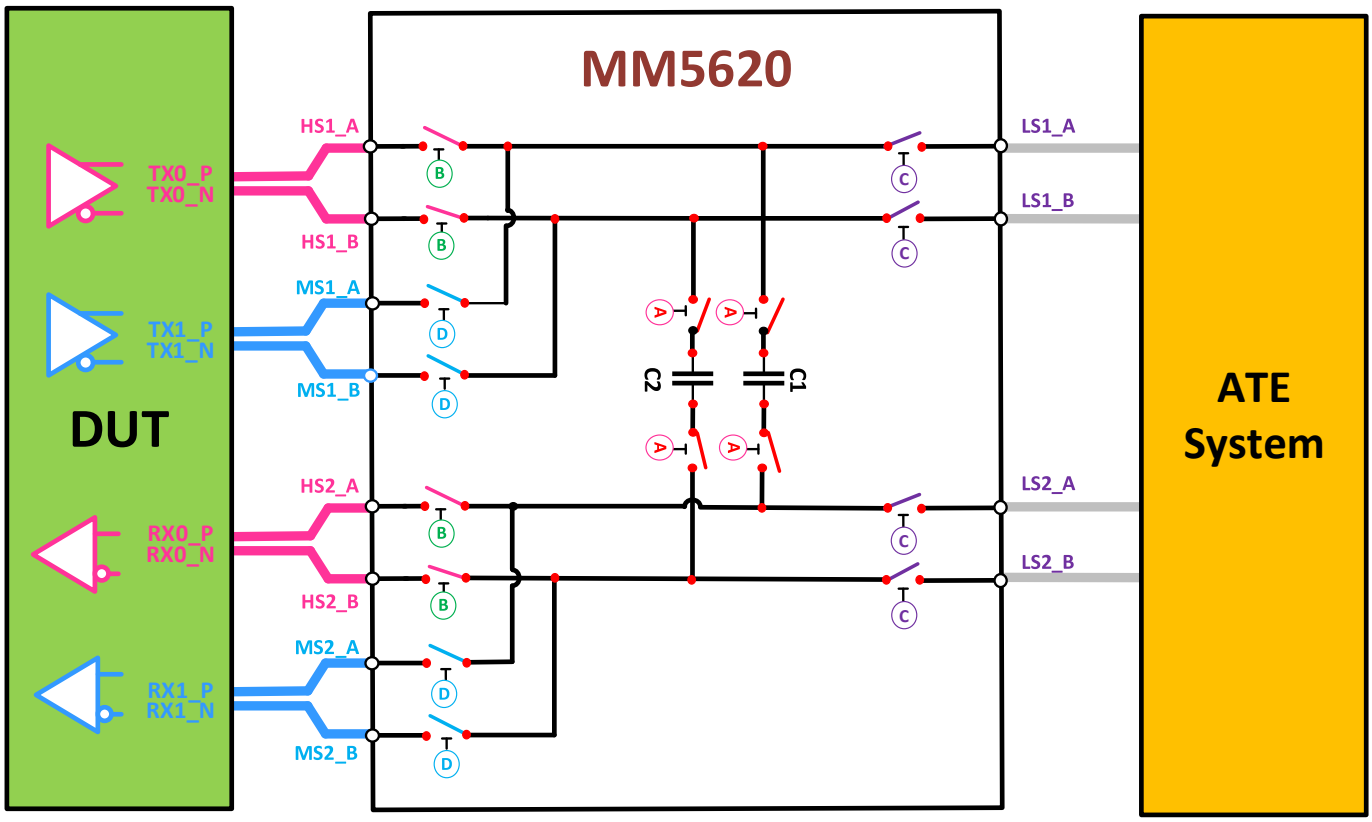


Figure 17. Double-Density HSIO Loopback Mode Test

Package Drawing

Figure 18 shows the 8.2 mm x 8.2 mm 226P LGA package drawing. All dimensions are given in millimeters.

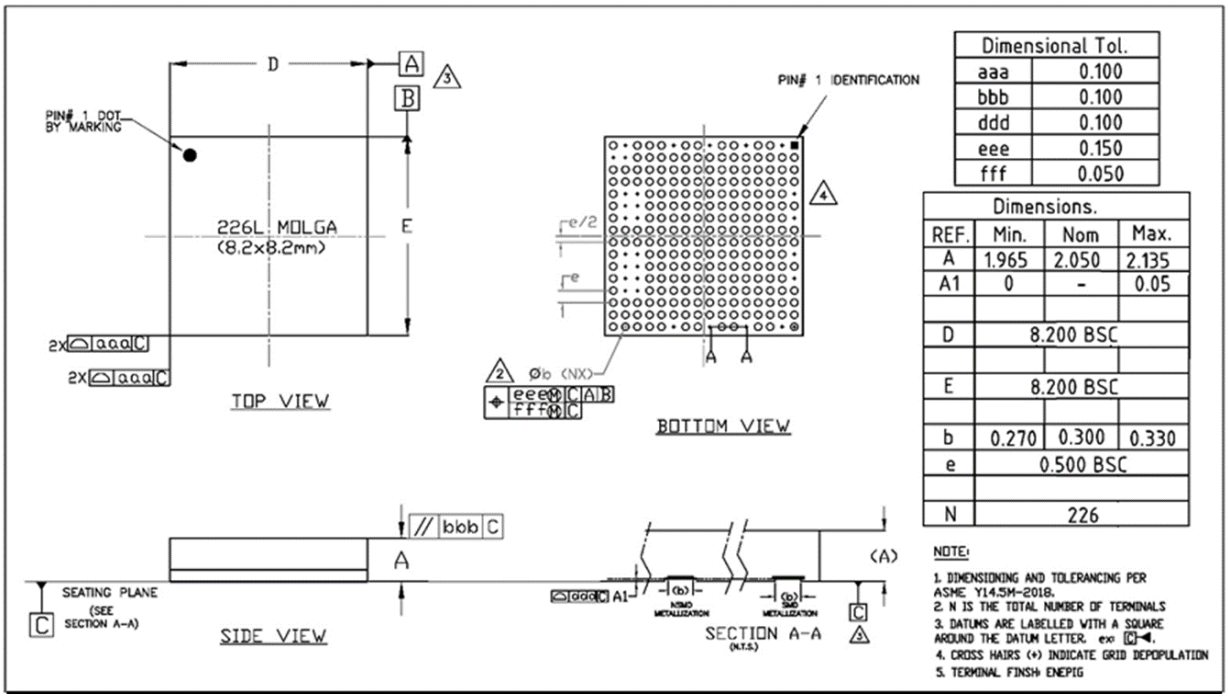


Figure 18. Package Drawing

MM5620 EVK PCB Layout

Figure 19 shows the PCB layout based on the MM5620 EVK stack-up.

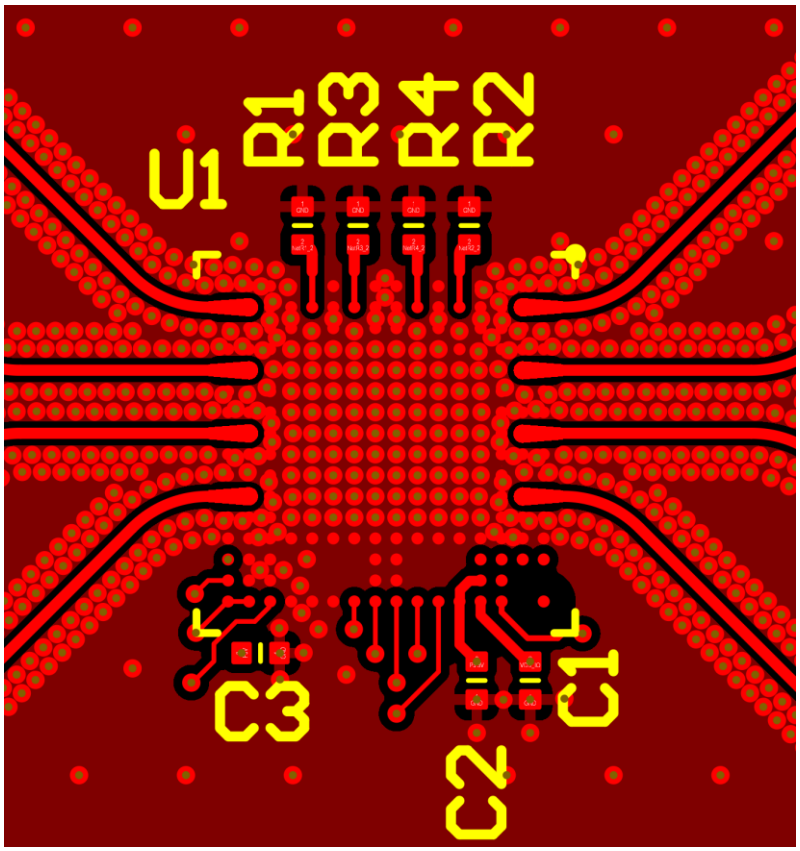


Figure 19. MM5620 EVK PCB Layout

Please contact your local Menlo Micro sales support for further information.

Recommended Solder Reflow Profile

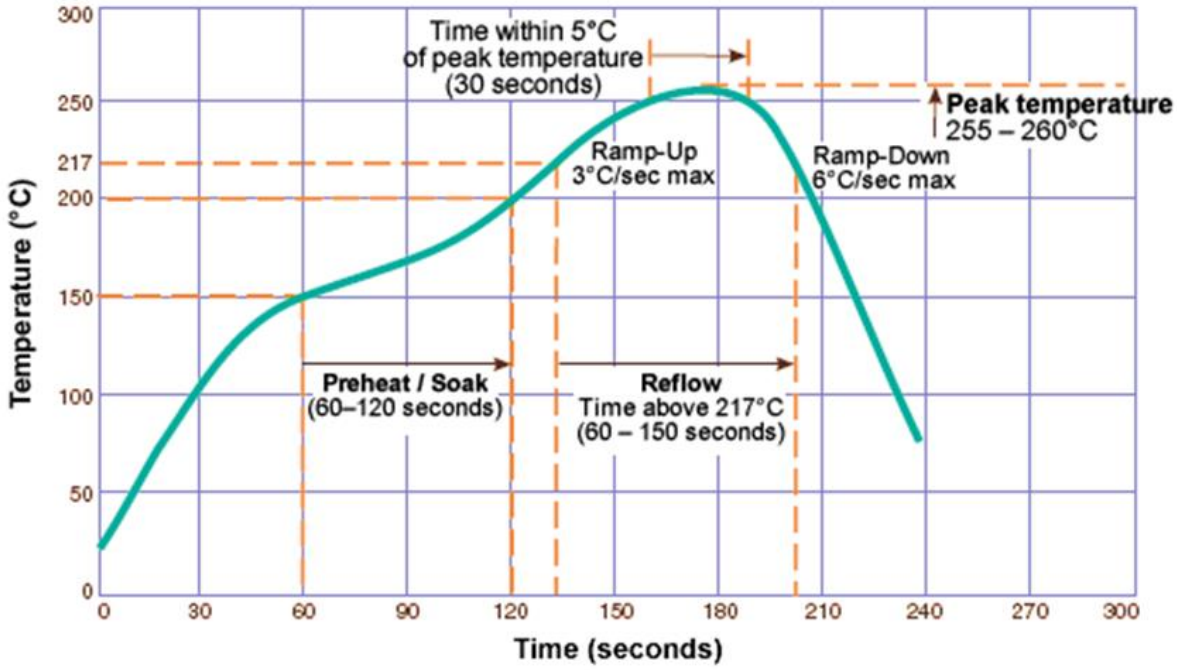


Figure 20. Reflow Profile

Reflow profiles and assembly guidelines are given for RoHS-compliant (lead-free) solder alloy.

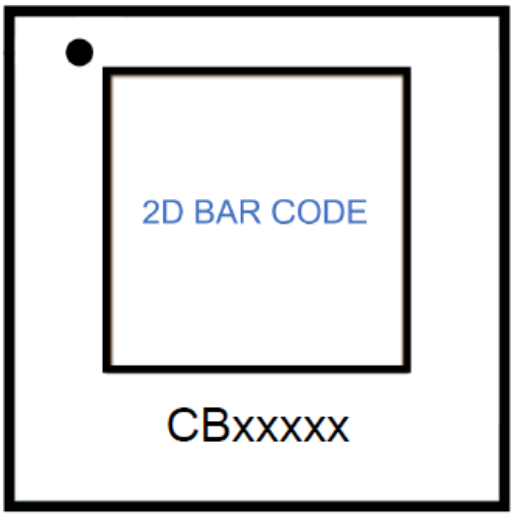
Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags, the following is recommended:

- Customer Shelf Life: 24 months from customer receipt date.
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less.

Package Marking Information



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Human-readable product code

Figure 21. Package Marking Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package Description	Temp Range	Device Marking[1]
MM5620-01NDB	Dual DPDT w/internal charge pump - loopback high-speed 64Gbps - 8.2mm x 8.2mm LGA Industrial Temperature	-40C to +85C	CBxxxxx
MM5620-01NDB-TR	Dual DPDT w/internal charge pump - loopback high-speed 64Gbps - 8.2mm x 8.2mm LGA Industrial Temperature Tape and Reel (Qty 250)	-40C to +85C	CBxxxxx
MM5620EVK2A	High-performance evaluation board for MM5620 (Dual DPDT w/internal charge pump-loopback, w/Southwest connectors-QTY-16), DC-64 Gbps - 8.2mmx8.2mm LGA		
MM5620EVK2B	High-performance evaluation board for MM5620 (Dual DPDT w/internal charge pump-loopback, w/Southwest connectors-QTY-8), DC-64 Gbps - 8.2mm x8.2mm LGA		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is a placeholder for a 5-digit numerical code.

Legacy Product	New Product Name	
Name	**Bulk**	**Tape and Reel[1]**
MM5620-01	**MM5620-01NDB**	**MM5620-01NDB-TR**

Notes:

1. 250pcs standard tape and reel increment.

Important Information

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Internet: www.menlomicro.com
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For product technical questions and application information: support@menlomicro.com.

