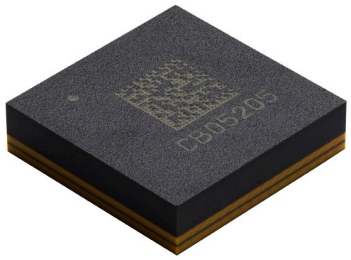
PRODUCT BRIEF

MM562x Product

64 Gbps/80 Gbps High-Speed Differential Switch



Menlo Micro's Differential Dual DP3T switches support the high-speed differential signal switching required in PCIe Gen 6, SerDes, and other applications. The MM562x (MM5620/MM5622-01NBX/MM5625/MM5627) switch is based on Menlo Micro's Ideal Switch® technology and can operate at 64 Gbps (MM5620) and 80 Gbps (MM5622-01NBX, MM5625, and MM5627) with a bandwidth of 20 GHz for high-performance applications.

The MM562x has low insertion loss, fast switching speed, and can operate with greater than 3 billion switching cycles. The MM562x has built-in integrated charge pump and high-voltage driver. A host processor can control the MM5620/MM5622 using GPIO or SPI control interface and the MM5625/MM5627 using SPI control interface only.

The MM5625/MM5627 has three additional gate control lines compared to the MM5620/MM5622, so it can provide much more flexible signal paths by controlling each differential pair individually. The design fully integrates the loopback capacitors for the MM5620/MM5625 and offers substantial reductions in size when compared with other high-speed switch solutions.

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FEATURES

- DC to 20 GHz range
- DP3T (differential mode) with Loopback Mode
- Normally Open, Reflective actuator
- Low Insertion Loss
- Each differential pair can be controlled individually and there are 128 possible switch control states for the MM5625
- Integrated charge pump and driver eliminates the requirement for external biasing and driver circuitry
- Fully controllable ports for low, medium, and high data rate signal routing
- High Reliability: Greater than 3 billion switching operations
- 8.2 x 8.2 mm LGA Package

APPLICATIONS

- High-Speed Data Digital SoC Testing
- ATE-Device Interface Boards
- O/E Module Testing
- Differential Switch Matrices

MARKETS

- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Test
- Compliance and Loopback Test

FIG. 1 MM5620/MM5625 Functional Block Diagram

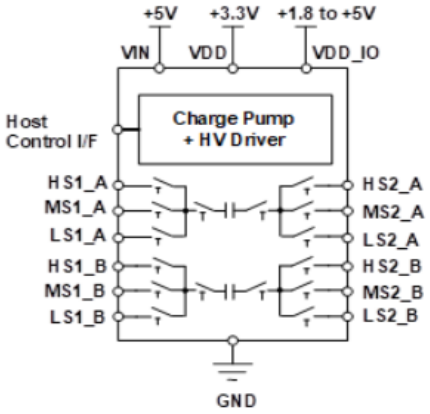

FIG. 2 MM5622/MM5627 Functional Block Diagram

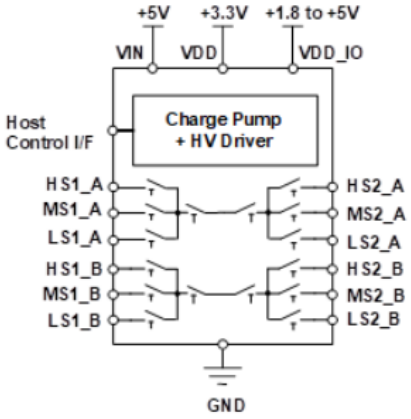

TABLE 1 MM562x Product Comparison

	MM5620	MM5622-01NBX	MM5625	MM5627
Frequency Range	DC to 20 GHz			
Built-in AC coupling capacitor	Yes	No	Yes	No
Enhanced RF performance	-	Yes	Yes	Yes
Differential Insertion Loss (dB) @16GHz	-1.5	-1.6	-1.6	-1.6
Differential Insertion Loss (dB) @20GHz	-3.0	-2.2	-2.7	-2.2
Support asymmetric signal paths	-	-	Yes	Yes
Host Control Interface	GPIO or SPI		SPI	
Max. switch control states	16		128	
Number of gate control lines	4		7	
Footprint compatibility	Yes	Yes	Yes	Yes

FIG. 3 MM5620: HS1-HS2 Differential PAM4 Eye Diagram - 64 Gbps

*Analyzed with ADK (Advanced SI Design Kit), PCIe Gen6, 500mVpp, PAM4, 64Gbps, PRBS 215-1, Rise Time 10ps (20-80%)

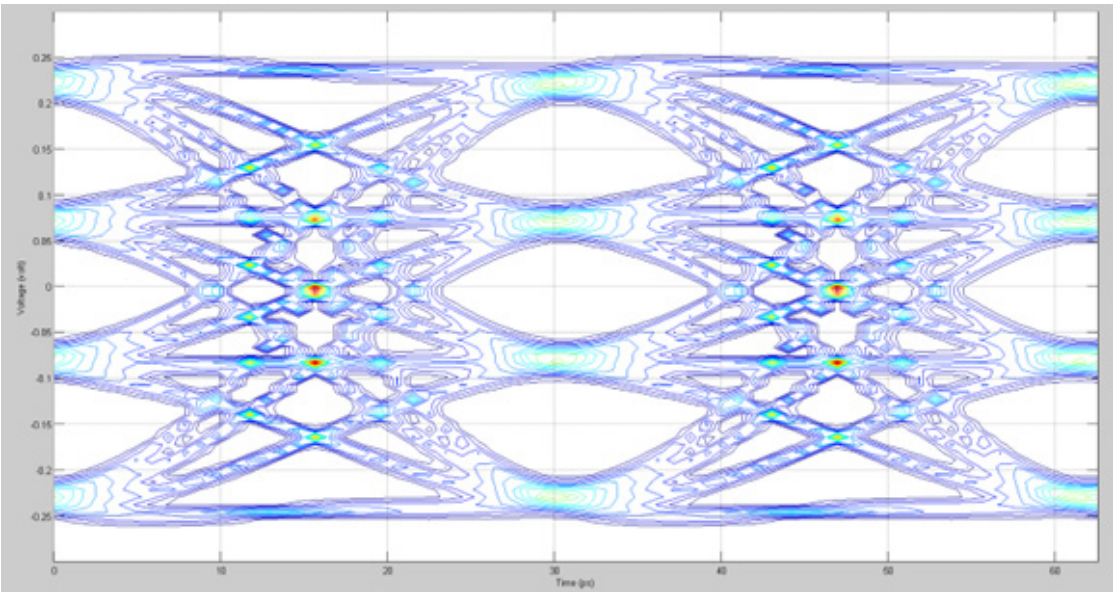

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FIG. 4 MM5622-01NBX: HS1-HS2 Differential PAM4 Eye Diagram - 80 Gbps

*Analyzed with ADK (Advanced SI Design Kit), 500mVpp, PAM4, 80Gbps, PRBS 215-1, Rise Time 7.5ps (20-80%

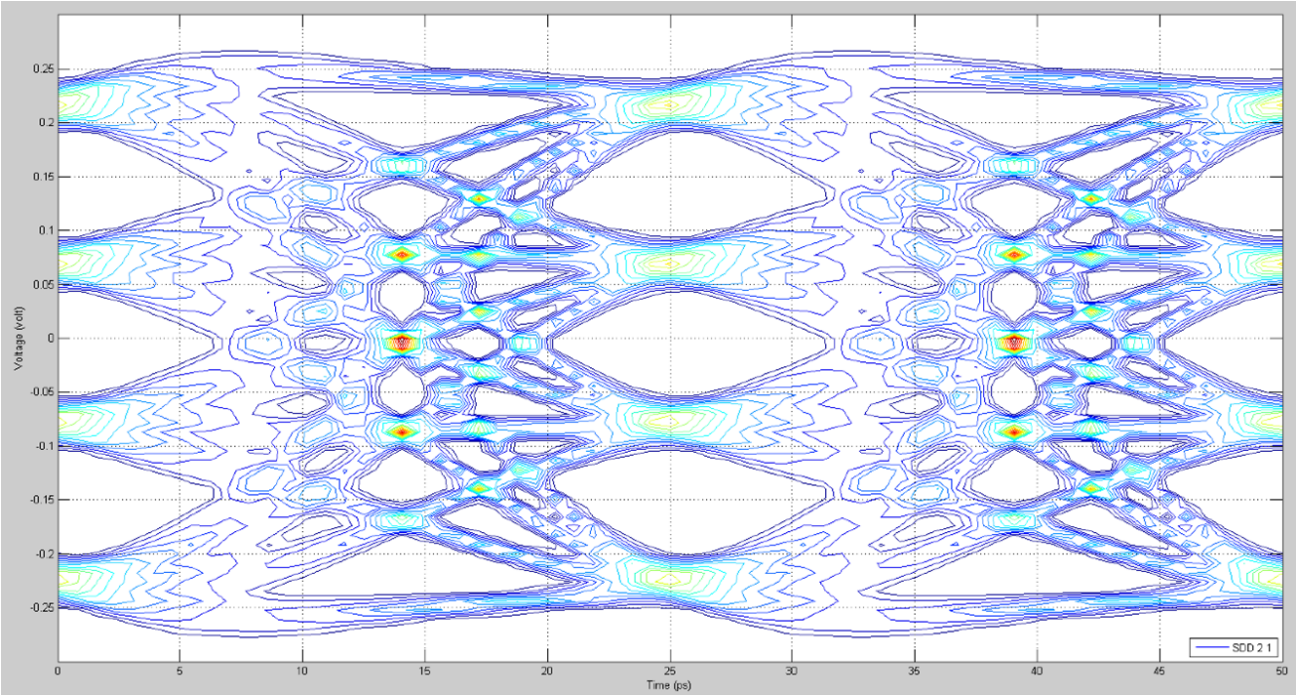

FIG. 5 MM5622-01NBX: HS1-HS2 Differential PAM4 Eye Diagram - 64 Gbps

*Analyzed with ADK (Advanced SI Design Kit), PCIe Gen6, 500mVpp, PAM4, 64Gbps, PRBS 215-1, Rise Time 10ps (20-80%)

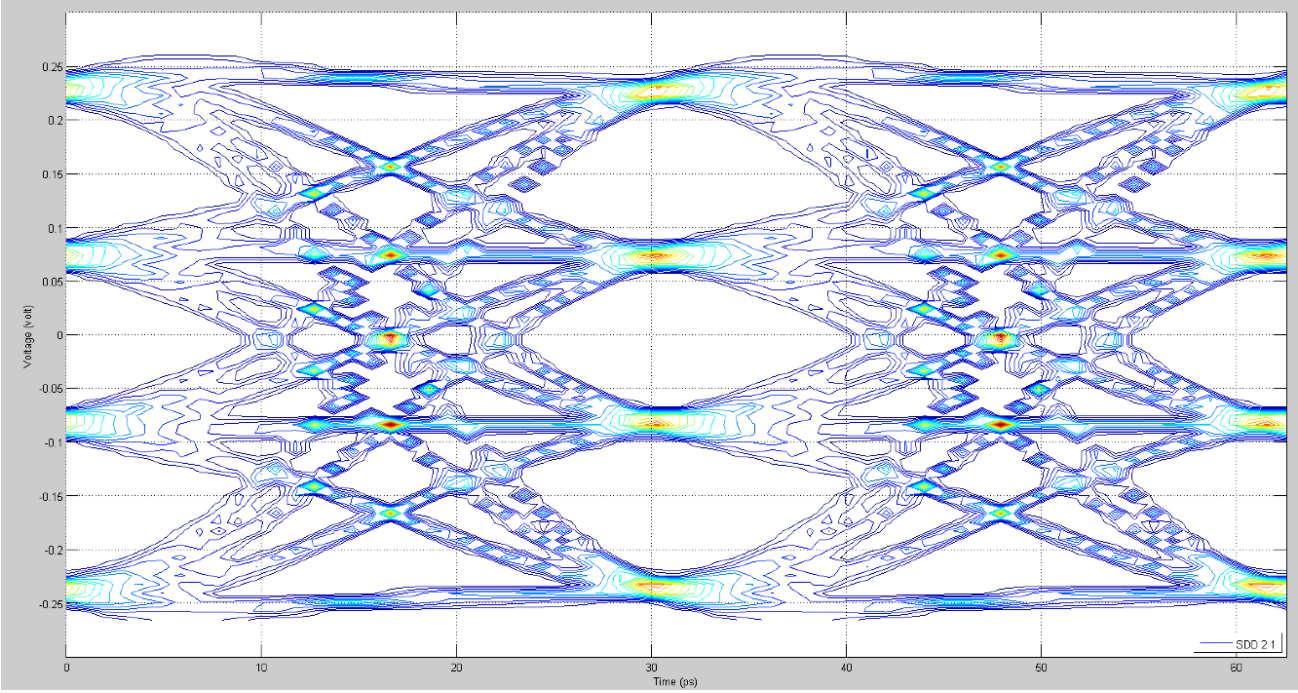

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FIG. 6 MM5625: HS1-HS2 Differential PAM4 Eye Diagram - 80 Gbps

*Analyzed with ADK (Advanced SI Design Kit), 500mVpp, PAM4, 80Gbps, PRBS 215-1, Rise Time 7.5ps (20-80%)

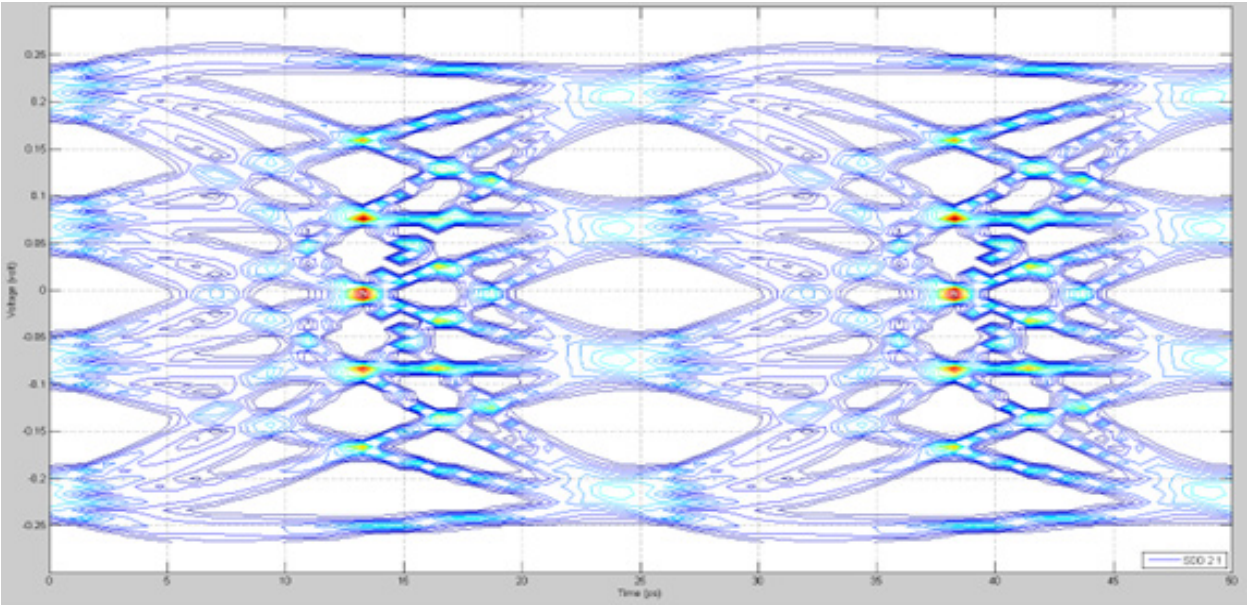
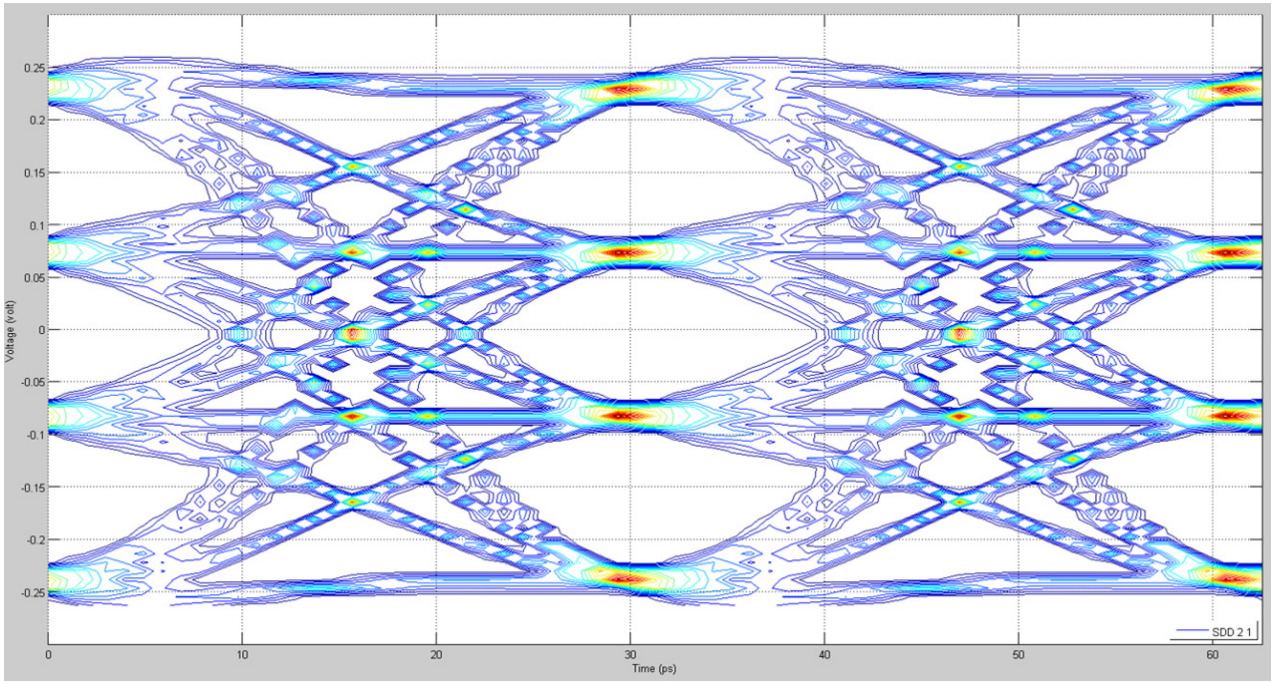


FIG. 7 MM5625: HS1-HS2 Differential PAM4 Eye Diagram - 64 Gbps

*Analyzed with ADK (Advanced SI Design Kit), PCIe Gen6, 500mVpp, PAM4, 64Gbps, PRBS 215-1, Rise Time 10ps (20-80%)



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