Edge Coupled DC to 60GHz Differential SPDT RF MEMS Switch for High-Speed Digital Applications

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***Abstract*— This paper introduces an edge-coupled differential SPDT MEMS switch for high-speed digital applications over 100Gbps. Built on an 8-inch fused silica wafer and hermetically sealed with a fused silica cap, it supports DC to 60GHz operation. The ohmic contact switch design achieves <1dB differential insertion loss up to 60GHz, with >15dB differential return loss and 20dB differential isolation.**

***Index Terms*— differential switch, RF MEMS, SPDT, Glass, CPWG**

I. INTRODUCTION

In recent decades, data transfer rates in electrical systems have increased exponentially. Wireless communication has progressed from 384Kbps in GSM to over 20Gbps in today's 5G networks. The development of computer systems, data centers, and AI applications has pushed single-lane data rates from tens of Mbps to over 64Gbps, with the industry aiming for 224Gbps soon [1][2]. To support these speeds, a minimum channel bandwidth of DC-16GHz is required, ideally covering the 2nd and 3rd harmonics to maintain high-frequency information and ensure a larger eye opening. To mitigate noise and EMI, digital signals are transmitted differentially, necessitating well-matched differential pair trace designs. Optimizing line impedance and reflection for optimal performance relies heavily on RF/Microwave design techniques.

This paper presents the first true full-differential DC-60GHz switch design for differential signal routing. Network systems in data centers and test equipment for high-performance digital chips, such as AI chips, CPUs, GPUs, and memory, require constant re-routing or reconfiguration of signal paths. Semiconductor solutions face bandwidth limitations and challenges in handling different DC-biasing voltage levels and large signal capabilities. In test equipment applications, the insertion loss of semiconductor switches varies significantly with temperature, complicating the removal of this variation from final DUT test results. MEMS switch solutions, with their inherent high linearity, are immune to changes in digital system DC bias voltage and environmental temperature variations, making them ideal for applications where sub-microsecond switching and tens of billions of cycles over the lifetime are not required.

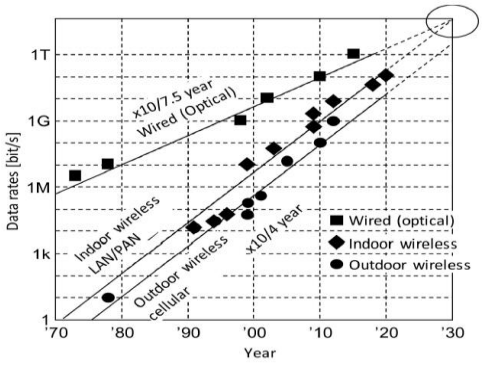

Fig. 1. Evolution of data rate of wired communication and wireless communication [1].

II. EDGE COUPLED DIFFERENTIAL SPDT SWITCH DESIGN

This switch leverages the high isolation capability of RF MEMS technology and adopts a simple in-line switch topology, avoiding the parasitic loading of signal lines common in series-shunt configurations used in semiconductor switch designs (Fig. 2(a)). A unique aspect of this design is its edge-coupled full differential structure, which is like a traditional double-pole double-throw (DPDT) switch (Fig. 2(b)) but its physical implementation is significantly different. In a traditional DPDT switch, the two paths inside the switch are not coupled, resulting in zero cross-coupled terms (e.g., S31, S42) and diminished common mode and interference rejection, leading to lower SNR. The direct benefit of this design is saving layout space, as sufficient isolation ground traces and associated clearance to RF traces consume a lot of chip area, as shown in the die layout (Fig. 2(c)). Enhance impedance tuning can be implemented at the device terminal, which tends to be inductive due to long through-glass vias (TGVs) (Fig. 2(d)). This design includes stubs for fine-tuning port differential impedance on the MEMS device substrate next to TGVs. Further details are shown in Fig. 2(c), featuring a coplanar edge-coupled waveguide GSSG structure. The top metal layer serves as a

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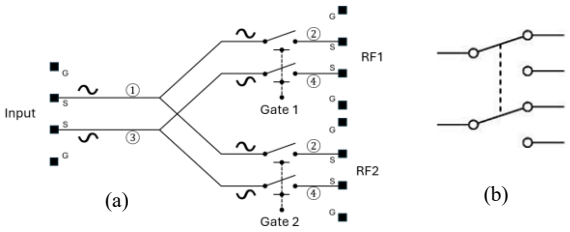
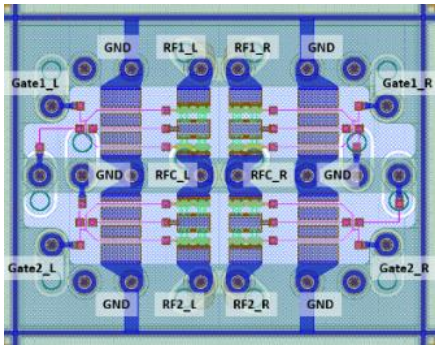
ground plane, with RF signals and DC gate controls fed from the top surface to the MEMS substrate through 50µm diameter Cu TGVs. TGVs also connect the ground trace on the MEMS wafer to the top ground plane. The GSSG RF signal trace width is 246µm, the space between edge-coupled RF traces is 150µm, and the space between RF traces and the ground plane is 275µm, resulting in a 100Ω differential impedance with a return loss close to 20dB.

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \Leftrightarrow \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} \begin{bmatrix} S_{dd11} & S_{dd11} \\ S_{dd11} & S_{dd11} \end{bmatrix} \begin{bmatrix} S_{cc11} & S_{dd11} \\ S_{dd11} & S_{dd11} \end{bmatrix} \quad (1)$$





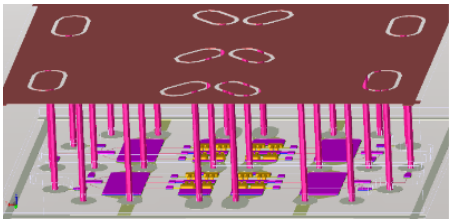


Fig. 2. Full differential SPDT switch design. (a) Schematic diagram of proposed differential SPDT switch; (b) Schematic diagram of traditional DPDT switch; (c) Device layout; (d) Device 3-D CAD view with TGVs connecting top feeding ports to the MEMS switch device inside hermetic sealed CSP.

The 3D FEM simulation results are shown in Fig. 3. The 2D layout was converted to a 3D structure in Keysight ADS using the appropriate substrate technology setup and then exported to a 3D structure simulation tool, such as Keysight EMPro or RFPro. With a 50Ω excitation applied to each RF port, no special constraints were needed to simulate this differential edge-coupled coplanar waveguide structure. The simulation yields a 4-port single-ended S-parameter, as shown on the left side of Eq. 1. The insertion loss and return loss are plotted in Fig. 3(a), with a 1dB bandwidth around 38GHz. This 4-port single-ended S-parameter can be converted to a 2-port mixed-mode S-parameter [4], as shown on the right side of Eq. 1. The upper left quadrant, describing differential signal input and output, is of particular interest. The differential signal insertion loss and return loss are plotted in Fig. 3(b). The 1dB bandwidth approaches 60GHz, significantly higher than the single-ended bandwidth due to cross-coupling between differential traces, which confines RF energy within the two parallel traces rather than allowing energy loss to adjacent metals.

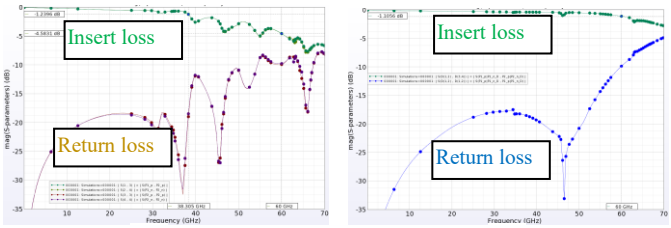


Fig. 3. 3D FEM simulation results of full differential SPDT switch design under all absorb boundary conditions. (a) Single-end mode; (b) Differential mode.

III. Devie Fabrication

The device fabrication involves two separate wafer process flows: constructing MEMS cantilever structures on a 200mm Fused Silica (FS) substrate and creating an encapsulation cap wafer, also on a 200mm FS wafer. The MEMS wafer process begins with depositing and patterning a doped polysilicon layer, primarily used as a DC biasing resistor in the control lines. Next, the gate control metal layer is deposited and patterned, followed by forming Au GSSG trace. A sacrificial layer is then deposited and patterned, followed by RF switch contact and Au alloy cantilever beams. The final step in the MEMS wafer process is removing the sacrificial layer to release the cantilever beam. The cap wafer process starts with laser drilling through holes, which are then filled with copper. A cavity is etched, and Au is deposited and patterned on both sides. The finished cap wafer is thermal compression bonded with the MEMS wafer to provide a hermetic seal environment for the MEMS ohmic contact switch. The cross-section of a switch element is illustrated in Fig. 4, and the completed die photo is shown in Fig. 4(c).

III. Measurement Result

The device was tested using Formfactor 250µm pitch Dual-Infinity 67GHz GSSG probes and the Formfactor 129-247 GSSG Impedance Standard Substrate. SLOT and LRRM methods were employed for on-wafer probe calibration up to 67GHz. Various VNAs, including the Keysight 67GHz PNA-X, 50GHz Streamline PNA, and Rohde & Schwarz 67GHz

ZNA, were evaluated. The switch has inherently low loss, much smaller than the cables and RF probes, therefore network analyzers used in the test need to have sufficient output power at the frequency range interested for receiver to detect insertion loss induced by the switch. Fig. 5 shows that the differential performance of the measured DUT closely matches the EMPro simulation up to 50GHz, both in terms of insertion loss and return loss. The impact of metal chuck of probe station is modelled as Perfect Electric Conductor PEC boundary at the bottom of the MEMS switch. The insertion loss becomes non-passive for this passive device above 60GHz. The Keysight Streamline PNA has a weaker PA and receiver component compared to the Keysight PNA-X and Rohde & Schwarz ZNA, resulting in a noisier signal. The insertion loss results from all VNAs are better than 0.5dB at 50GHz, and the return loss is close to 20dB up to 50GHz. This is the best performance published to date, surpassing all previously published semiconductor and RF MEMS switches [5-9].

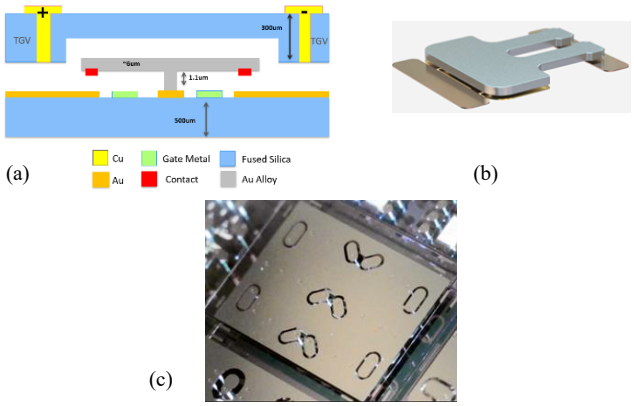


Fig. 4. Details of MEMS switch device. (a) Cross section of metal MEMS switch which will be sealed by a cap wafer; (b) Perspective view of single cantilever switch element, as in Fig. 2; (c) Die photo.

By inputting the measured S-parameters into Keysight ADS High-Speed Digital simulation, NRZ or PAM eye-diagrams can be derived. With a 1dB bandwidth exceeding 50GHz, which is much wider than existing RF MEMS products on the market [8][9], even a 64Gbps NRZ signal produces a perfect eye-diagram, as shown in Fig. 6(a). Typically, for data rates over 32Gbps, the industry adopts higher modulation schemes, with PAM4 widely used in communication interface standards like PCI Express (PCIe) for connecting peripherals such as CPUs, GPUs, DRAM, flash memory, and Ethernet. With confining s-parameter data bandwidth to 55GHz and at a 128Gbps data transfer rate, the eye-diagrams from Keysight and Rohde & Schwarz measured S-parameters appear similar. However, when pushed beyond 160Gbps, the eye opening for Rohde & Schwarz starts to shrink and nearly closes at 200Gbps. In contrast, Keysight's eye opening remains relatively decent even at 200Gbps. The hypothesis is that rapid variations in the magnitude of insertion loss and return loss may distort the time-domain response, thus affecting the eye diagram.

V. Discussion

After eliminating several factors from the test, including different VNAs from various vendors, different VNA settings, RF cables from different vendors, and standard SOLT and LRRM calibration procedures, the focus shifted to the calibration procedure to address the non-causality issue. With assistance from the Formfactor R&D department, several new calibration routines for handling GSSG probe configurations were explored. The top half of the switch was measured first using a pair of GSSG probes, followed by stepping the wafer to probe the second half of the switch. This allowed the RFC port to be connected to both sides of the VNA in different port configurations, examining any potential asymmetry in the measurements.

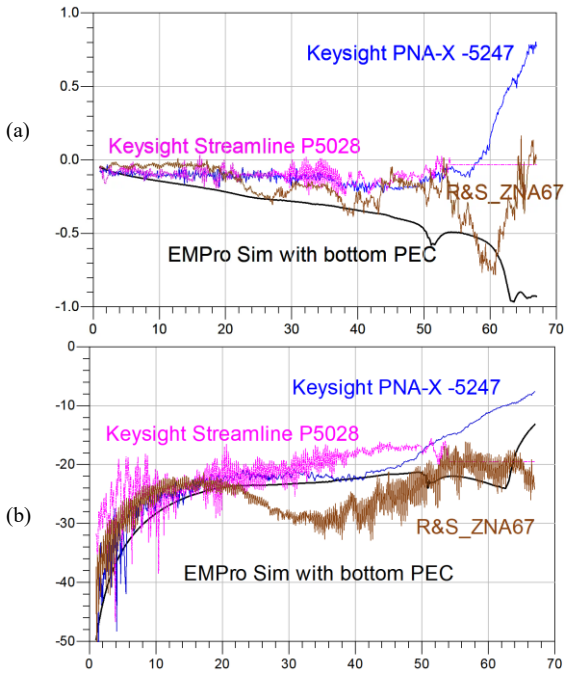


Fig. 5. Wafer probe measured differential performance of edge coupled differential switch *vs*. Keysight EMPro FEM simulation. In EMPro simulation, the boundary condition for bottom of die is set to PEC whereas all other sides are set to absorption to mimic device wafer sitting on metal chuck during the wafer probing. Three 4-port networks analyzers are used to compare performance. (a) Differential insertion loss; (b) Differential return loss.

The differential port measurement configuration is shown in Fig. 7(a). The 4x4 single-ended S-parameter plot for the switch's CLOSE state is shown in Fig. 7(b) and indicates that the device is symmetric as designed. Fig. 7(c) and (d) shows the first quadrant of measurement *vs.* FEM at OPEN and CLOSE state. Deviations in the measured return loss from the FEM simulation of each port are observed above 30GHz, with significant discrepancies in the OPEN state, while in the CLOSE state, these discrepancies are less noticeable. This difference could be due to improper treatment of cross-

coupling between adjacent ports, such as between ports 1 and 2, and between ports 3 and 4. In the OPEN state, the cross-coupling is more pronounced in measurement than in the simulation, leading to less reflection power being measured at each port, as seen in Fig. 7(d) for S11 and S22. In the CLOSE state, as Fig. 7(c), the cross-coupling between the two ports is stronger, but the difference between the measurement and FEM simulation is smaller, mainly because there is no strong reflector from the small open state in-line capacitance of MEMS in the signal path. However, the improperly treated cross-coupling still causes slightly higher port reflection.

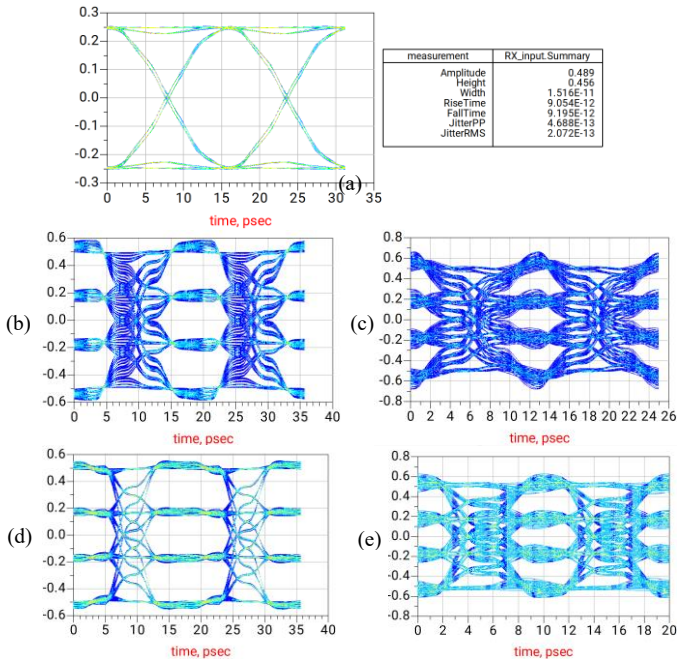
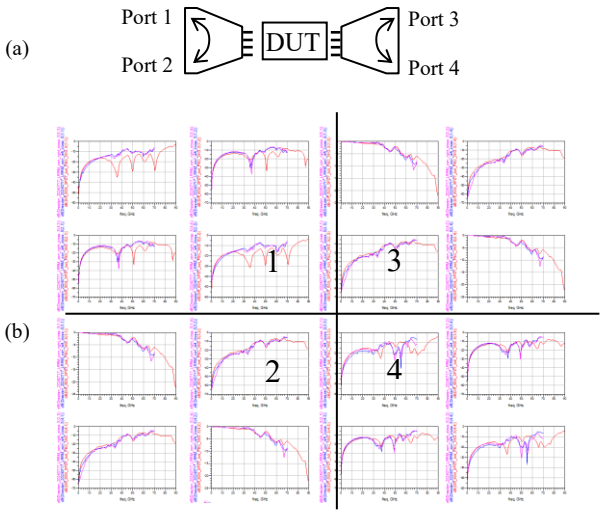


Fig. 6. 4-Port S-parameter generated eye diagram by Keysight ADS channel simulator. No equalization is applied. (a) 64Gbps 2^{15}-bit NRZ signal, similar for S-parameter obtained from Keysight and Rohde & Schwarz VNA; (b) 112Gbps PAM4 and (c) 160Gbps PAM4 eye diagram with S-parameter obtained from Rohde & Schwarz ZNA67; (d) 112Gbps PAM4 and (e) 200Gbps PAM4 eye diagram with S-parameter obtained from Keysight PNA-X 5247.



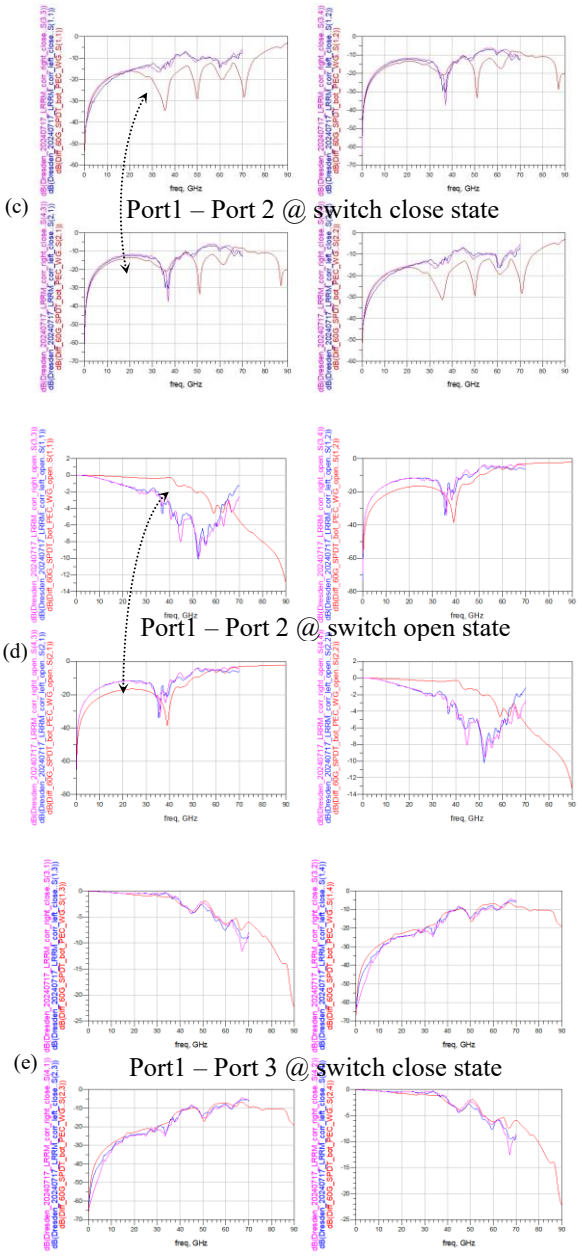


Fig. 7. Single-end 4-port S-parameter of switch at CLOSE and OPEN states. (a) 4-port configuration; (b) 4 quadrants of 16 S-parameters; (c) Adjacent ports' return loss and cross coupling (e.g. quadrant 1) at switch CLOSE state shows divergent from simulation from 30GHz; (d) Adjacent ports' return loss and cross coupling (e.g. quadrant 1) at switch OPEN state show divergent from simulation from 30GHz; (e) Forward insertion loss and channel coupling (e.g. quadrant 2) at switch CLOSE state matched simulation.

To further explore the root cause, with assistant from FormFactor, four different calibration routines are evaluated. They are: first tier typical calibrations: LLRM-SOLR (Line-Reflect-Reflect-Match Short-Open-Load-Reciprocal) and SOLR (Short-Open-Load-Reciprocal;) and second tier modal calibrations ML (Modal LRRM) and MS (Modal SOLR)[10]. The modal calibration algorithm is developed with the

consideration of differential trace configuration and factor in cross coupling of the trace. The differential insertion loss and return loss are shown in Fig. 8. Unfortunately, the non-passive behavior of insertion loss persists. The LRRM-SOLR shows the best match of differential return loss between measurement and simulation but has the worst deviation of differential insertion loss. The modal methods show closer match of differential insertion loss but more than 10dB worse of return loss. Both Modal LRRM and SOLR show unexpected insertion loss hump from 20~45GHz. Similar insertion loss behavior is also reported with different calibration methods and ISS designs [11].

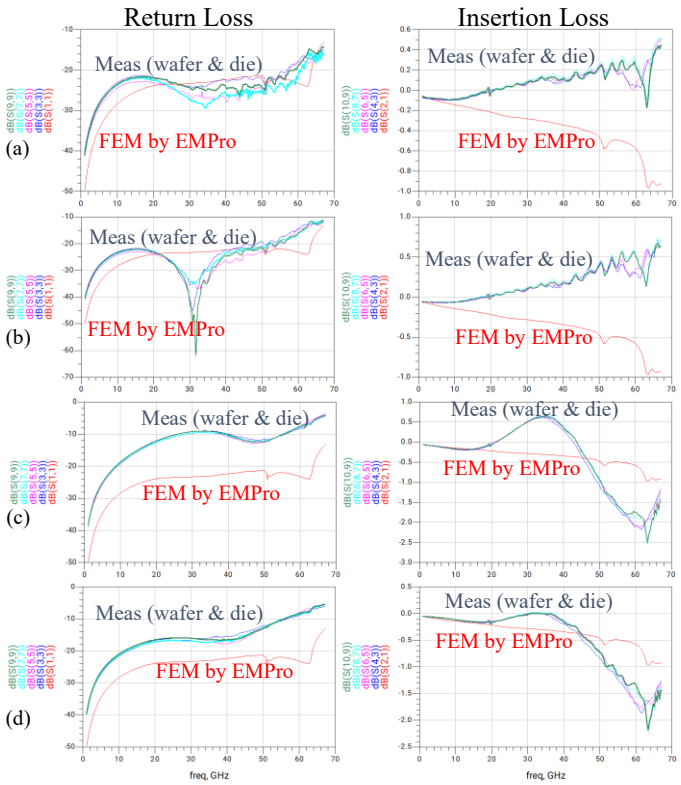


Fig. 8. Differential insertion loss and return loss of the differential switch at CLOSE state under four different calibration method: (a) LRRM-SOLR (b) SOLR (c) Modal LRRM and (d) Modal SOLR. The solid redline is Keysight EMPro FEM simulation results. The blue & purple color line (probing DUT on un-diced wafer) and cyan and green color line (probing singulated die) are measured data of each throw at CLOSE state while the other throw is set at OPEN. The left column of plots is differential return loss, and the right column of plots is differential insertion loss.

There are several suspected root causes for this kind of behavior. The first one is that the GSSG probe is calibrated on an alumina substrate with ε_r=9.8, and the device is built on FS substrate ε_r=3.7. The difference in coupling capacitance between the two signal probes could be amplified when loaded with the high-quality factor small open capacitance of the RF MEMS switch. The proposed plan is to build a full calibration kit on the FS substrate for probe testing. The ISS structure design may also play a role here. More specifically, the differential THRU and OPEN structure design has incorporated ground pattern and trace between two differential traces, making more like two isolated single-ended structures. The purpose for this kind of ISS design is to match 4-port VNA whereas all ports are independent and uncoupled. Therefore, calibration may yield different coupling between RF probe tips than this differential SPDT switch design, probably less coupling capacitance which results in difference between simulation and measurement shown in Fig. 7. For high-speed digital applications, another approach is to use an arbitrary waveform generator with a high-speed digital series oscilloscope to obtain the eye-diagram directly.

V. Conclusion

In the paper, we demonstrated a differential SPDT RF MEMS switch fabricated on fused silica substrate with glass hermetic sealed. The design is based on edge coupled co-planar wave guide structure and achieves state-of-art broadband performance: 1dB insertion loss bandwidth close to 60GHz and return loss close to 20dB. This device is able to serve the demand for over 100Gbps data transfer rate applications such as data center ethernet connection and test and measurement of high-performance AI chips, mobile applications processor, CPU, GPU and DRAM.

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