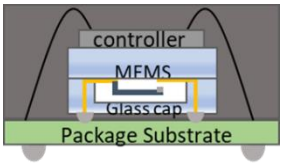
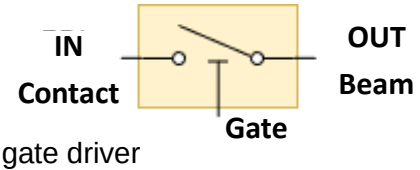
Preliminary Datasheet
MM1200 – 6 Channel SPST Micro Relay

Product Overview

Description

The MM1200 device is a 6-channel SPST Micro Relay intended for power and signal switching applications in both DC and AC circuits. Each channel provides ultra-low on-state contact resistance and high off-state isolation with greater than 3 billion switching cycles. Each channel can be individually controlled by a serial-to-parallel interface that drives the gate lines of the individual channels. The flexibility of six SPST channels enable implementation of different signal topologies such as dual SP3T, triple SP2T or 2x3 matrix. Only an external logic supply and gate bias source is required for operation of the device.





Features

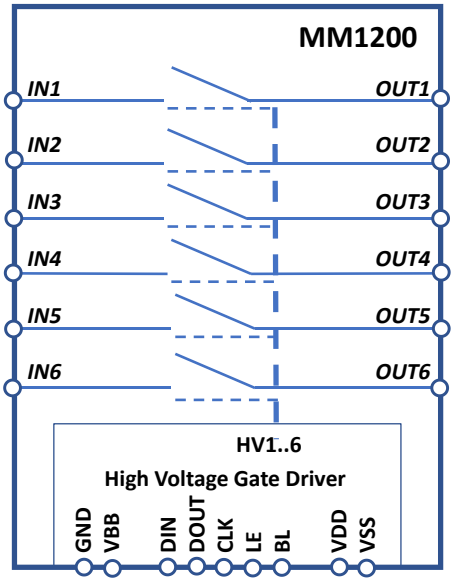
- 1.0 A per channel and 3.0 A per package
- Maximum Voltage (AC peak or DC): +/-150 V on Input
- Low On-State Resistance < 1.0 Ω typical per channel
- 10 G Ω Input to Output Isolation
- Switching Time of 8 us typical
- High Reliability > 3 Billion Switching Operations
- Integrated driver eliminates requirement for an external gate driver
- 6 mm x 6 mm BGA Package

Applications

- High Density Switch Matrices
- Automated Test and Measurement Systems
- Mechanical Relay Replacement

Markets

- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom



Electrical Characteristics

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1200 should be restricted to the limits indicated in Table 2 and Table 3 recommended operating conditions listed below.

Electrostatic Discharge (ESD) Safeguards

The MM1200 is a Class 0 ESD device. When handling the MM1200, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Susceptibility to Latch-Up

The following power sequence is recommended to avoid latch-up:

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, remove all inputs, remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present.

Table 1 Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (VDD)		7.5	VDC
High Voltage Gate Supply (VBB)		90	VDC
Driver Logic Input Levels	-0.3	VDD + 0.3	V
DC Voltage VBB to OUTx pin (V_{VBB_OUT})	-100	100	V
Open State Voltage Rating/Channel INx to OUTx[2]	-150	150	V

[1] All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied during the on-state condition (cold-switched condition).

[2] This also applies to ESD events. This is a Class 0 device.

Open State Voltage OUT1-OUT6, IN1-IN6 to GND	-150	150	V
DC Current Rating / Channel		1000	mA
Operating Temperature Range MM1200-00	-40	+85	˚C
Storage Temperature Range	-65	+150	ºC
Reflow Soldering (Pb Free) Peak temp		260	C
Reflow Soldering Time at Peak		30	sec
ESD Rating HBM Driver Pins[3]		TBD	V
ESD Rating HBM Channel I/O Pins[4] [5]		150	V
Mechanical Shock		TBD	G
Vibration		TBD	Hz

[3] Driver pins include: CLK, LE, DIN, DOUT, BL, VBB, VDD.

[4] Channel I/O pins include: IN1 to IN6, OUT1 to OUT6.

[5] IN and OUT pins must not be allowed to electrically float during channel operation. See section *Floating Node Restrictions* for details on avoiding floating nodes.

Table 2 Recommended Operating Conditions, DC and AC Electrical Characteristics

All specifications valid over full V_{BB} range and operating temperature range unless otherwise noted.

Parameter	Minimum	Typical	Maximum	Unit
AC/DC Carry Current/Channel			1.0	A
Total Carry Current per Device			3.0	A
Off/Open State Rated Carry Voltage (Input to Output)[6]	-150		150	V_{DC}
On / Closed State Output to VSS Voltage	TBD		TBD	V_{DC}
On / Off Switching Time[7]		8	TBD	µs
Full Cycle Frequency			10	kHz
On / Off Channel Operations (Cold Switched)	$3x10^9$	TBD		Cycle
On / Off Hot-Switch Operations[8] 0.5 V 1.0 V		 TBD TBD		Cycles
Off-State Input–Output Leakage @ 150 V		25	TBD	pA
On-State Resistance		1.0	3.0	Ω
Off-State Capacitance (C_{Off})		90		fF
High Voltage Gate Bias VBB (V_{BB})	78	79	80	V_{DC}
High Voltage Gate Bias VBB Current (I_{BB})		0.05	0.1	mA

[6] The voltage difference between Channel Output (Beam) pin and Supply Voltage Return (VSS) pin must be within ±2.5V. Ideally the VSS pin is tied to a node with the same potential as signal ground. This ties the GATE to ground potential in the off state.

[7] Includes channel settling time and actuator bounce. Recommended 1.0 us GATE pin voltage rise time (10% - 90%).

[8] Specified for 250 Ω load resistance, 25 ºC test conditions.

Table 3 Driver DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Driver Logic Supply VDD Voltage (V_{DD})	4.5	5.0	5.5	V_{DC}
Driver Logic Supply VDD Current in standby (I_{DD})		10	50	uA
Driver Input (DIN) @ VDD=5.0V				
High-Level Logic Voltage V_{IH}	3.5	5.0	5.3	V
Low-Logic Input Voltage V_{IL}	-0.3		0.8	V
High-Logic Input Current I_{IH}			1	uA
Low-Logic Input Current I_{IL}			TBD	uA
Driver Output (DOUT) VDD=4.5V				
High-Level Logic Output V_{OH}[9]	4			V
Low-Level Logic Output V_{OL}[10]			1.0	

Hot Switch Restrictions

The MM1200 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V. Further, the voltage at the channel terminals must be within +/-0.5 V relative to ground.

Floating Node Restrictions

IN/OUT pins must not be allowed to electrically float during switching operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples are:

- Unconnected IN/OUT pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats IN or OUT pins, shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

[9] V_{OH} measured at ID_{OUT} = -0.1 mA.

[10] V_{OL} measured at ID_{OUT} = -0.1 mA.

Table 4 Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	0		5	MHz
Clock Width High and Low t_{WL},t_{WH}	100			ns
Data Setup Time before Clock Rises t_{SU}	50			ns
Data Hold Time after Clock Rises t_H	50			ns
Latch Enable Pulse Width t_{WLE}	100			ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	50			ns
All Logic Inputs t_r, t_f			5	ns

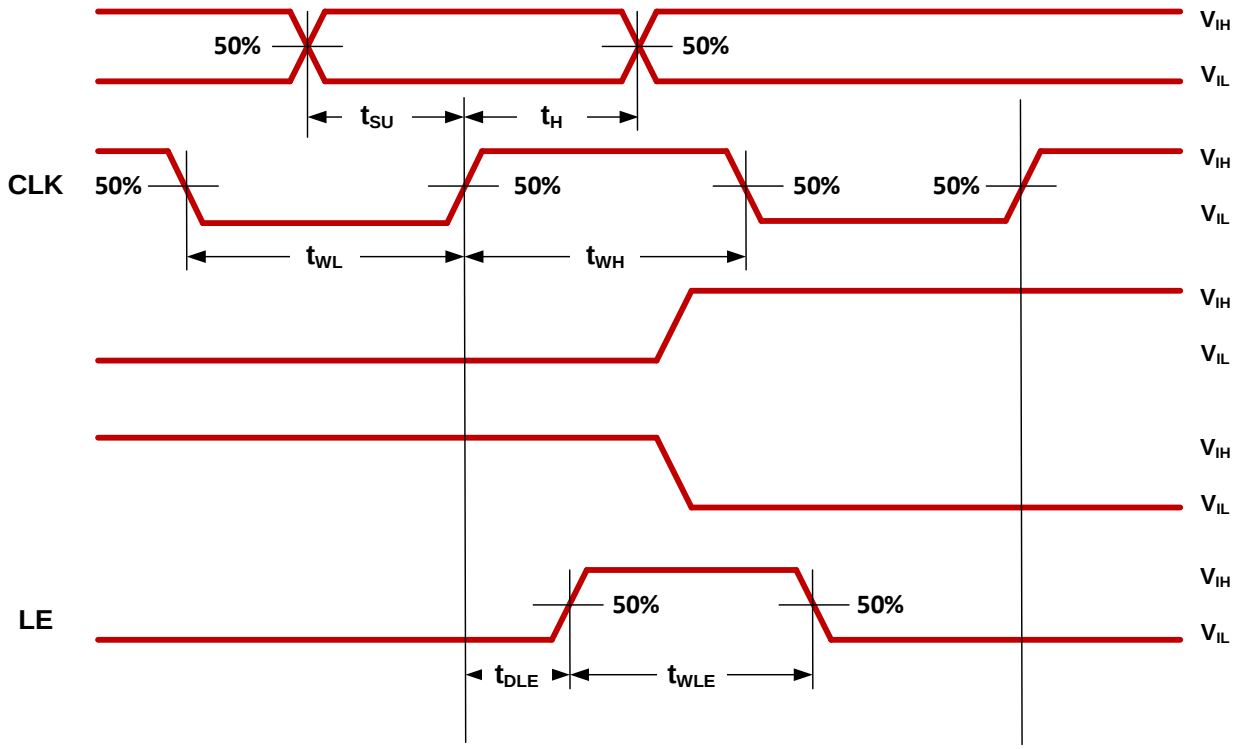


Figure 1: Driver Interface Timing Diagram

Functional Block Diagram

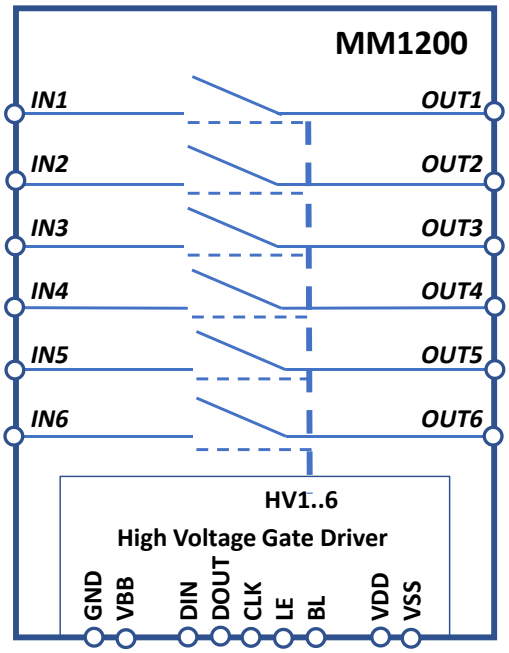
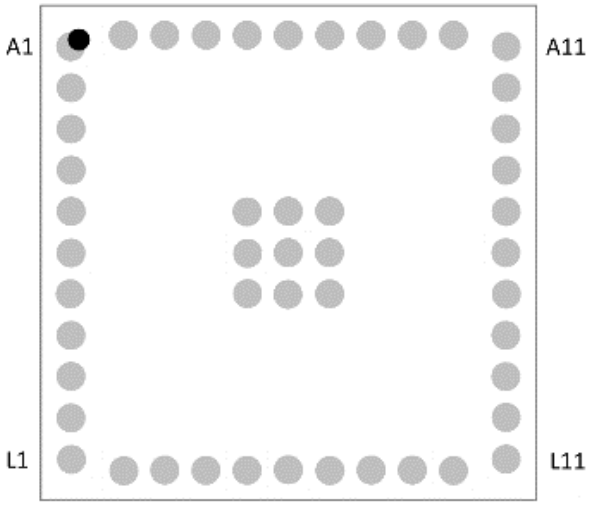


Figure 2: Functional Block Diagram

49-Lead BGA Package Pin Out



Top view / Bump side

Figure 3: Top-Down Pin Layout

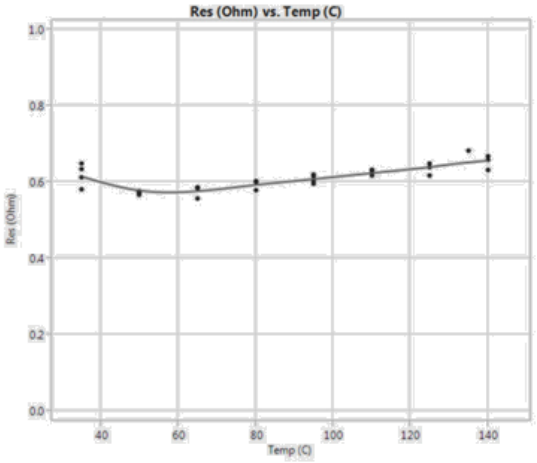
See Table 5 below for detailed pin description.

Table 5 Detailed Pin Description

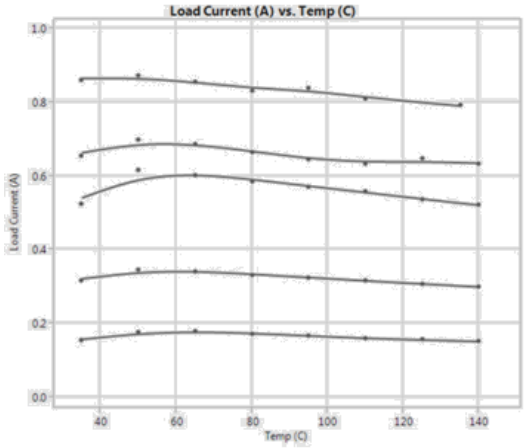
Pin #	Name	Description	Pin #	Name	Description
A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	GND	Ground Reference, internal shield	L9	IN5	Input (Contact 5)
B1	OUT1	Output (Beam 1)	K11	IN6	Input (Contact 6)
D1	BL	All Channels Off	H11	CLK	Driver Clock Input
E1	DIN	Driver Serial Data Input	G11	VSS	Supply Voltage Return
F1, D11	N/C	Do Not Connect	F11	VDD	Driver Logic Supply
G1	VBB	Gate Bias High Voltage Supply	E11	LE	Driver Latch Input
H1	DOUT	Driver Serial Data Output	B11	OUT6	Output (Beam 6)
K1	IN1	Input (Contact 1)	A9	OUT5	Output (Beam 5)
L3	IN2	Input (Contact 2)	A7	OUT4	Output (Beam 4)
L5	IN3	Input (Contact 3)	A5	OUT3	Output (Beam 3)
L7	IN4	Input (Contact 4)	A3	OUT2	Output (Beam 2)

Performance

Typical device performance measured on MM1200-EVK evaluation board.



1. Resistance vs Temperature



2. Load Current vs Temperature

High Voltage Gate Driver Control

Operating Description

The integrated high voltage gate driver is controlled through a serial-to-parallel interface that drives the high voltage gate lines of the channels. Channel control data is shifted into a 10-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 4 below.

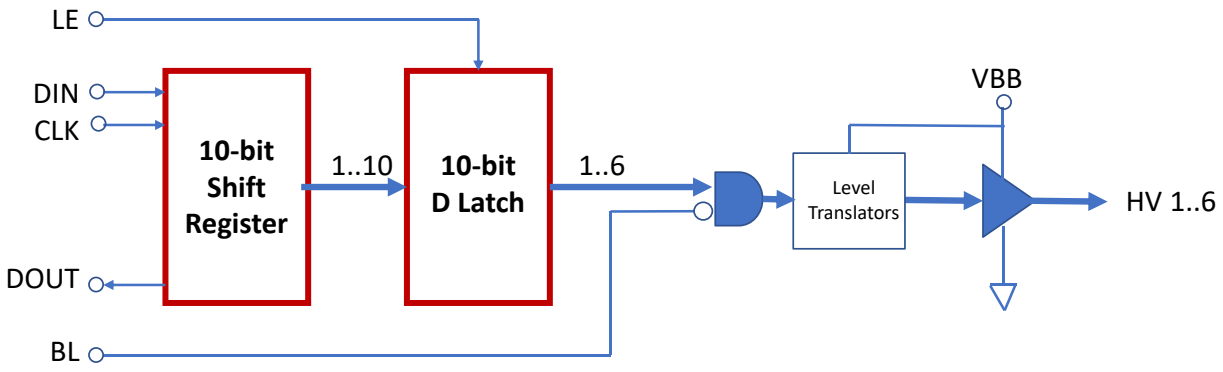


Figure 4: High Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- A 10-bit data byte is serially loaded into shift register bits 1-to-10 on the positive edge of CLK. Shift order is MSB first starting with bit 10.
- Parallel data from the shift register is transferred to the high voltage gate output buffers through a 10-bit D latch when the latch enable input LE is logically high.
- The MM1200 uses only six of the ten data bits latched for channel control. Bits 1 through 6 correspond to high voltage gate lines HV1 through HV6 respectively. Bits 7,8,9 and 10 are not used. Data bits set to logical “1” close the corresponding channel to On and “0” open the channel to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 10-bit words consisting of four dummy bits and six channel control bits so that each data packet controls one channel.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically high. The pin should be logically low for normal operation.

Table 6 Truth Function Table

	Inputs				Shift Register		High Voltage Output HVx	
Function	Data	CLK	LE	BL	1	2…10	1	2 3 - - - - 10
All off (blank)	X	X	X	H	*	*…*	L	L L - - - - L
Load Shift Register	H/L	↑	L	L	H/L	*…*	*	* * - - - - *
Latched	X	X	L	L	*	*…*	*	* * - - - - *
Transfer	H/L	X	H	L	H/L	*…*	H/L	* * - - - - *

Note:

H = High logic level
L = Low logic level
X = Don't care logic level
↑ = Low to high logic transition
* = Dependent on the previous stage's state before the last CLK or last LE high
HVx corresponds to high voltage gate drivers where only HV1..6 are used

Package Drawing

49 Lead Ball Grid Array 0.30mm Ball, 0.50mm Pitch

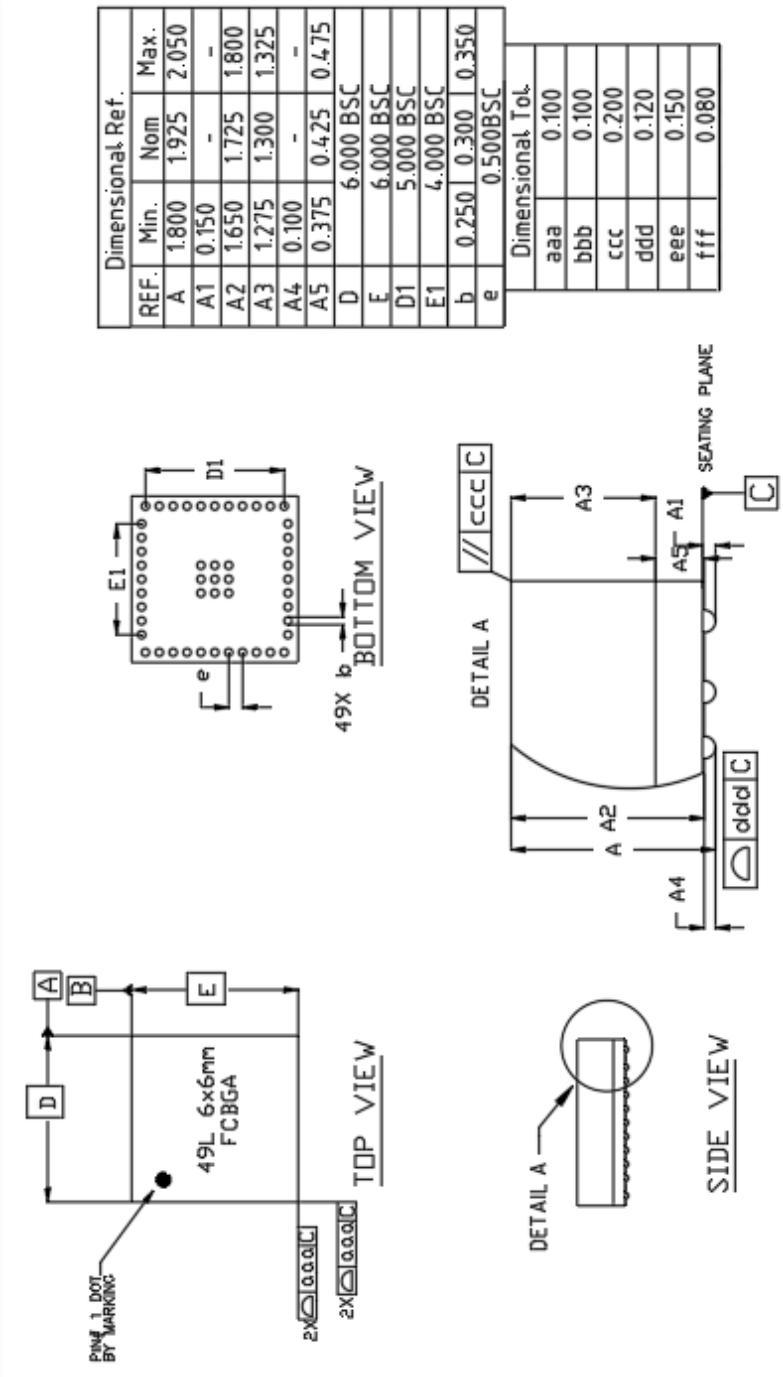


Figure 5 Package Drawing

Recommended PCB Layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram
- Connect GND node (floating shield inside the package) to Signal Ground
- Open space around the package can have grounded thru holes
- ENIG (Electroless Nickel Immersion Gold) pad surface finish
- 20 micron (µm) thick solder mask
- Type 3 or higher solder paste with no clean flux
- Component placement force not to exceed 100 grams

Recommended PCB Pad Pattern

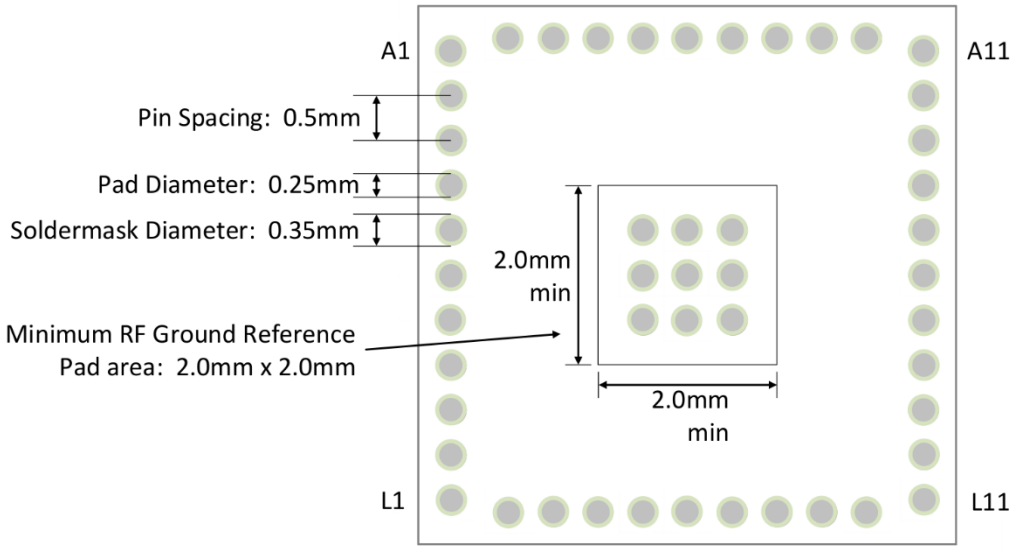
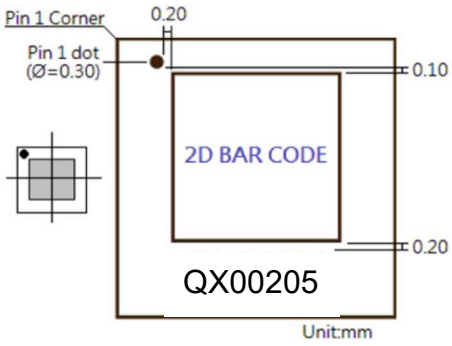


Figure 6: Recommended PCB Pad Pattern

Package Options and Ordering Information

The MM1200 package marking and nomenclature is illustrated in Figure 7 below.



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Device Part Number

Figure 7: Package Marking Drawing

Ordering Information

Part Number	ECCN	Package	Packaging	Temp Range
MM1200-00	EAR99	6mm x 6mm x 2mm BGA	Tray	-40°C to +85°C
MM1200-EVK	EAR99	EVK	N/A	

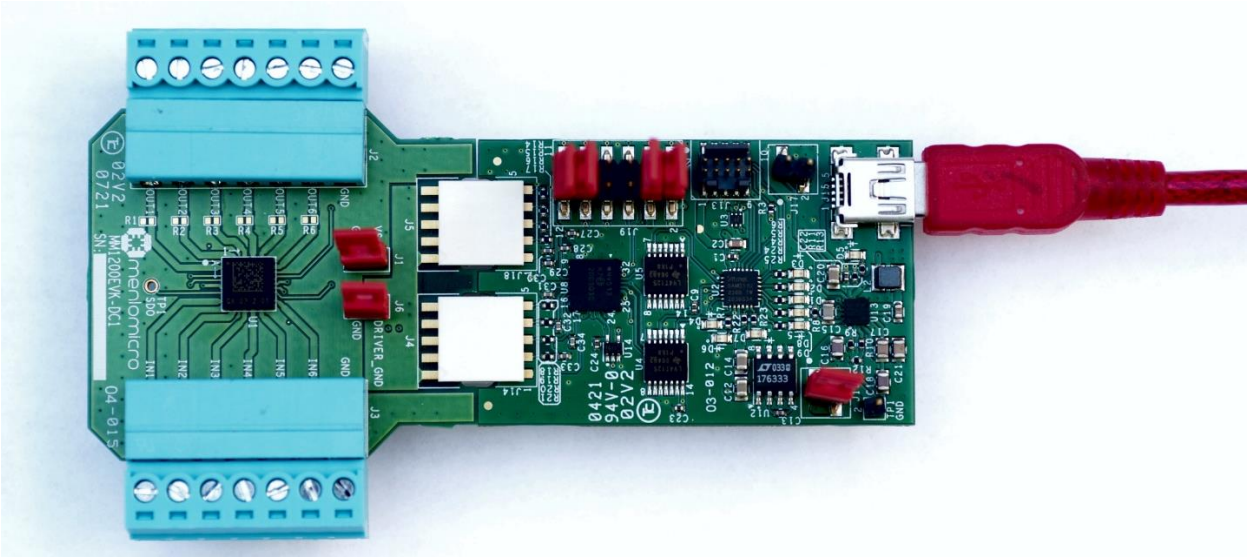


Figure 8: Evaluation Kit (EVK)

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