Preliminary Datasheet
MM1200 – 6 Channel SPST Signal Relay

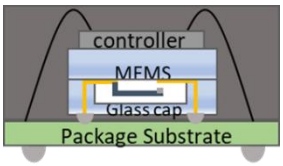
Product Overview

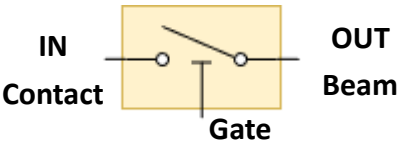
Description

The MM1200 device is a 6-channel SPST Signal Relay intended for signal switching applications in both DC and AC circuits. Each channel provides low on-state contact resistance, high off-state isolation and 3 billion switching cycles. Each channel can be individually controlled by a serial-to-parallel interface that drives the gate lines of the individual channels. The flexibility of six SPST channels enable implementation of different signal topologies such as dual SP3T, triple SP2T or 2x3 matrix. Only an external logic supply and gate bias source are required for operation of the device.

Features

- 1.0 A per channel and 2.0 A per package
- Maximum Voltage (AC peak or DC): +/-150 V on Input
- Low On-State Resistance 1.0 Ω typical per channel
- Input to Output Isolation > 20 G Ω typical
- Switching Time < 10 us typical
- High Reliability > 3 Billion Switching Operations typical
- Integrated driver eliminates need for external gate driver
- 6 mm x 6 mm BGA Package



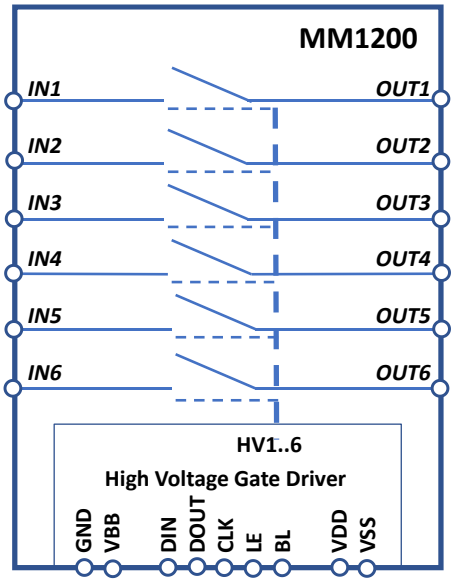


Applications

- High Density Switch Matrices
- Automated Test and Measurement Systems
- Mechanical Relay Replacement

Markets

- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom



RoHS COMPLIANT

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1200 should be restricted to the limits indicated in the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM1200 is a Class 0 ESD device. When handling the MM1200, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Power Sequencing

The following power sequence is recommended to avoid latch-up:

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, remove all inputs, remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present. VBB voltage should not drop below VDD or float during operation.

Table 1 Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (VDD)		7.5	VDC
High Voltage Gate Supply (VBB)		90	VDC
Driver Logic Input Levels	-0.3	VDD + 0.3	V
DC Voltage VBB to OUTx pin (V_{VBB_OUT})	-100	100	V
Off-State Voltage INx to OUTx[2] [3]	-150	150	V
Hot Switching Voltage[4]	-0.5	0.5	V
DC Carry Current / Channel		1.1	A
Total Carry Current per Device		2.2	A
Storage Temperature Range[5]	-65	+150	ºC
ESD Rating HBM Driver Pins[6]		500	V
ESD Rating HBM Channel I/O Pins[7] [8]		150	V
Mechanical Shock[9]		500	G
Vibration[10]		500	Hz

[1] All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied during the on-state condition (cold-switched condition).

[2] This also applies to ESD events. This is a Class 0 device.

[3] The voltage difference between Output (Beam) pin and Supply Voltage Return (VSS) pin should be minimal. Ideally the VSS pin is tied to a node with the same potential as signal ground. This ties the GATE to ground potential in the off state.

[4] See section Hot Switch Restrictions for more information.

[5] See section Recommended Solder Reflow Profile for more information on shelf and floor life.

[6] Driver pins include: CLK, LE, DIN, DOUT, BL, VBB, VDD.

[7] Channel I/O pins include: IN1 to IN6, OUT1 to OUT6.

[8] IN and OUT pins must not be allowed to electrically float during channel operation. See section *Floating Node Restrictions* for details on avoiding floating nodes.

[9] See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis.

[10] See JESD22-B103 for vibration test methodology at 3.1 G and 30min/cycle, 1 cycle/axis, 3 axis.

Table 2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Conditions
Driver Logic Supply VDD Voltage	V_{DD}	4.5	5.5	V_{DC}	
High Voltage Gate Bias VBB	V_{BB}	78	82	V_{DC}	
Operating Temperature Range		-40	+85	ºC	Ambient

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted.

Table 3 DC and AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
AC/DC Carry Current/Channel			1.0	A
Total Carry Current per Device			2.0	A
On-State Output Voltage to GND[11]			13	V_{DC}
Off-State Output Voltage to GND[12]			50	V_{DC}
On / Off Switching and Settling Time[13] Turn on time Turn off time		 8.5 2.5		 µs µs
Full Cycle Frequency			10	kHz
On / Off Channel Operations[14] **(Cold Switched)**		3B		Cycle
Off-State Input-Output Leakage @ 100V		5		nA
Off-State Input-Output Leakage @ 10V		0.3		nA
Off-State Insulation Resistance (R_{Off}) @ 100V		20		GΩ

[11] Voltage at which unintended de-actuation may occur
[12] Voltage at which unintended actuation may occur
[13] Includes any actuator bounce and settling time.
[14] Cold switched operations, measured at 10 kHz cycling rate, specified at 25 C ambient.

Parameter	Minimum	Typical	Maximum	Unit
Off-State Insulation Resistance (R_{Off}) @ 10V		33		GΩ
On-State Resistance		1.0	3.0	Ω
Off-State Capacitance (C_{IO})[15]		45		fF
Channel to Channel Off-State Capacitance (C_{Off})[16] In1 – In2 In1 – In6		 40 2		 fF fF
High Voltage Gate Bias VBB Current (I_{BB})		0.2	1.7	µA

Table 4 Driver DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Driver Logic Supply VDD Current in standby (I_{DD})		10	50	µA
Driver Input (DIN) @ VDD=5.0V High-Level Logic Voltage V_{IH} Low-Logic Input Voltage V_{IL} High-Logic Input Current I_{IH}	 3.5 -0.3	5.0	 5.3 0.8 1	 V V µA
Driver Output (DOUT) VDD=4.5V High-Level Logic Output V_{OH}[17] Low-Level Logic Output V_{OL}[18]	 4 -		 - 1.0	 V

[15] Capacitance between input and output pins measured at 1MHz at 25 C ambient.
[16] Capacitance between channel inputs measured at 1MHz at 25 C ambient.
[17] V_{OH} measured at ID_{OUT} = -0.1 mA.
[18] V_{OL} measured at ID_{OUT} = -0.1 mA.

Table 5 Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	0		5	MHz
Clock Width High and Low t_{WL},t_{WH}	100			ns
Data Setup Time before Clock Rises t_{SU}	50			ns
Data Hold Time after Clock Rises t_H	50			ns
Latch Enable Pulse Width t_{WLE}	100			ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	50			ns
All Logic Inputs t_r, t_f			5	ns

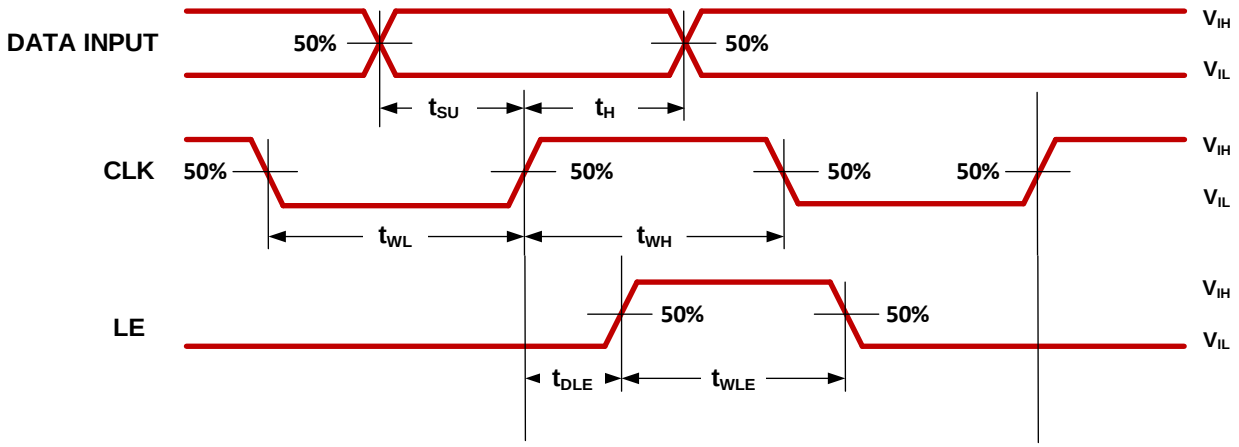


Figure 1: Driver Interface Timing Diagram

Hot Switch Restrictions

The MM1200 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V.

Floating Node Restrictions

IN/OUT pins must not be allowed to electrically float during switching operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples and recommended solutions are:

- Unconnected IN/OUT pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats IN or OUT pins, shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Functional Block Diagram

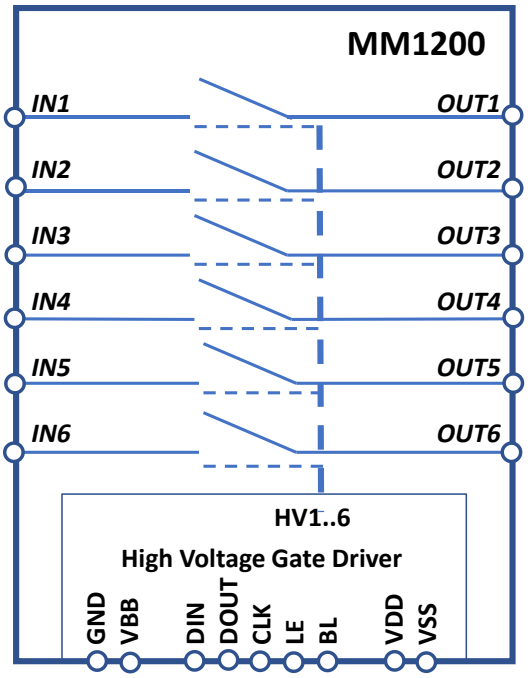


Figure 2: Functional Block Diagram

49-Lead BGA Package Pinout

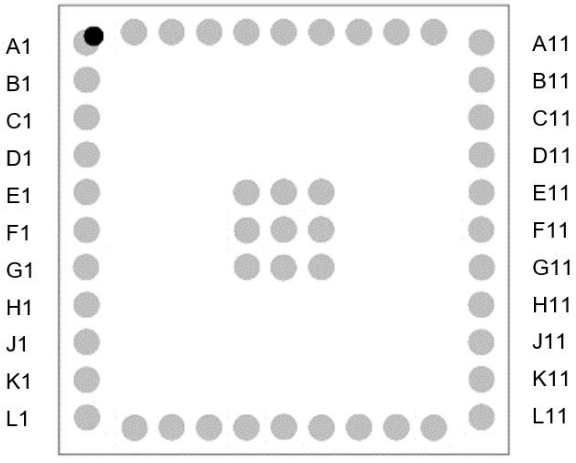


Figure 3: Top View Pin Layout, Solder Balls Down

Dot indicates pin 1. See below for detailed pin description.

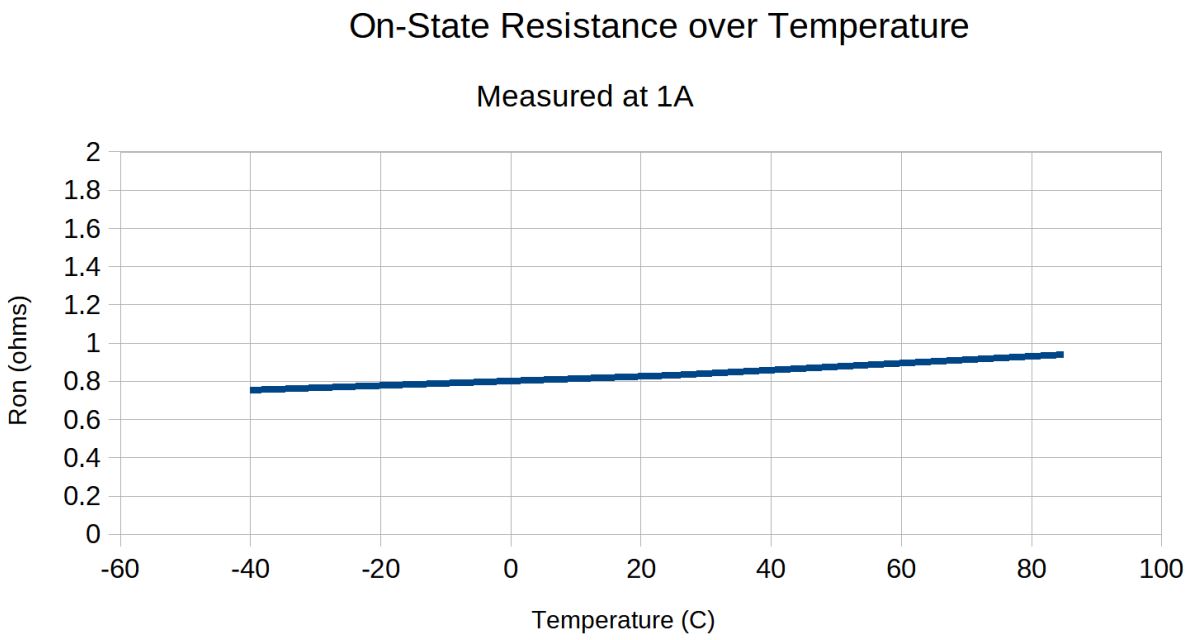
Table 6 Detailed Pin Description

Pin Name	Pin #	Description
GND	A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	Ground Reference, internal shield
VBB	G1	Gate Bias High Voltage Supply
VDD	F11	Driver Logic Supply
VSS	G11	Supply Voltage Return
IN1	K1	Input (Contact 1)
IN2	L3	Input (Contact 2)
IN3	L5	Input (Contact 3)
IN4	L7	Input (Contact 4)
IN5	L9	Input (Contact 5)
IN6	K11	Input (Contact 6)
OUT1	B1	Output (Beam 1)
OUT2	A3	Output (Beam 2)
OUT3	A5	Output (Beam 3)
OUT4	A7	Output (Beam 4)
OUT5	A9	Output (Beam 5)
OUT6	B11	Output (Beam 6)
DIN	E1	Driver Serial Data Input
DOUT	H1	Driver Serial Data Output
CLK	H11	Driver Clock Input
LE	E11	Driver Latch Input
BL	D1	All Channels Off
N/C	F1, D11	Do Not Connect

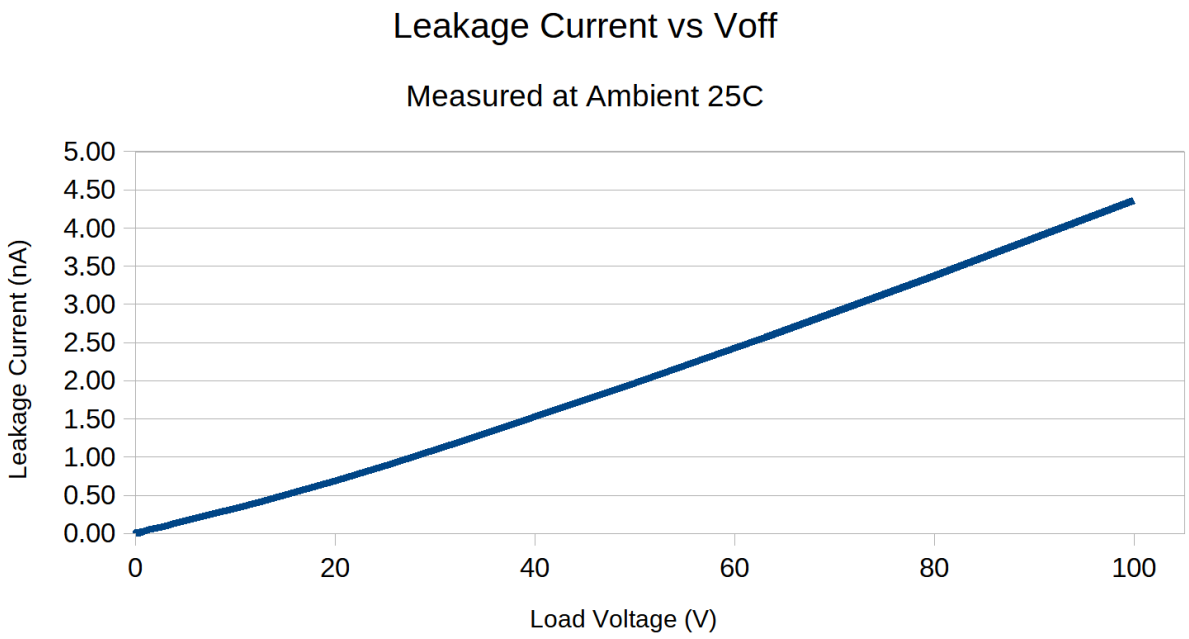
Performance

Typical device performance measured on MM1200-EVK evaluation board.

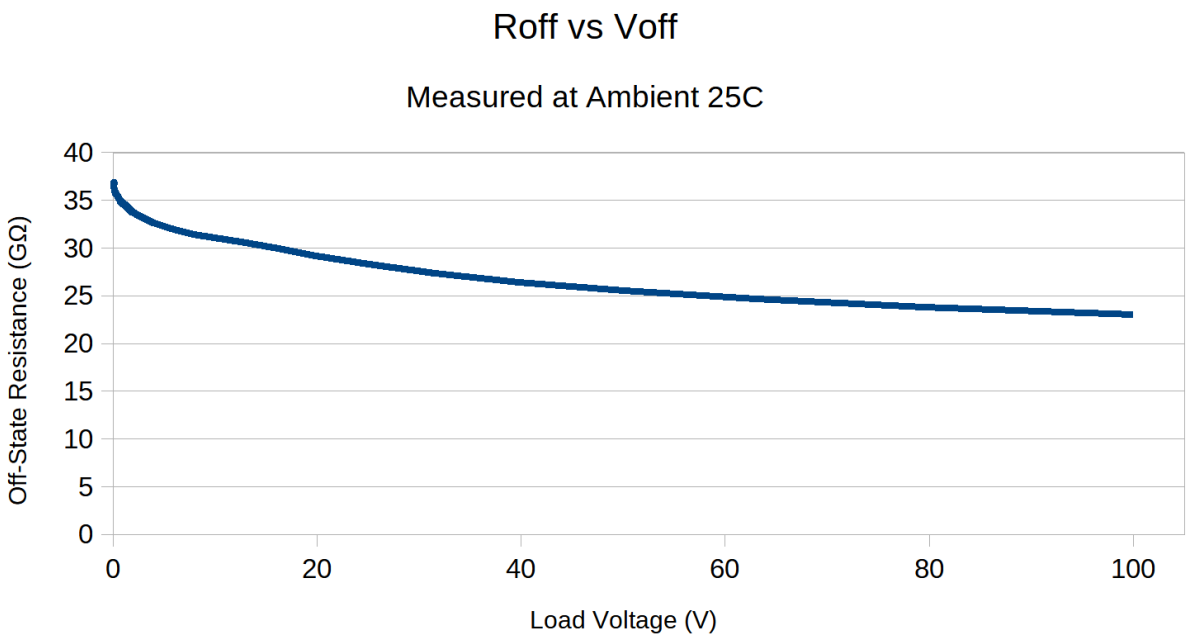
1. On-State Resistance over Temperature



2. Off-State Input-Output Leakage Current vs Voff



3 Off-State Input-Output Resistance



High Voltage Gate Driver Control

Operating Description

The integrated high voltage gate driver is controlled through a serial-to-parallel interface that drives the high voltage gate lines of the channels. Channel control data is shifted into a 10-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 4 below.

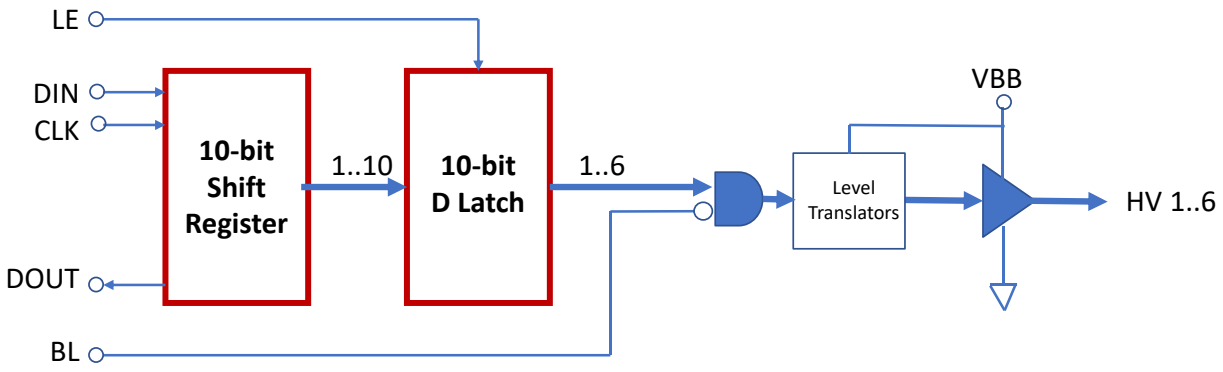


Figure 4: High Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- A 10-bit data byte is serially loaded into shift register bits 1-to-10 on the positive edge of CLK. Shift order is MSB first starting with bit 10.
- Parallel data from the shift register is transferred to the high voltage gate output buffers through a 10-bit D latch when the latch enable input LE is logically high.
- The MM1200 uses only six of the ten data bits latched for channel control. Bits 1 through 6 correspond to high voltage gate lines HV1 through HV6 respectively. Bits 7,8,9 and 10 are not used. Data bits set to logical “1” close the corresponding channel to On and “0” open the channel to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 10-bit words consisting of four dummy bits and six channel control bits so that each data packet controls one device.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically high. The pin should be logically low for normal operation.

Table 7 Truth Function Table

	Inputs				Shift Register		High Voltage Output HVx	
Function	Data	CLK	LE	BL	1	2…10	1	2 3 - - - - 10
All off (blank)	X	X	X	H	*	*…*	L	L L - - - - L
Load Shift Register	H/L	↑	L	L	H/L	*…*	*	* * - - - - *
Latched	X	X	L	L	*	*…*	*	* * - - - - *
Transfer	H/L	X	H	L	H/L	*…*	H/L	* * - - - - *

Note:

H = High logic level
L = Low logic level
X = Don't care logic level
↑ = Low to high logic transition
* = Dependent on the previous stage's state before the last CLK or last LE high
HVx corresponds to high voltage gate drivers where only HV1..6 are used

Package Drawing

49 Lead Ball Grid Array 0.30mm Ball, 0.50mm Pitch

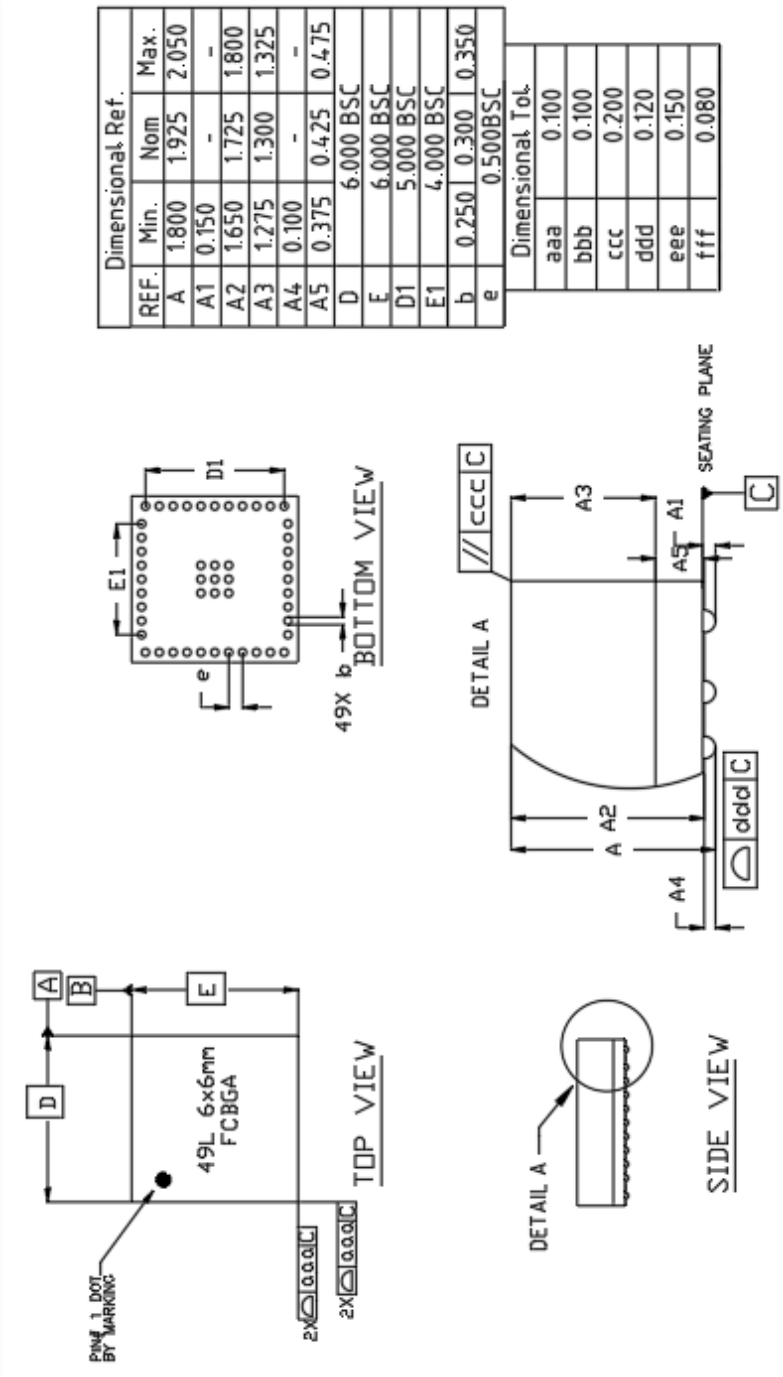


Figure 5 Package Drawing

Recommended PCB Layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram
- Connect GND node (floating shield inside the package) to Signal Ground
- Open space around the package can have grounded thru holes
- ENIG (Electroless Nickel Immersion Gold) pad surface finish
- 20 micron (µm) thick solder mask
- Type 3 or higher solder paste with no clean flux
- Component placement force not to exceed 100 grams

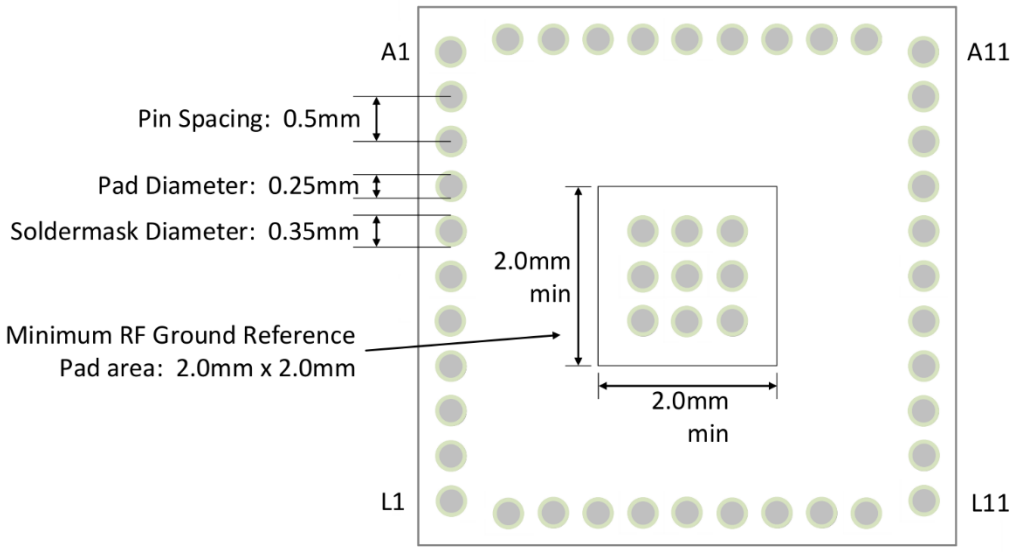


Figure 6: Recommended PCB Pad Pattern

Recommended Solder Reflow Profile

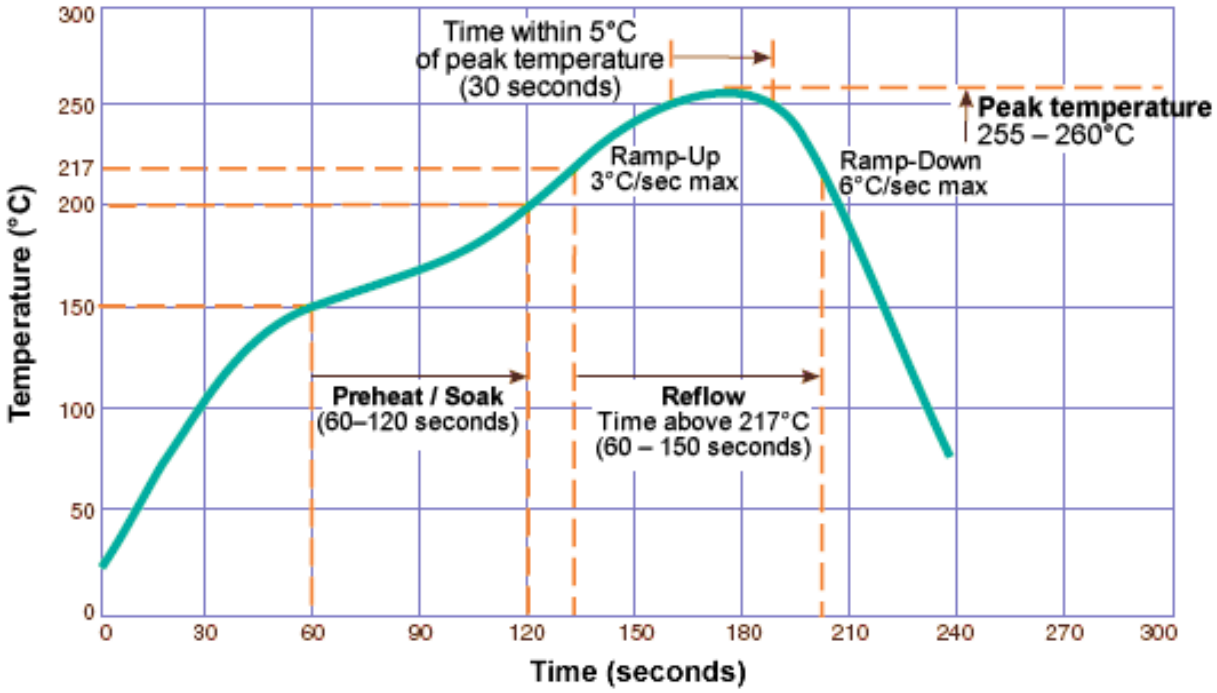


Figure 7: Reflow Profile

Follow Moisture Sensitivity Level (MSL) 5 handling precautions specified in IPC/JEDEC J-STD-020.

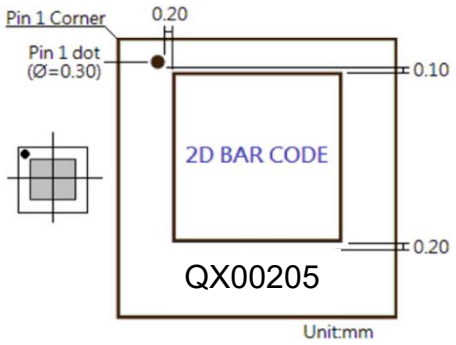
Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags the following is recommended:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 32 months or less.

Package Options and Ordering Information

The MM1200 package marking and nomenclature is illustrated in Figure 8 below.



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Device Part Number

Figure 8: Package Marking Drawing

Package Materials Information

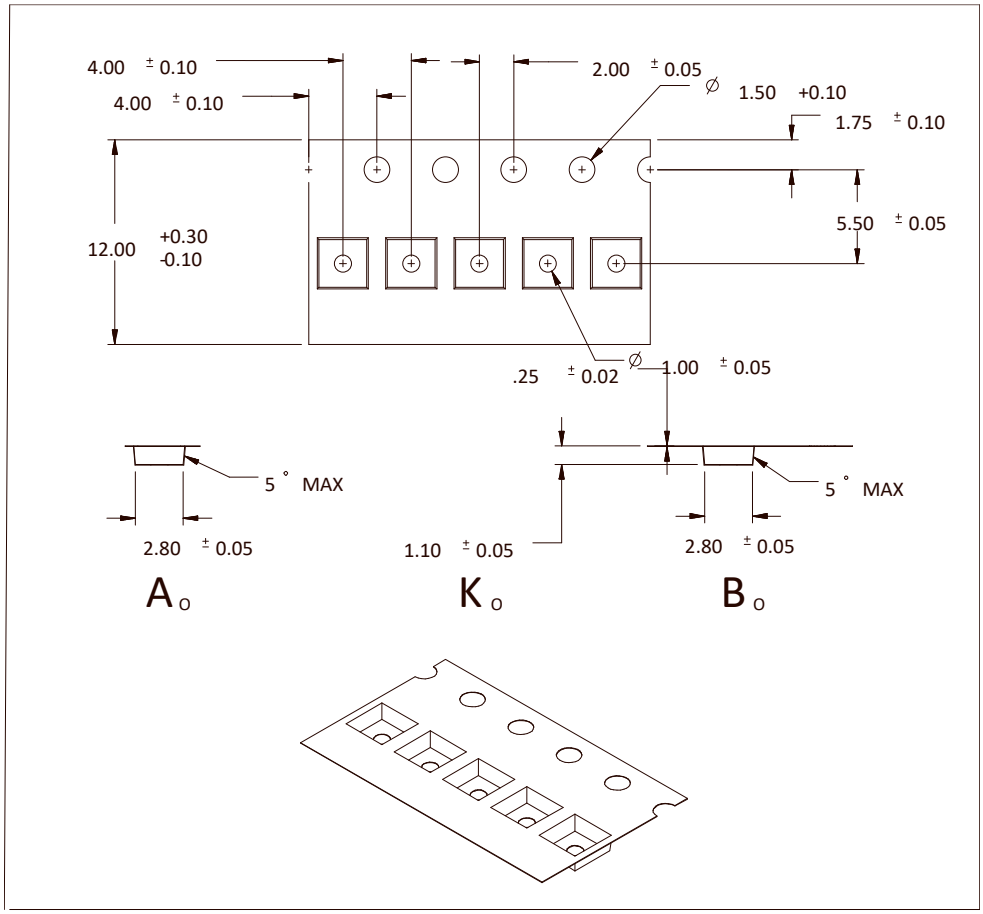


Figure 9: Tape and Reel Drawing

Ordering Information

Part Number	ECCN	Package	Temp Range
MM1200-00NDB	EAR99	150V/1A - 6xSPST - 6mm x 6mm BGA; Industrial Temp with 3B Cycles Mechanical Endurance at 25°C	-40°C to +85°C
MM1200-00NDB-TR		150V/1A - 6xSPST - 6mm x 6mm BGA; Industrial Temp with 3B Cycles Mechanical Endurance at 25°C, Tape and Reel (Qty 250)	
MM1200-EVK	EAR99	EVK	

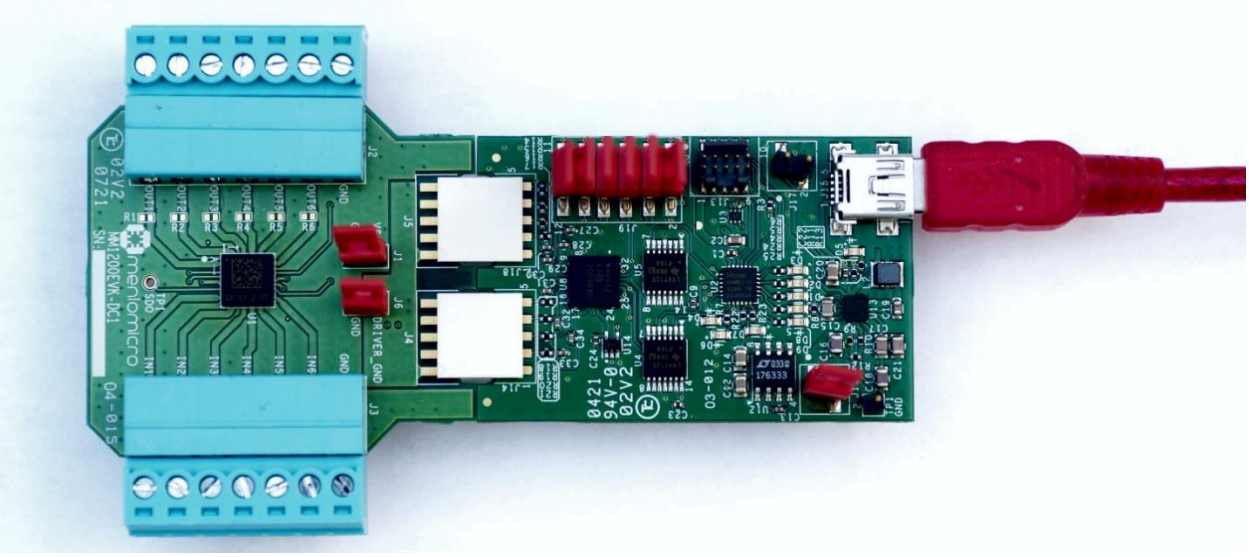


Figure 10: Evaluation Kit (EVK)

Important Information

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