



## Preliminary Datasheet

# MM5120 DC – 12 GHz RF SP4T with Integrated Driver

## Product Overview

### Description

The MM5120 is a high-power SP4T switch built on Menlo Micro's Ideal Switch technology. This innovative technology enables highly reliable switches capable of greater than 25 W forward power. The MM5120 provides ultra-low insertion loss and superior linearity as an SP4T from DC to 12 GHz, with greater than 3 billion switching cycles. The MM5120 is an ideal solution for replacing large RF electromechanical relays, as well as RF/microwave solid-state switches in applications where linearity and insertion loss are critical parameters. The MM5120 features an integrated driver circuit with SPI or parallel interface control options and an integrated charge pump to drive the gate.

### Features

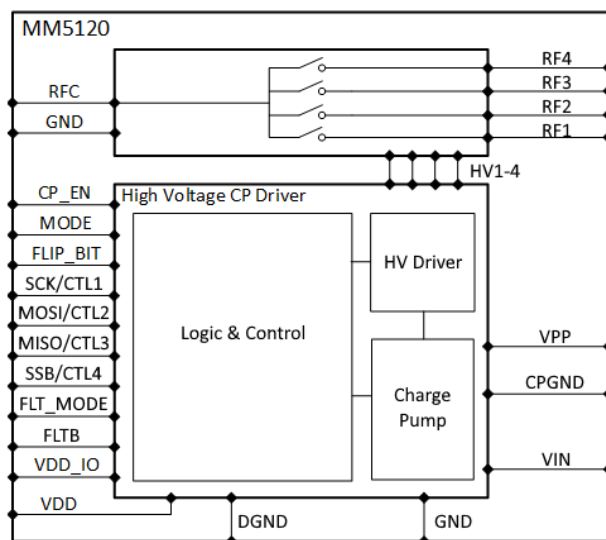
- DC to 12 GHz Frequency Range
- Integrated High-Voltage Driver
- 25 W (CW), 150 W (Pulsed) Max Power Handling
- Low On-State Insertion Loss: 0.4 dB @ 6.0 GHz
- High Linearity, IIP3 > 90 dBm
- 25 dB Isolation @ 6.0 GHz
- Very Low Current Consumption <1mA
- High Reliability > 3 billion Switching Operations
- 5.2 mm x 4.2 mm LGA Package

### Markets

- Defense and Aerospace
- Test and Measurement
- Wireless Infrastructure

### Applications

- Switched Filter Banks and Tunable Filters
- High Power RF Front-Ends
- Low-Loss Switch Matrices
- RF EM Relay Replacement
- Antenna Tuning
- Antenna Beam Steering
- Digital Step Attenuators



## Electrical Characteristics

### Operating Characteristics

#### Absolute Maximum Ratings

Exceeding the maximum ratings as listed in **Table 1** below may reduce the reliability of the device or cause permanent damage. Operation of the MM5120 should be restricted to the limits indicated in Tables 2, 3 and 4 recommended operating conditions listed below.

#### Electrostatic Discharge (ESD) Safeguards

The MM5120 is a Class 0 ESD device. When handling the MM5120, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

**Table 1** Absolute Maximum Ratings<sup>1</sup>

Parameter	Minimum	Maximum	Unit
CW Input Power @ 6 GHz		25	W
Peak Input Power @ 6 GHz		150	W
Open State Voltage Rating / Switch RF1-4 to RFC <sup>2</sup>	-150	150	V
Open State Voltage RF1-RF4, RFC to GND <sup>2</sup>	-150	150	V
DC Supply Voltage (VDD)	-0.3	3.6	V
I/O Supply Voltage (VDD_IO)	-0.3	5.5	V
Charge Pump Input (VIN)	-0.3	5.5	V
Charge Pump High Voltage Output (VPP)	-0.3	105	V
DC Current Rating / Switch		500	mA
Operating Temperature Range	-40	85	°C

<sup>1</sup> All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition).

<sup>2</sup> This also applies to ESD events. This is a Class 0 device.

<b>Storage Temperature Range</b>	-65	150	°C
<b>ESD Rating HBM RF Pins<sup>3</sup></b>		150	V
<b>ESD Rating HBM Control and Power Pins<sup>4</sup></b>		2000	V
<b>ESD Rating HBM VPP Pin</b>		1000	V
<b>Mechanical Shock</b>		TBD	G
<b>Vibration</b>		TBD	Hz

### Recommended Operating Conditions

All specifications valid over full supply voltage and operating temperature range unless otherwise noted. Operating with all RF, analog, and digital GND pins connected to system ground (0 V) and with input frequencies of greater than 10 MHz in a 50  $\Omega$  impedance system.

**Table 2 DC and AC Electrical Specifications**

Parameter	Minimum	Typical	Maximum	Unit
<b>Operating Frequency Range</b> Normal SP4T mode	DC		12	GHz
<b>CW Power @ 6 GHz<sup>5</sup></b>			25	W
<b>Peak Power @ 6 GHz<sup>6</sup></b>			150	W
<b>Insertion Loss</b> @ 6 GHz @ 12 GHz		0.35 0.7		dB

<sup>3</sup> RF pins include: R1, RF2, RF3, RF4, and RFC.

<sup>4</sup> Control and power pins include: VIN, VDD, VDD\_IO, FLT\_MODE, FLTB, FLIP\_BIT, CP\_EN, MODE, and VCTL1-4.

<sup>5</sup> Measured at +85°C.

<sup>6</sup> For 10 % Duty Cycle and 10  $\mu$ s pulse width, measured at +85°C.



<b>Input / Output Return Loss</b>				
@ 6 GHz		17		dB
@ 12 GHz		11		
<b>Isolation</b>				
@ 6 GHz		25		dB
@ 12 GHz		18		
<b>Channel to Channel Isolation @ 6 GHz</b>		25		dB
<b>Third-Order Intercept Point (IP3)<sup>7</sup></b>		> 90		dBm
<b>Second Harmonic (H2)<sup>8</sup></b>		-130		dBc
<b>Third Harmonic (H3)<sup>8</sup></b>		-130		dBc
<b>Charge Pump Noise</b>		-130		dBm
<b>Switching Time<sup>9</sup></b>				
Turn on time		8.5	16	μs
Turn off time		2.5	6	
<b>Full Cycle Frequency</b>			10	kHz
<b>Cold Switch Operations<sup>10</sup></b>	3x10 <sup>9</sup>			Cycles
<b>Hot Switch Operations<sup>11</sup></b>				
at TBD dBm		TBD		Cycles
<b>DC Steady State Carry Current</b>			500	mA
<b>Off-State RFC to RF# Leakage Current</b>		15	150	nA
<b>On-State Resistance (R<sub>on</sub>)</b>		1.2		Ω
<b>Off-State Capacitance (C<sub>off</sub>)</b>		TBD		fF
<b>Video Feedthrough<sup>12</sup></b>		16		mV <sub>Peak</sub>

<sup>7</sup> Measured at +25°C.

<sup>8</sup> Measured at 1.0 GHz and 2.0 GHz fundamental frequency and 35 dBm input power.

<sup>9</sup> Switching time measured from 50% gate voltage to settling to within 0.05 dB of final value.

<sup>10</sup> Measured at 5kHz cycling rate.

<sup>11</sup> Measured at 3 GHz, and TBD cycling rate.

<sup>12</sup> Performed with 1 MΩ termination.

**Table 3** Charge Pump and Driver Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Charge Pump Power Supply (VIN)	4.5	5.0	5.5	V
VIN Current (Dynamic) <sup>13</sup> (I <sub>VIND</sub> )		1.6	TBD	mA
VIN Quiescent Current <sup>14</sup> (I <sub>VINQ</sub> )		0.8	TBD	mA
Charge Pump High-Voltage Output <sup>15</sup> (VPP)	-	-	100	V
Low Voltage Digital Supply (VDD)	3.0	3.3	3.6	V
VDD UVLO Rising Threshold (UVLO <sub>RISE</sub> )	2.77	-	2.95	V
VDD UVLO Falling Threshold (UVLO <sub>FALL</sub> )	2.72		2.90	V
Low Voltage Digital Current <sup>16</sup> (IDD)	-	400	TBD	μA
Low Voltage Digital Quiescent Current <sup>17</sup> (IDD <sub>Q</sub> )	-	350	TBD	μA
Low Voltage Digital Sleep Mode Current <sup>18</sup> (IDD <sub>SLEEP</sub> )	-	10	TBD	μA
Logic Reference Level (VDD_IO)	1.71	-	5.25	V
Fault Indicator Open-Drain Output (FLT <sub>B</sub> )	0	-	VDD_IO	V
Logic I/O Level High (I/O <sub>VH</sub> )	0.7*VDD_IO	-	VDD_IO	V
Logic I/O Level Low (I/O <sub>VL</sub> )	0	-	0.3*VDD_IO	V

<sup>13</sup> SPI mode, Charge pump on, OCS open, Outputs switching at 10 kHz, C<sub>Load</sub> = 2 pF (per output).

<sup>14</sup> Charge pump on, all I/O and outputs static.

<sup>15</sup> VPP requires a filter capacitor with a voltage rating derated to twice the maximum VPP.

<sup>16</sup> SPI mode, Outputs Switching at 10 kHz, OCS=OPEN, CL = 2 pF (per channel).

<sup>17</sup> Charge pump On, All I/O & RF channels static.

<sup>18</sup> Charge pump Off, SPI and inputs in static state.

<b>SDO Load Capacitance (<math>C_{SDO}</math>)<sup>19</sup></b>	-	-	10	pF
<b>SDO Source/Sink Current (<math>I_{SDO}</math>)</b>	10	-	-	mA
<b>CP_EN pin toggle low time<sup>20</sup> (<math>T_{TOGGLE}</math>)</b>	500	-	-	ns
<b>FLT pin max sink current<sup>21</sup></b>	300			$\mu$ A
<b>Logic I/O Hysteresis (SCK only) (<math>I/O_{VH}</math>)</b>	-	0.25	-	V
<b>Start-Up Time<sup>22</sup> (<math>T_{ST}</math>)</b>	-	21	TBD	ms
<b>Power-On-Reset<sup>23</sup> POR</b>	-	0.1	TBD	ms

<sup>19</sup> Specification is for design guidance only. SDO load capacitance is SDI input capacitance pin and PCB trace capacitance from SDO to SDI.

<sup>20</sup> Minimum time CP\_EN has to be held low to re-start the IC from fault condition.

<sup>21</sup> FLT active low.

<sup>22</sup> CP\_EN=1 (CPEN bit=1) to VPP rises to 90% of set value.

<sup>23</sup> Time for logic input signals to be considered valid after application of VIN and VDD.

**Table 4** Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
SPI Clock Frequency SCK	-	-	33	MHz
SDI Valid to SCK Setup Time ( $t_{SU}$ )	2	-	-	ns
SDI Valid to SCK Hold Time ( $t_{HD}$ )	5	-	-	ns
SCK High Time ( $t_{HI}$ )	15.5	-	-	ns
SCK Low Time ( $t_{LO}$ )	15.5	-	-	ns
SSB Pulse Width ( $t_{CSH}$ )	TBD	-	-	ns
LSB SCK to SSB High ( $t_{CSHLD}$ )	15	-	-	ns
SSB Low to SCK High ( $t_{CSSU}$ )	15	-	-	ns
SDO Propagation Delay from SCK Falling Edge ( $t_{SDOH}$ )	10	-	-	ns
SDO Output Valid after SSB Low ( $t_{CSDO}$ )	20	-	-	ns
SSB Inactive to SDO High Impedance ( $t_{SDOZ}$ )	-	-	10	ns

See Programming section for driver interface timing diagrams and details.

## Functional Block Diagram

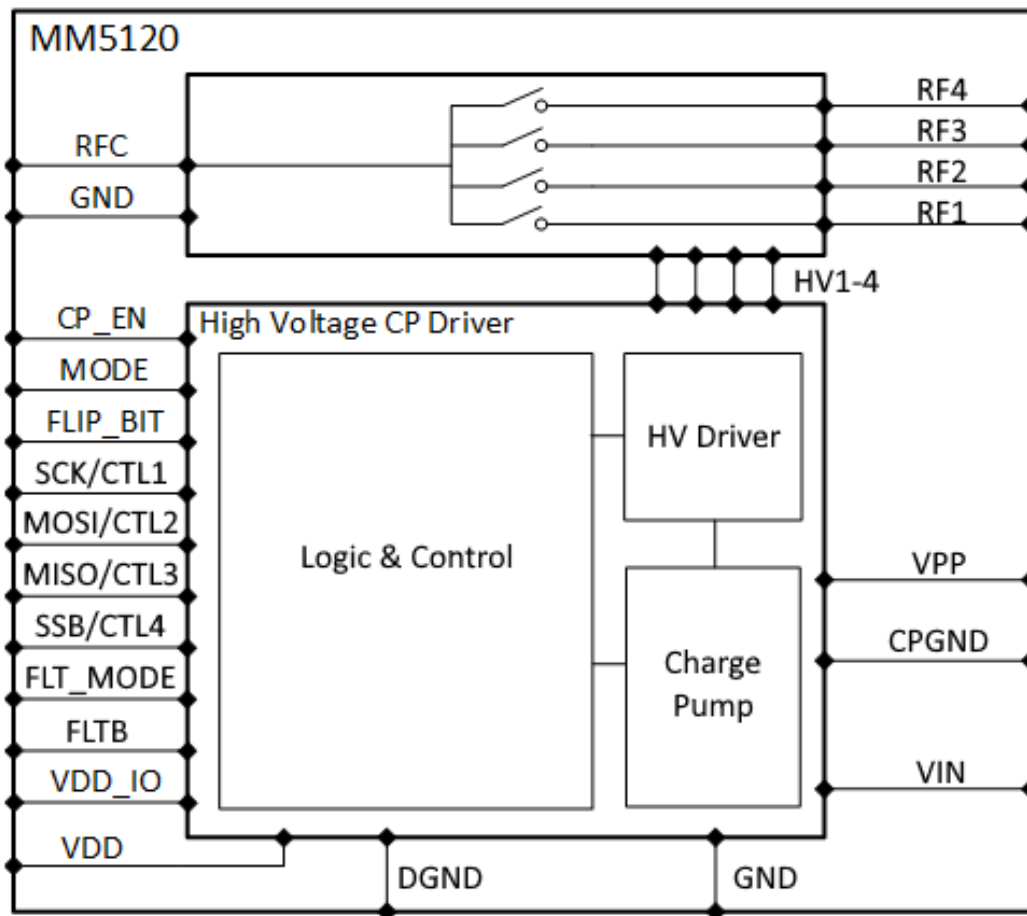


Figure 1: Functional Block Diagram





## Package / Pinout Information

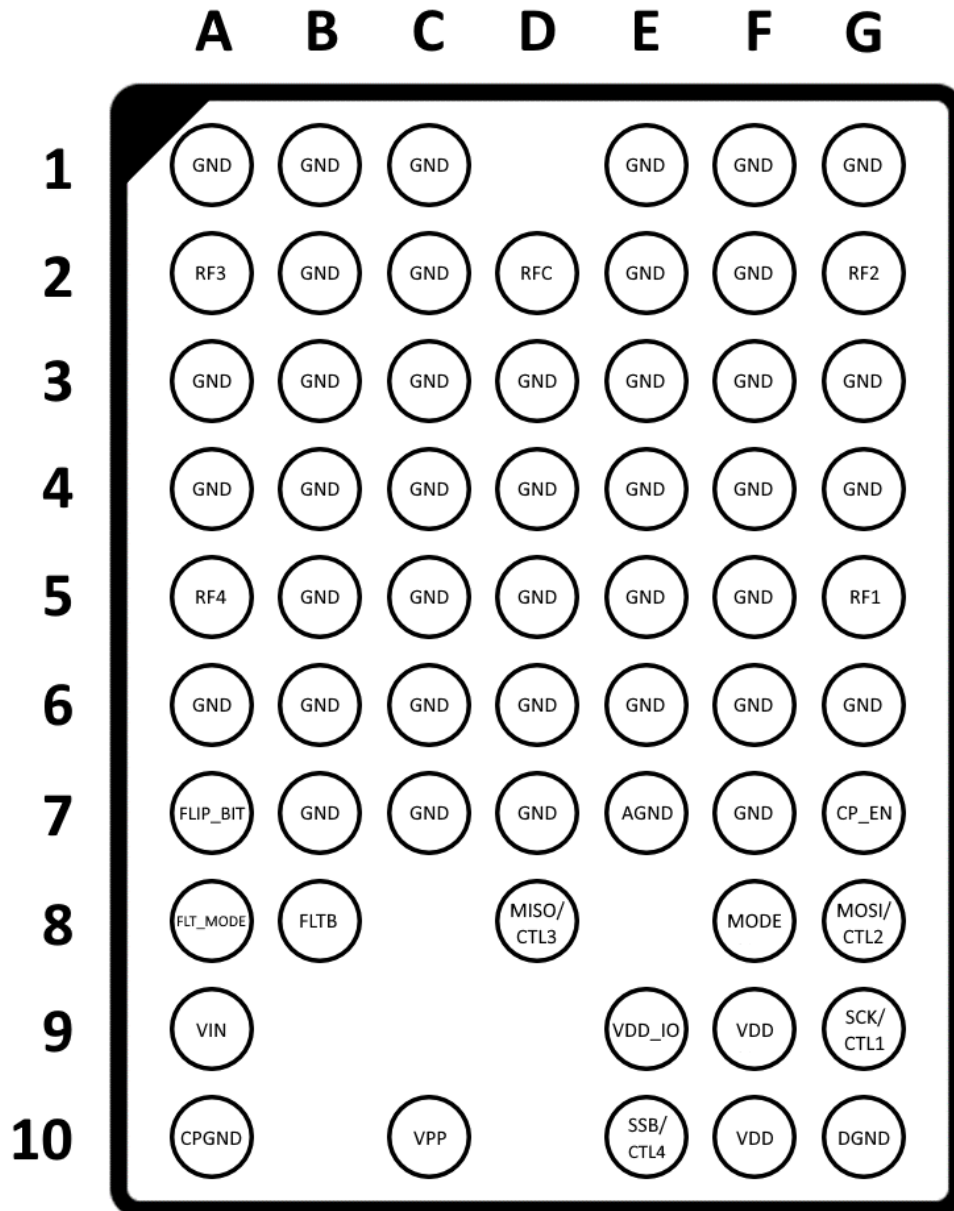


Figure 2: MM5120 5.2 mm x 4.2 mm LGA package pinout (Top View/As Mounted)

**Table 5** Detailed Pin Description

Pin #	Pin Name	Description
A1, A3, A4, A6, B1-B7, C1-C7, D3-D7, E1-E6, F1-F7, G1, G3, G4, G6	GND	Connect to common ground. These pins are internally connected to the RF ground reference.
A2	RF3	RF 3 (Contact)
A5	RF4	RF 4 (Contact)
A7	FLIP_BIT	This pin has an internal pull-down resistor. In SPI mode, spread spectrum is enabled if high.  In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and RF1-4. When FLIP_BIT is low, CTL1 enables RF1 when high, and so on for CTL2-4. When FLIP_BIT is high, refer to <b>Table 6</b> .
A8	FLT_MODE	Fault Mode select in GPIO mode. Pull to VDD to disable Fault Mode. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
A9	VIN	Connect to 5 V power supply. Bypass with a low ESR 1 $\mu$ F ceramic capacitor. See TBD app note if using external high-voltage supply.
A10	CPGND	Charge pump ground, should be connected to PCB ground.
B8	FLT_B	Fault indicator in GPIO and SPI modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when fault is detected. Can be left open if not used.  Pull-up voltage must be $\leq$ VDD_IO.
C10	VPP	High-voltage input to the output drivers. Bypass with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor, to the CPGND pin..
D2	RFC	RF common input.
D8	MISO/CTL3	SPI data output in SPI mode; RF3 channel enable in GPIO mode. Has an internal pull-down resistor.
E7	AGND	Analog ground, should be connected to PCB ground.



Pin #	Pin Name	Description
<b>E9</b>	VDD_IO	For 3.3 V nominal digital I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). Bypass with a low ESR 1 $\mu$ F ceramic capacitor if separate from VDD.
<b>E10</b>	SSB/CTL4	Chip select in SPI mode; RF4 channel enable in GPIO mode. Has an internal pull-up resistor in SPI mode, and an internal pull-down resistor in GPIO mode.
<b>F8</b>	MODE <sup>24</sup>	Logic level input to switch inputs between SPI and GPIO modes. MODE = 0 is SPI mode. MODE = 1 is GPIO mode.
<b>F9, F10</b>	VDD	3.3 V nominal input to digital logic and internal level translators. Bypass with a low ESR 1 $\mu$ F ceramic capacitor.
<b>G2</b>	RF2	RF 2 (Contact)
<b>G5</b>	RF1	RF 1 (Contact)
<b>G7</b>	CP_EN	Charge pump enable pin in GPIO mode. Pull-up to VDD to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
<b>G8</b>	MOSI/CTL2	SPI data input in SPI mode; RF2 channel enable in GPIO mode. Has an internal pull-down resistor.
<b>G9</b>	SCK/CTL1	Clock input in SPI mode; RF1 channel enable in GPIO mode. Has an internal pull-down resistor.
<b>G10</b>	DGND	Digital ground, should be connected to PCB ground.

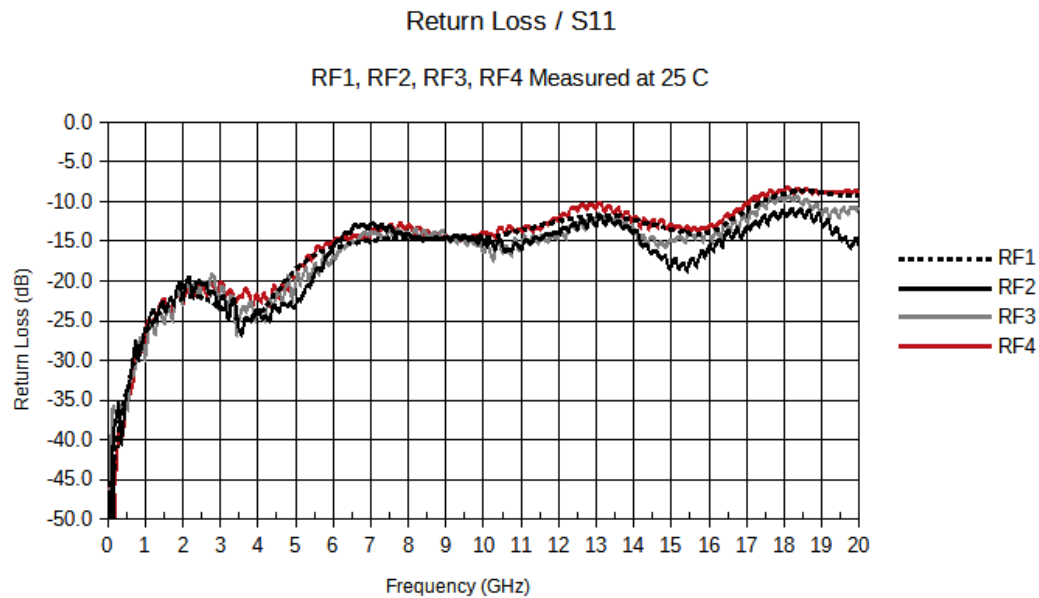
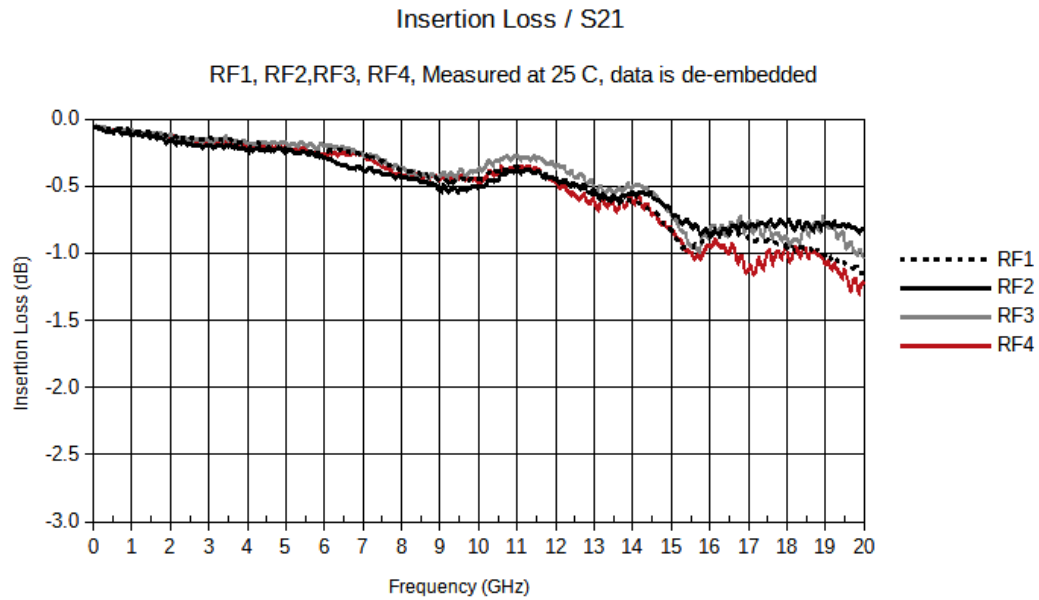
<sup>24</sup> MODE should be tied to GND or VDD\_IO if the use case is SPI or GPIO control, respectively.



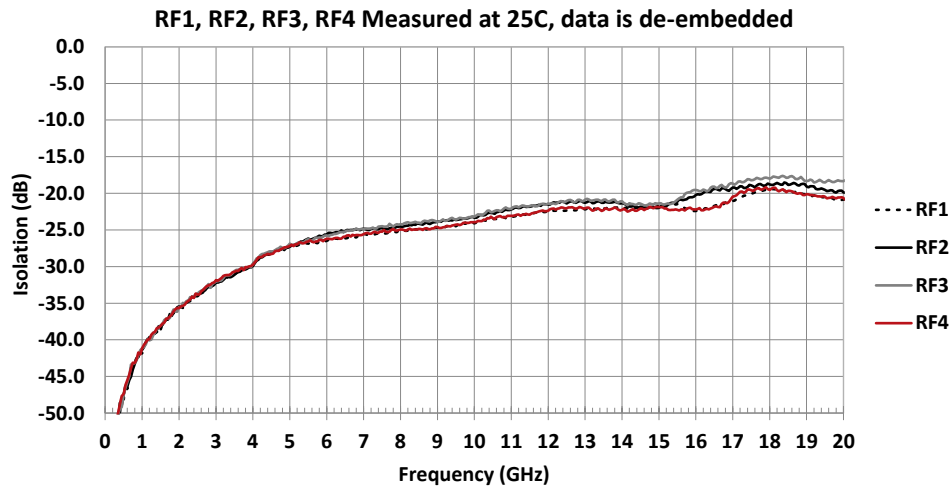
## RF Performance

### Normal Mode (SP4T)

Typical device performance measured on MM5120 evaluation board, de-embedded.

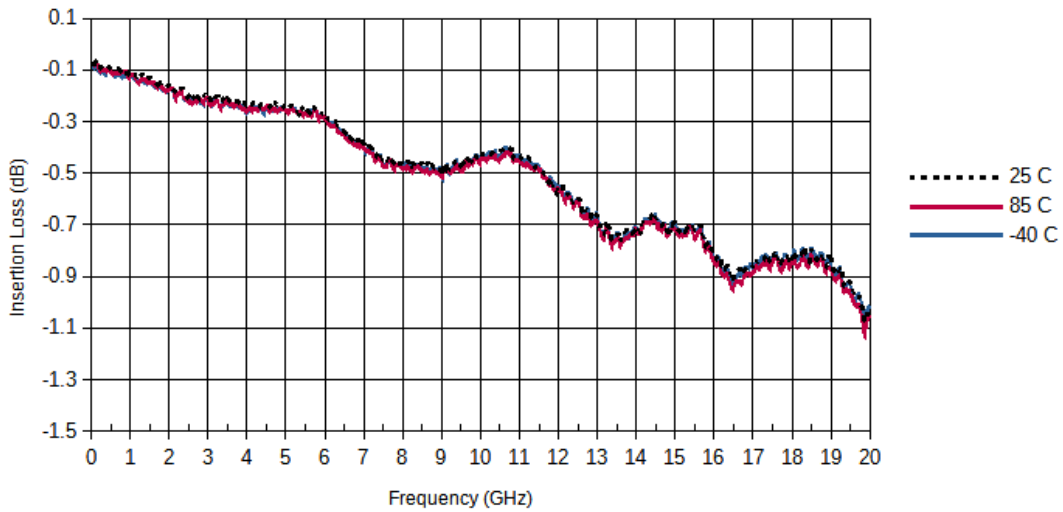


Off-State Isolation / S21



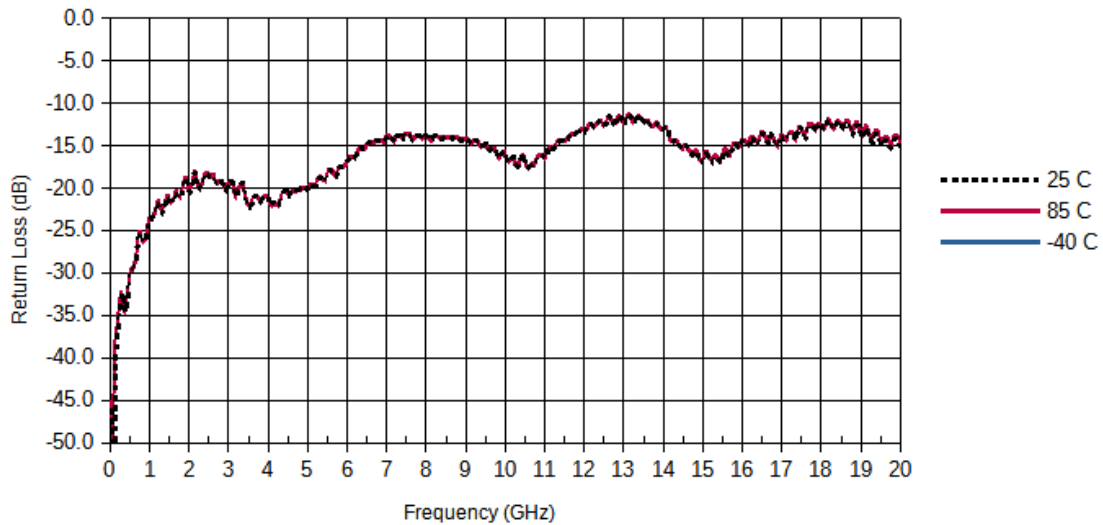
Insertion Loss / S21 for 25 C, 85 C and -40 C

For channel RF2, data is de-embedded



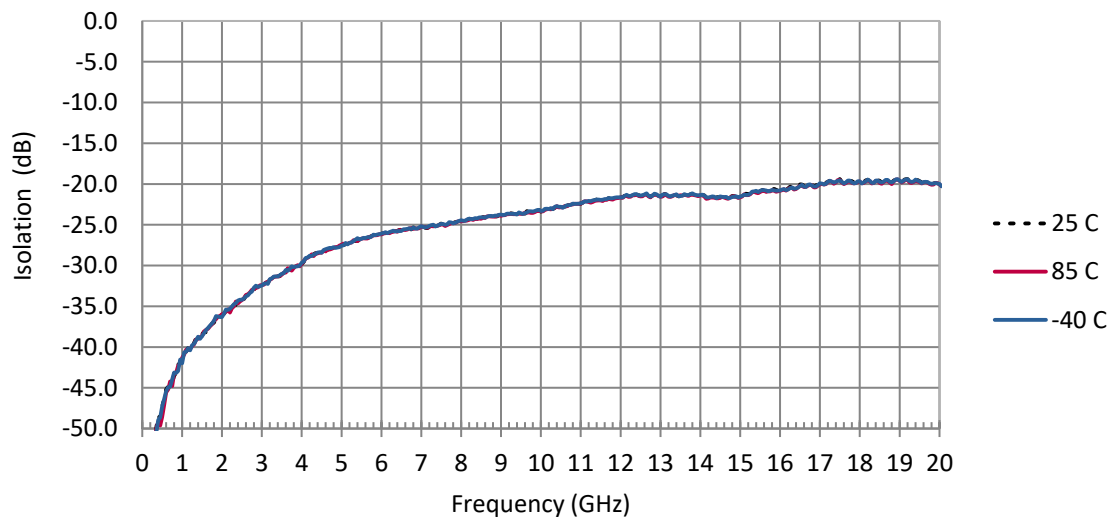
## Return Loss / S11 FOR 25 C, 85 C and -40 C

For channel RF2, data is de-embedded

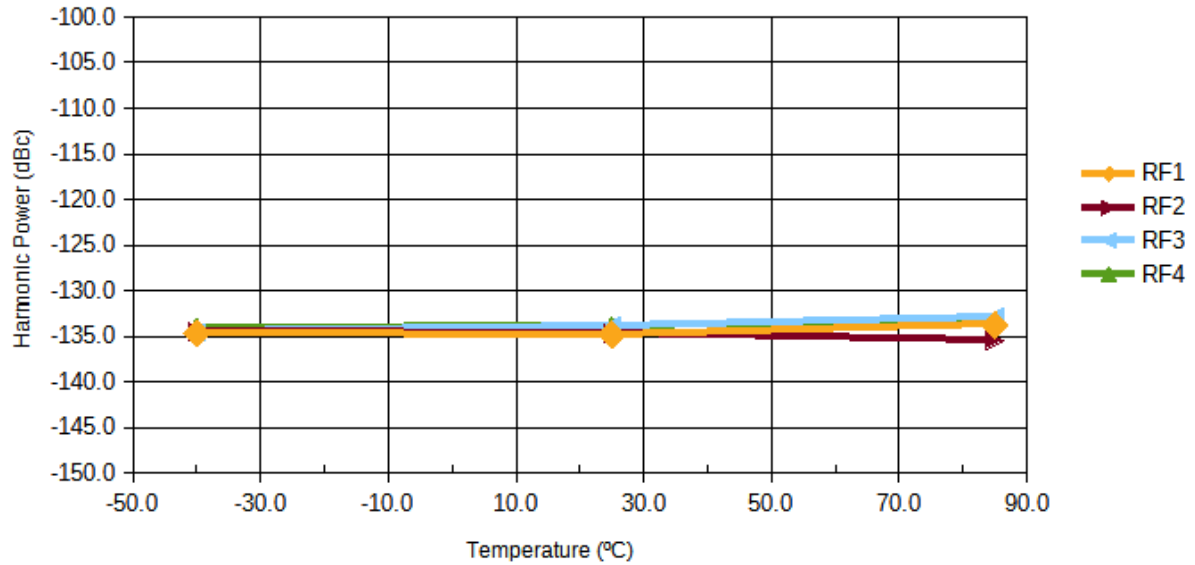


## Off-State Isolation / S21 for 25 C, 85 C and -40 C

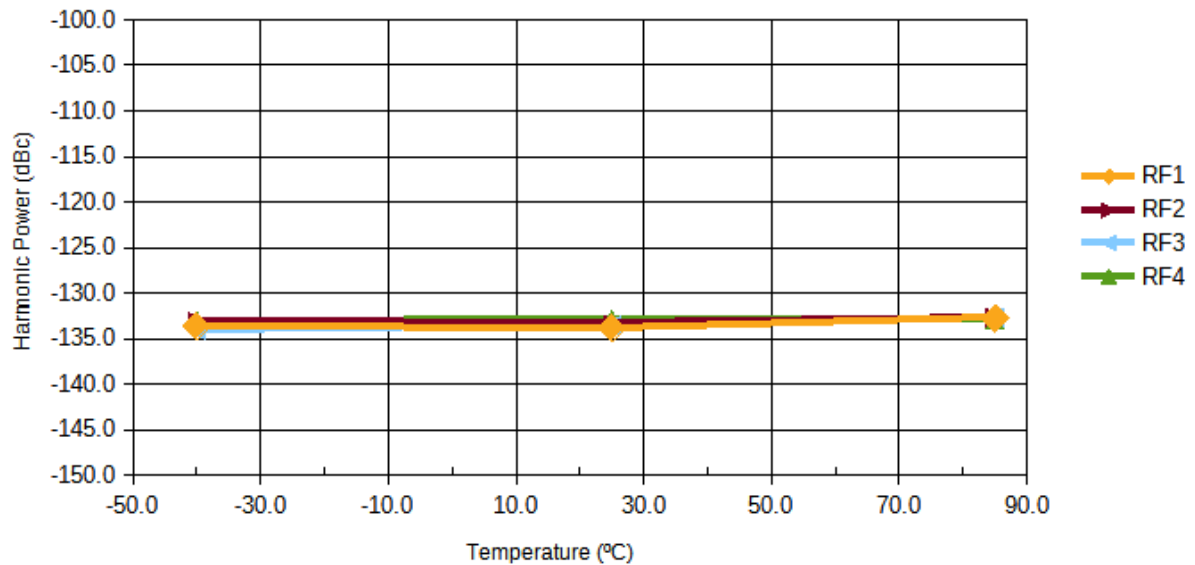
For channel RF2, data is de-embedded



## Second Harmonic Power vs. Temperature

 $f_0 = 1.0 \text{ GHz}, 36 \text{ dBm}$ 

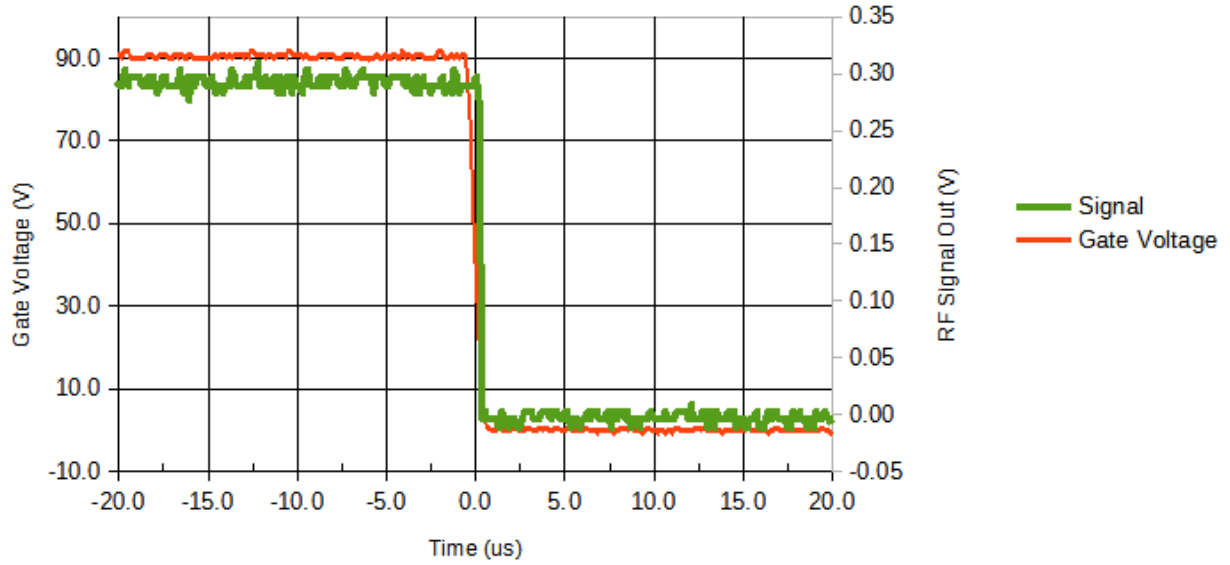
## Third Harmonic Power vs. Temperature

 $f = 1.0 \text{ GHz}, 36 \text{ dBm}$ 

## On / Off Switching Time

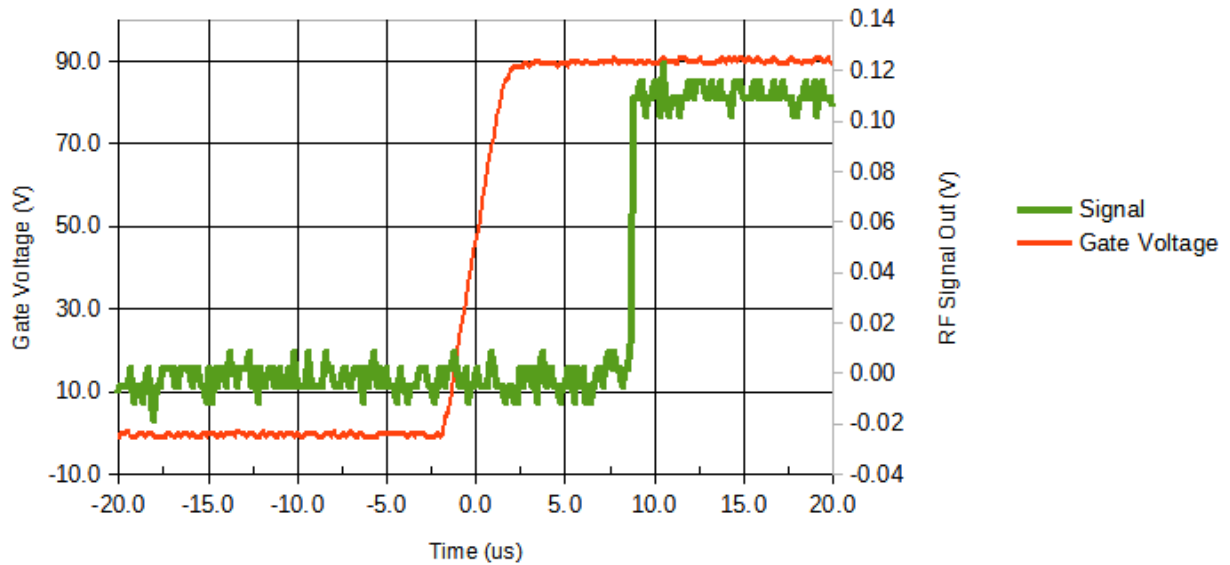
Switch Off Timing

f = 100 MHz



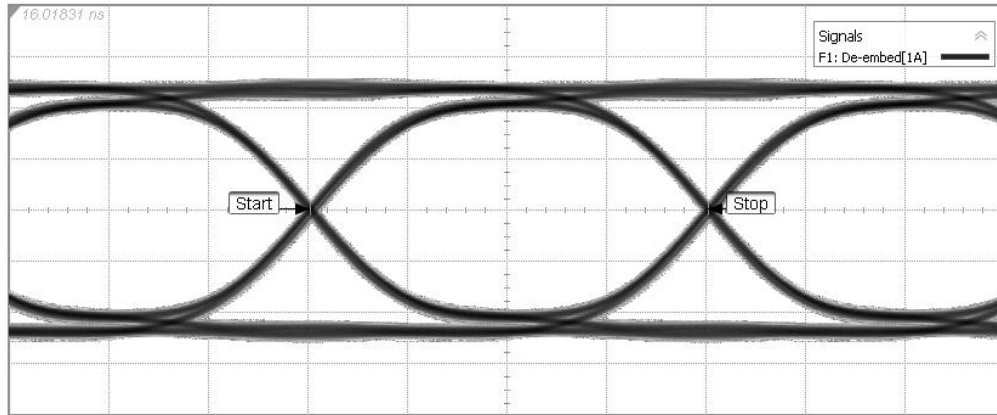
Switch On Timing

f = 100 MHz





### Single-Ended Eye Diagram Measurement

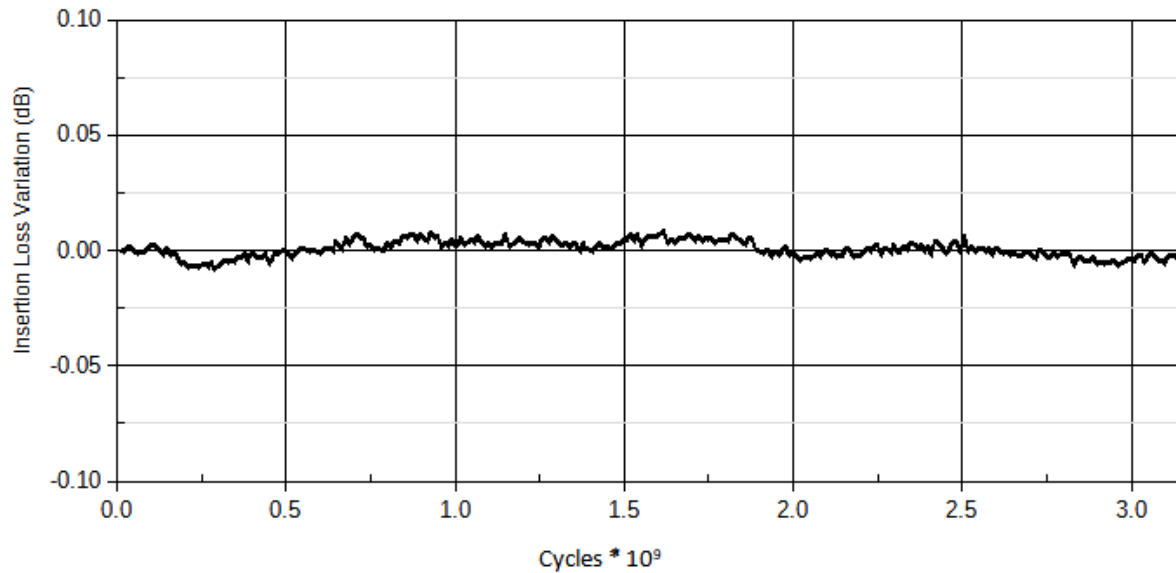


Test Cases	Bit rate	Eye Height	Eye Width	Jitter (Pk to Pk)	Rise Time	Fall Time
Baseline-Test System	20.000 Gbps	440.00 mV	48.16 ps	1.99 ps	14.99 ps	14.33 ps
MM5120 EVK	20.000 Gbps	339.80 mV	48.20 ps	2.16 ps	24.00 ps	24.34 ps

## Typical Hot-switching Performance

### Insertion Loss Variation over Cycling

Channel RF1 cycled with 10 dBm RF power, measured at 25 C



## Programming

### Communication Interface

The driver interface two modes of operation; **Serial** and **GPIO (Parallel)**, selected by the **MODE** input pin.

All the SPI pins (except SSB pin), the FLIP\_BIT and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float.

The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is VIN4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

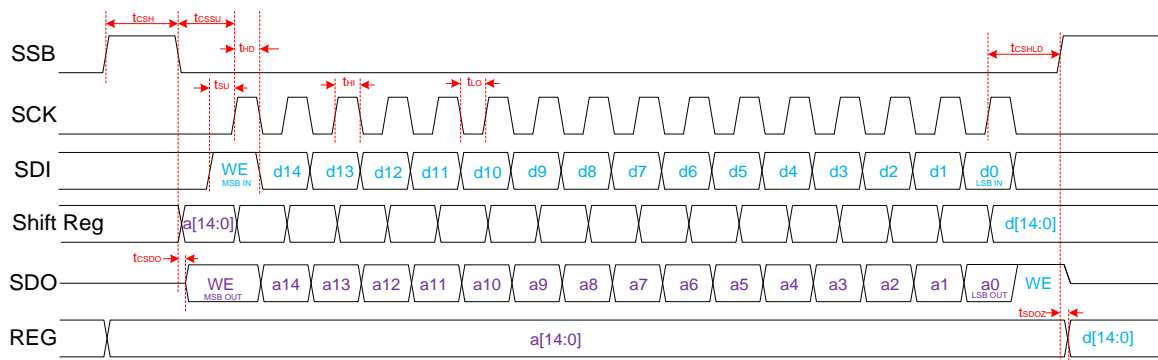


Figure 4: SPI Timing Diagram

### Serial Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. (See Daisy Chain Operation figures 7 to 9)

The SPI works at any frequency up to a maximum of 33 MHz, and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

### SPI Interface Mode

SPI timing diagrams are provided in Figures 4 to 9. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires

data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data ( $D_N$ ) to Target, while Target passes its previous ( $D_{N-1}$ ) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if  $WR\_EN = 1$ .

### SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

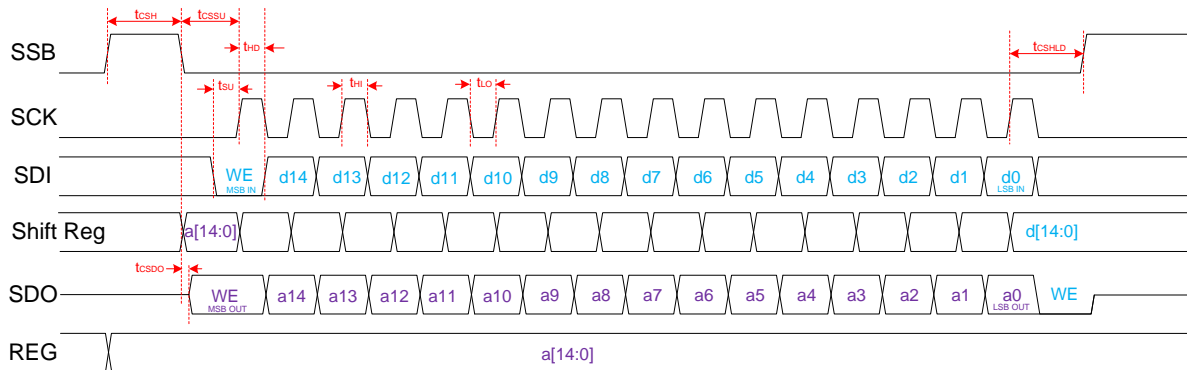


Figure 3: SPI Read Only (1 IC, No Daisy Chain)

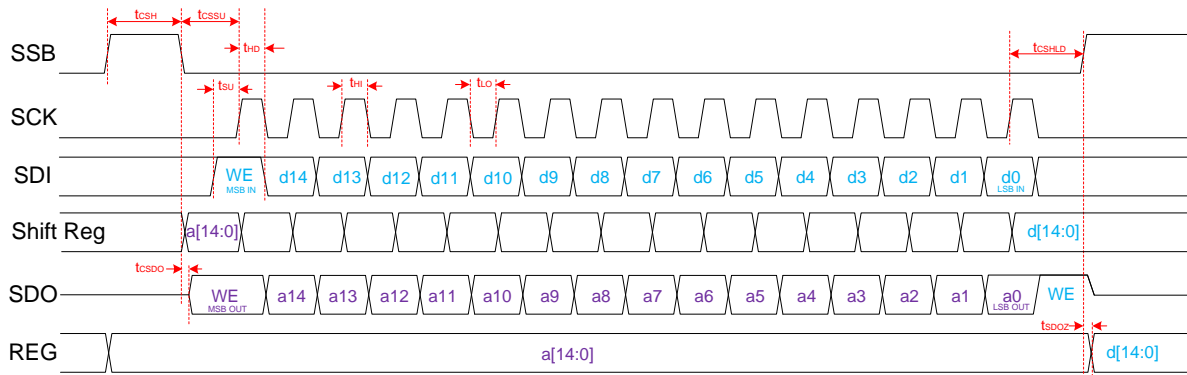


Figure 4: SPI Read & Write (1 IC, No Daisy Chain)



## SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the SDO pin while clocking the SCK pin.

Register STATE holds the state of the 4 switches and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high.

Register CONTROL holds four control bits (CPEN, VPPCOMP, FLT\_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high.

In SPI mode, the CP\_EN and FLT\_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

### STATE REGISTER

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
0	0	0	0	RF4	RF3	RF2	RF1
bit 7							bit 0

#### bit 7: **Low**

Set this bit low.

#### bit 6: **Low**

Set this bit low.

#### bit 5: **Low**

Set this bit low.

#### bit 4: **Low**

Set this bit low.

#### bit 3: **RF4**

1 = RFC to RF4 is Enabled

0 = RFC to RF4 is Disabled

#### bit 2: **RF3**

1 = RFC to RF3 is Enabled

0 = RFC to RF3 is Disabled

#### bit 1: **RF2**

1 = RFC to RF2 is Enabled

0 = RFC to RF2 is Disabled

#### bit 0: **RF1**

1 = RFC to RF1 is Enabled

0 = RFC to RF1 is Disabled

**CONTROL REGISTER**

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit7							bit 0

**bit 7: WR\_EN**

- 1 = Enable write mode
- 0 = Disable Write mode (read only)

**bit 6: FSTAT<sup>25</sup>**

- 1 = VPP OR VDD Fault status = faulted
- 0 = VPP OR VDD Fault status = NOT faulted

**bit 5: SLEEP<sup>26</sup>**

- 1 = SLEEP mode active (all analog circuits disabled)
- 0 = SLEEP mode inactive (all analog circuits enabled)

**bit 4: FLTMODE**

- 1 = Fault Mode Disabled (shutdown Disabled)
- 0 = Fault Mode Enabled (shutdown Enabled)

**bit 3: VPPCOMP**

- 1 = VPP under-voltage comparator is disabled
- 0 = VPP under-voltage comparator is active

**bit 2: Do Not Care**

This bit can be set to either state without effecting performance.

**bit 1: CPEN**

- 1 = Charge Pump is enabled
- 0 = Charge Pump is disabled

**bit 0: Do Not Care**

This bit can be set to either state without effecting performance.

<sup>25</sup> VPP and VDD faults are latched. Once this bit is set high, it must be written to 0 to clear the fault.

<sup>26</sup> The SLEEP bit is forced low in GPIO mode.



### Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the SDO of one chip to the SDIN of the next chip in the chain, as shown in Figure 5. SPI timing diagrams with daisy-chained devices are provided in Figure 6 and Figure 7.

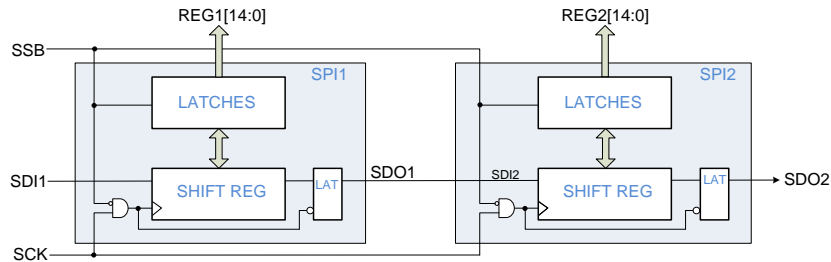


Figure 5: SPI with 2 ICs Daisy-chained

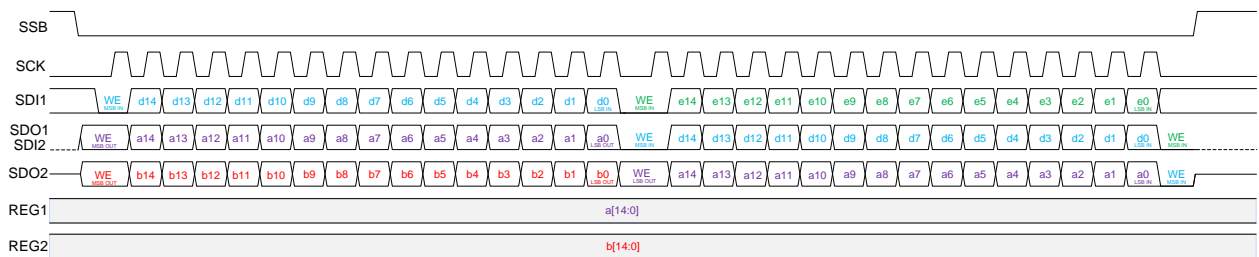


Figure 6: SPI Read Only (2 ICs Daisy-chained)

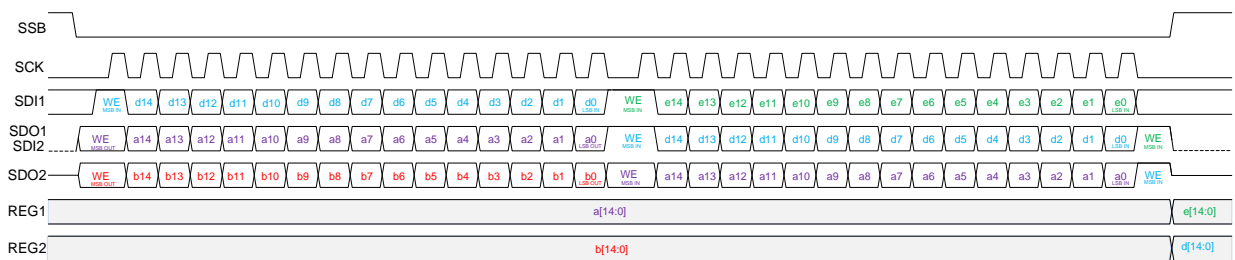


Figure 7: SPI Read & Write (2 ICs Daisy-chained)



### GPIO Communication

MODE = 1 activates the GPIO (General Purpose Input Output or Parallel Mode) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs, as described in the Detailed Pin Description Table 5.

**Table 6** Switch State Table in GPIO Mode

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
0	1	0	0	0	0	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	<b>ON</b>
2	1	0	0	1	0	OFF	OFF	<b>ON</b>	OFF
3	1	0	0	1	1	OFF	<b>ON</b>	OFF	OFF
4	1	0	1	0	0	<b>ON</b>	OFF	OFF	OFF
5	1	0	1	0	1	OFF	OFF	OFF	OFF
6	1	0	1	1	0	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	OFF	OFF	OFF
8	1	1	0	0	0	OFF	OFF	OFF	OFF
9	1	1	0	0	1	<b>ON</b>	OFF	OFF	<b>ON</b>
10	1	1	0	1	0	OFF	<b>ON</b>	<b>ON</b>	OFF
11	1	1	0	1	1	<b>ON</b>	OFF	<b>ON</b>	OFF
12	1	1	1	0	0	<b>ON</b>	OFF	<b>ON</b>	OFF
13	1	1	1	0	1	<b>ON</b>	OFF	<b>ON</b>	OFF
14	1	1	1	1	0	OFF	<b>ON</b>	OFF	<b>ON</b>
15	1	1	1	1	1	OFF	OFF	OFF	OFF



#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
16	0	0	0	0	0	OFF	OFF	OFF	OFF
17	0	0	0	0	1	OFF	OFF	OFF	ON
18	0	0	0	1	0	OFF	OFF	ON	OFF
19	0	0	0	1	1	OFF	OFF	ON	ON
20	0	0	1	0	0	OFF	ON	OFF	OFF
21	0	0	1	0	1	OFF	ON	OFF	ON
22	0	0	1	1	0	OFF	ON	ON	OFF
23	0	0	1	1	1	OFF	ON	ON	ON
24	0	1	0	0	0	ON	OFF	OFF	OFF
25	0	1	0	0	1	ON	OFF	OFF	ON
26	0	1	0	1	0	ON	OFF	ON	OFF
27	0	1	0	1	1	ON	OFF	ON	ON
28	0	1	1	0	0	ON	ON	OFF	OFF
29	0	1	1	0	1	ON	ON	OFF	ON
30	0	1	1	1	0	ON	ON	ON	OFF
31	0	1	1	1	1	ON	ON	ON	ON

## Fault Conditions

There are two comparators<sup>27</sup> that can signal a fault condition - VDD under voltage fault and VPP under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO.

The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than  $UVLO_{RISE}$  and VPP goes higher than  $V_{EN}$ ). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below  $UVLO_{FALL}$  or VPP goes below  $VPP_{DIS}$ , a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared – the FSTAT bit remains latched high until it is cleared via a SPI write.

If Fault Mode is enabled (in GPIO mode, FLT\_MODE pin = 0, in SPI mode, FLT\_MODE bit = 0), the outputs are all set low and the charge pump is turned off. The user must toggle the CP\_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to re-start the device.

If Fault Mode is disabled (in GPIO mode, FLT\_MODE pin = 1; in SPI mode, FLT\_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

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<sup>27</sup> The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP\_EN pin is set low.

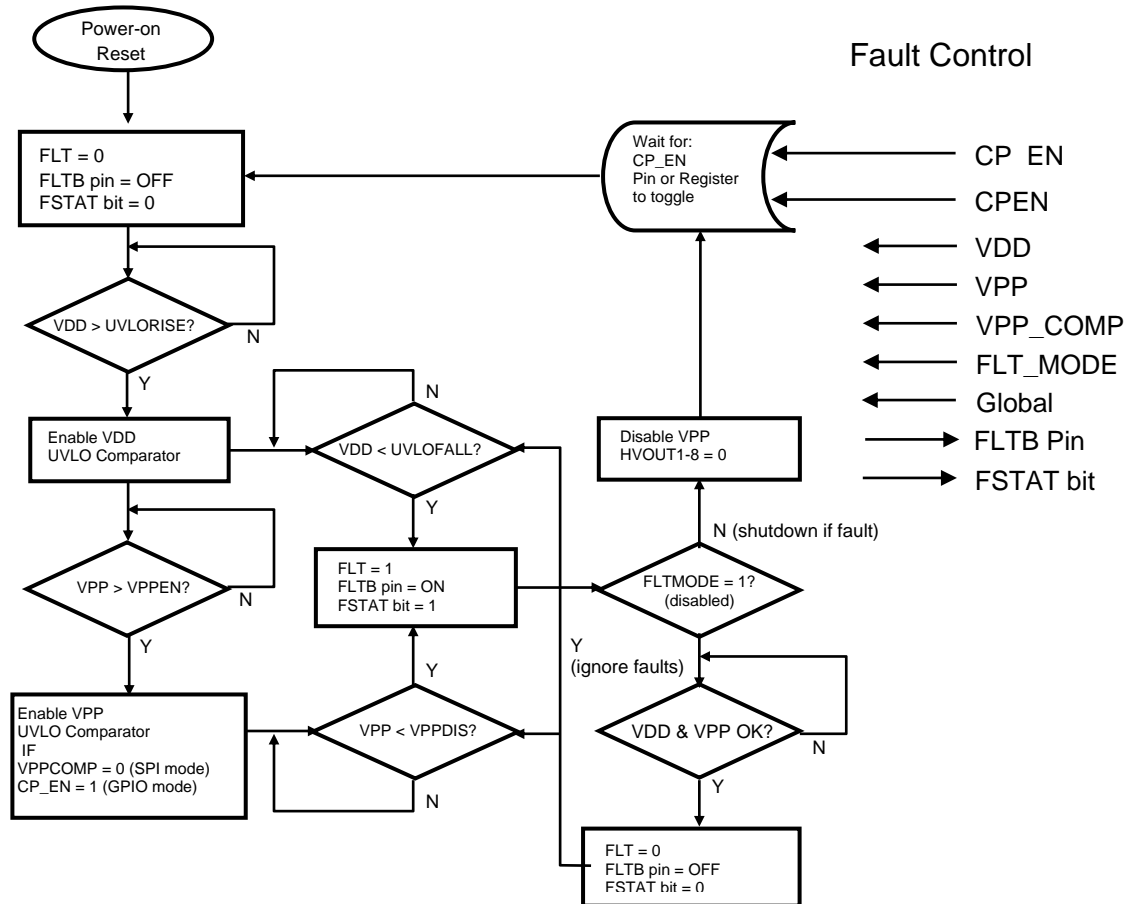


Figure 3: Flowchart for Fault

Notes:

- 1) The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
- 2) VDD\_IO is not monitored unless it is connected to VDD.
- 3) VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP\_EN pin is low In GPIO mode.

## External Circuitry

The MM5120's internal driver requires external circuitry to operate its charge pump. The diagram below shows the suggested bypass capacitors that have been used with good results. Menlo Micro recommends selecting components with equal or better performance.

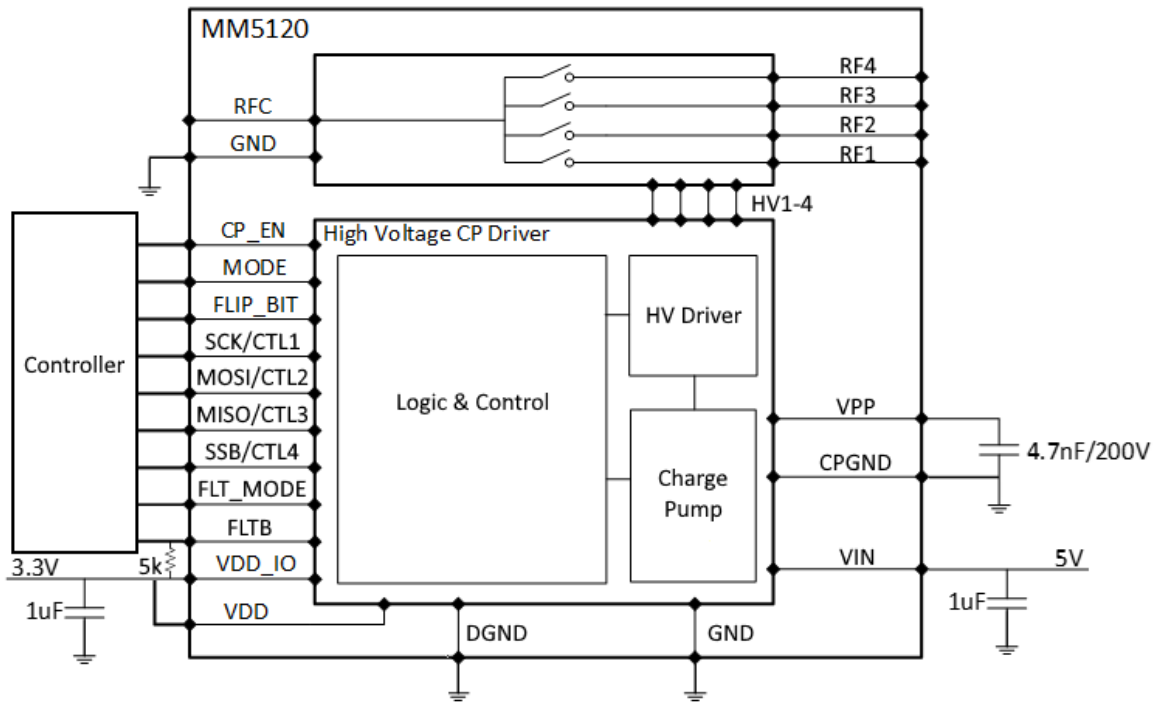


Figure 8: MM5120 Application Diagram

## Package Drawing

### 62 Pin LGA Package

Dimensions are given in millimeters.

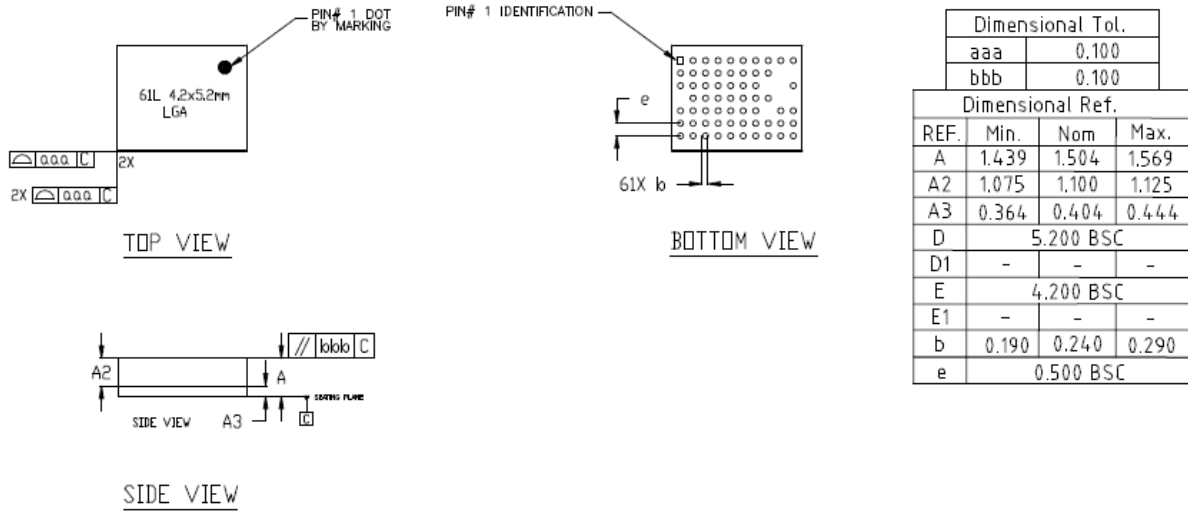


Figure 9: Package Drawing



## Recommended PCB layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram below.
- Open space around the package can have grounded thru holes.
- Use ENIG pad surface finish.
- Use 20 micron thick solder mask.
- Use Type 3 or higher solder paste with no clean flux.
- Component placement force should not exceed 100 grams.

Layout recommendation for connecting the MM5120 with coplanar RF line or grounded coplanar line as used for the MM5120 evaluation board.

For the coplanar RF lines, it is recommended to taper the line to fit the 150 um recommended landing pad while keeping the spacing to the ground metal constant and identical to the spacing used for the line.

## Recommended Solder Reflow Profile

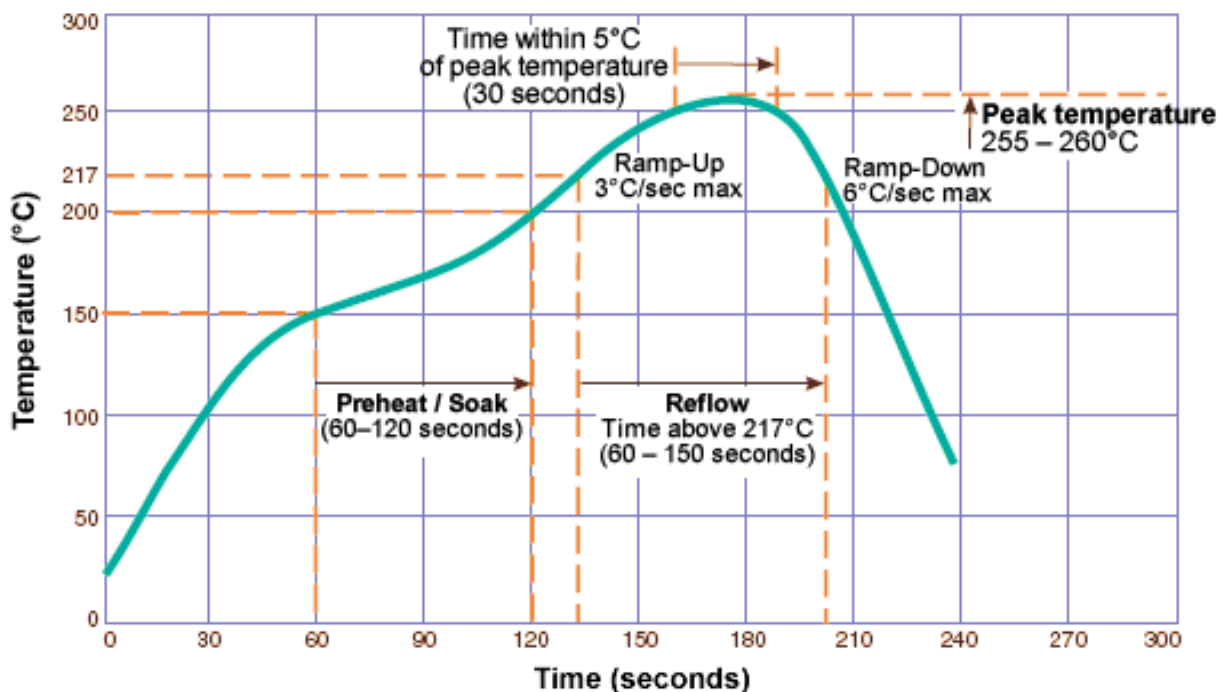


Figure 10: Recommended Reflow Profile

A ROHS compliant Solder Alloy used is SAC alloy: 96.5% Sn, 3.0%Ag, 0.5%Cu. These are the nominal percentages of the components. This alloy is designed to replace SnPb solders to eliminate Lead (Pb) from the process, requiring a higher reflow temperature.



Moisture resistance performance may be impacted if not using the Pb-Free reflow conditions.

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

## Tape & Reel Details

Tape and reel details will be included in a future revision.

## Package Options and Ordering Information

Part Number	ECCN	Package	Temperature Range
<b>MM5120</b>	EAR99	5.2 mm x 4.2 mm 62 pin LGA	-40°C to +85°C
<b>MM5120EVK</b>	EAR99	Evaluation Board MM5120 <12 GHz	

## Important Information

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