menlomicro

WL-FC device

Assembly Instructions
December 2023

The push to make electronic components smaller and smaller has resulted in many Wafer Level Packaged devices as this can save much needed space within assemblies and also results in performance advantages due to removal of interconnects. For example, our MM5130 is a 2.5 x 2.5 x 0.9 mm wafer level device.

As the bump interconnects are not set in a regular array, we have termed it Wafer Level Flip Chip (WL-FC) to differentiate it from other WL-CSP devices.

The interconnects are formed using 0.100 mm diameter copper pillars with nominally 0.100 mm diameter tin caps, see figure 1.

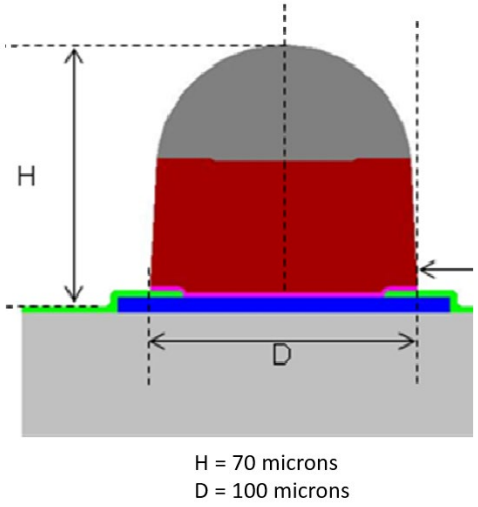

Figure 1: Copper pillar details

The top surface of the chip is covered with a black acrylic coating and marked as indicated in the data sheet. Figure 2 shows typical part marking including machine readable 2D bar code and human readable part number. Care should be taken during clean operations as some solvents may attack the acrylic coating. Heated DI water has been used successfully, in addition Ultrasonic cleaning is not recommended and may cause part damage/reliability issues.

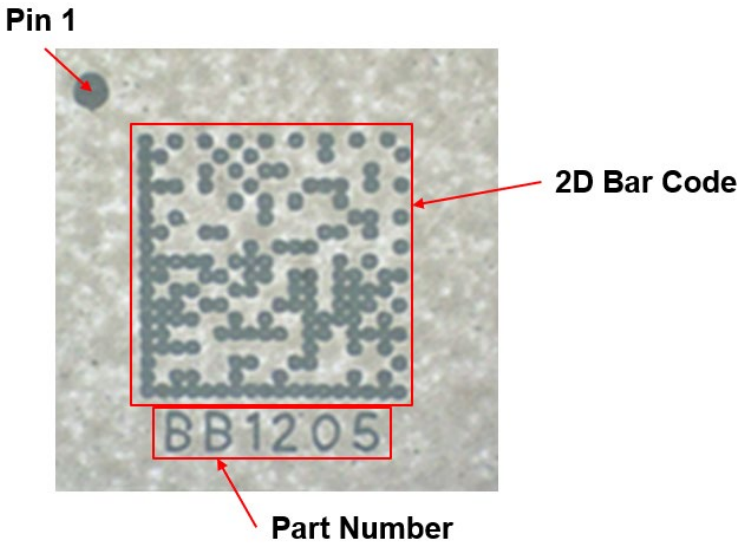

Figure 2: Typical marking with Pin 1 identifier, 2D barcode and Part Number

The devices are provided on tape and reel as defined below in Figure 3.

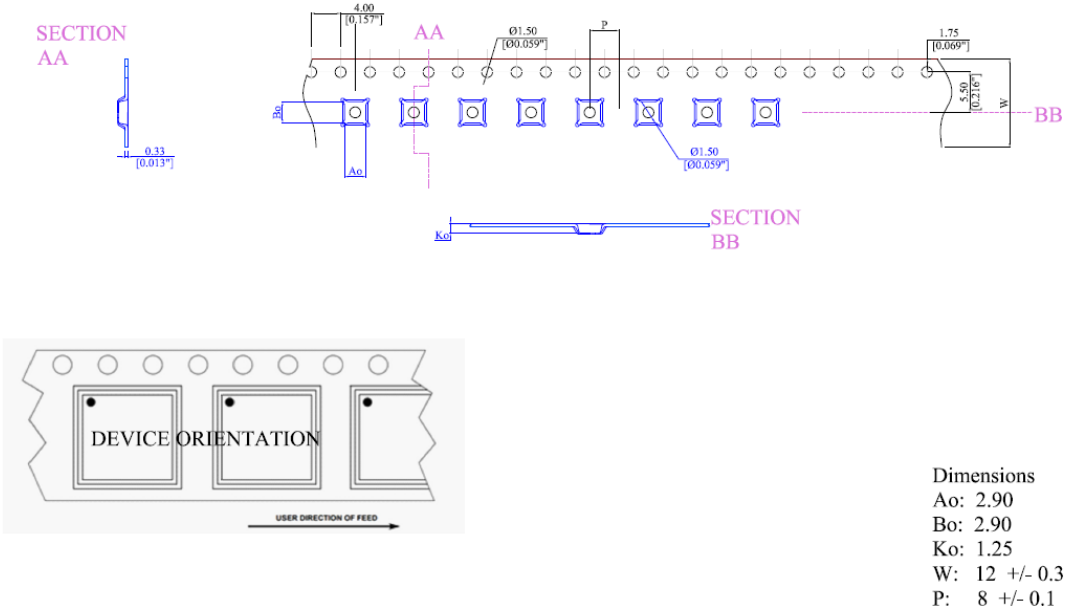

Figure 3: Tape and Reel definition, MM5130 EVK (dimensions in mm)

PCB Board design considerations

For best results an RF substrate should be chosen based on the operating frequency/operating parameters and cost consideration for the design.

Minimum pad diameter is 0.150 mm.

Due to the size of the device and pin layouts a 50 ohm impedance line may not be possible at the device pins based on linewidth and spacing limitations during board fabrication.

While no particular surface finish is required, Menlo has used both ENIG and EPIG/EPAG successfully.

Use typical 0.020 mm thick solder mask over circuit traces.

Use a non-conductive silkscreen border outline around the part location to aid in part placement during assembly and any possible rework, ensure silkscreen does not extend underneath part placement area. See MM5130 EVK design files for reference.

Solder Screen Recommendations:

1. Each connected bump on the device needs to be soldered to the PCB substrate, the solder stencil should be between 0.037 to 0.075 mm (1.5 to 3 mil) thick laser cut steel.
2. No nano-coating is required on the stencil.
3. The optimum aperture for each bump is octagonal and is detailed in Figure 4., dimensions are in mm (inches). This was developed through numerous solder trials and yields the best solder joint.
4. Lead-Free No-clean Type 4 or Type 5 solder paste, Indium 10.8HF SAC305 was used in our trials.

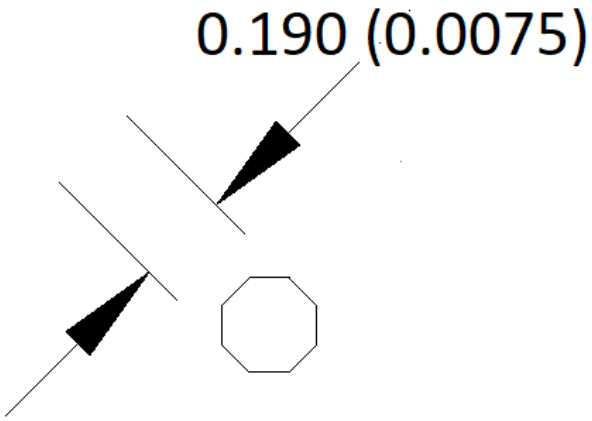

Figure 4: Aperture Details

Pick and Place Procedure:

1. Treat the device as electrostatic sensitive and observe all customary handling precautions including working on static dissipative surfaces, wearing wrist/shoe straps, ESD smocks/jackets or other ESD control devices. Store unused devices in their packaging in ESD bags. Do not store loose parts in bulk bins, do not use parts that have been stored on workbench tops or that have been dropped.
2. To ensure centering of the part during pick and place use look up vision centering.
3. Vacuum pick shall be used.
4. Component placement force should not exceed 100 g.

Solder Profile

Figure 5 details the recommended solder profile for lead free solder. Prior to board assembly it is recommended to run solder profile with thermocouples at the part location to ensure reflow temperature/duration are reached. This is especially important with large dense boards that contain many parts.

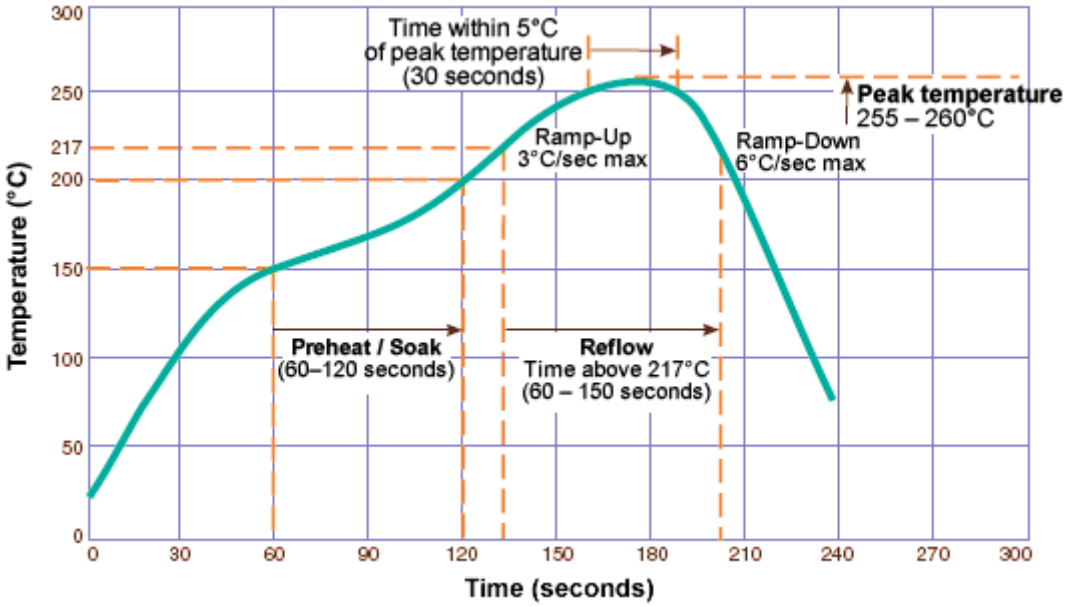

Figure 5: Solder reflow profile

A ROHS compliant Solder Alloy used is SAC alloy: 96.5% Sn, 3.0%Ag, 0.5%Cu. These are the nominal percentages of the components. This alloy is designed to replace SnPb solders to eliminate Lead (Pb) from the process, requiring a higher reflow temperature. Moisture resistance performance may be impacted if not using the Pb-Free reflow conditions.

Figure 6 details the recommended solder profile for leaded SnPb solders. Prior to board assembly it is recommended to run solder profile with thermocouples at the part location to ensure reflow temperature/duration are reached. This is especially important with large dense boards that contain many parts.

This profile allows an extended time at high temperature to allow the SnPb solder to mix with the Sn solder balls on the package and produce a reliable solder joint.

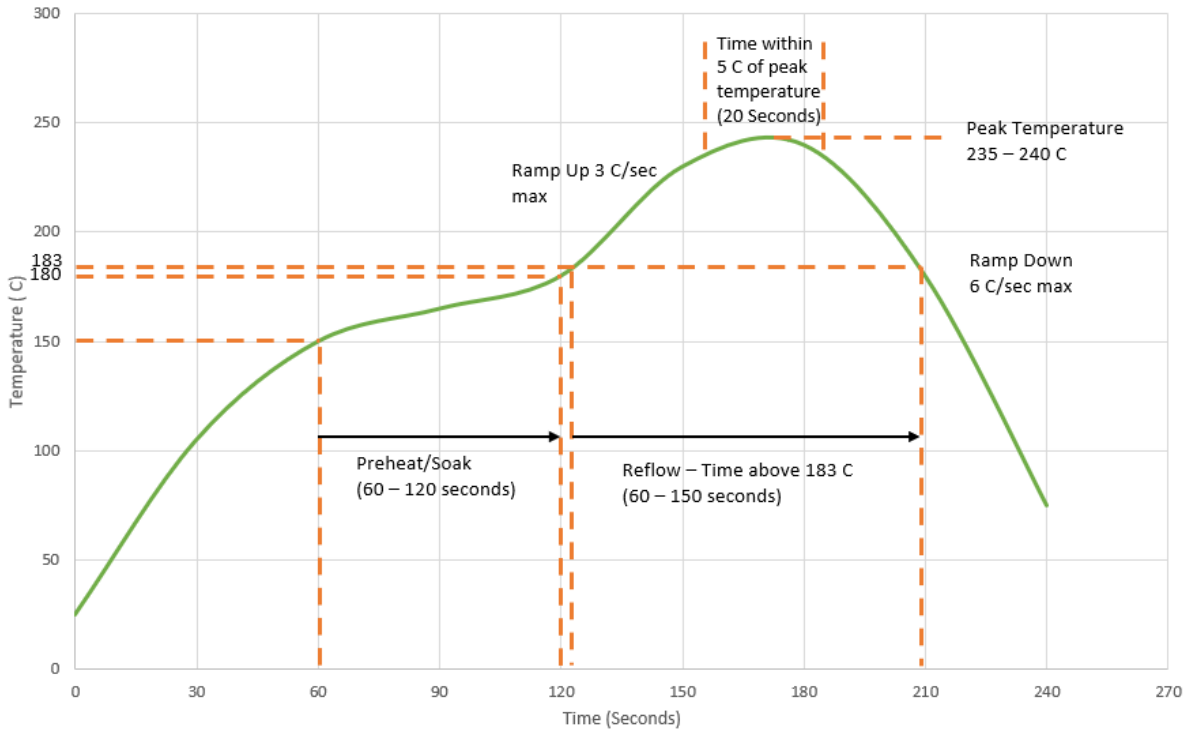

Figure 6: Solder reflow profile

Underfill Application

Although not typically required an underfill compound may be used. Care must be taken when choosing the underfill material to ensure good viscosity so that full coverage is acquired around the device pins. Some underfill materials have significant impact on RF performance and this should be verified prior to use. One material we have used which shows good viscosity, very low impact on performance and has a relatively well matched CTE is Namics Chipcoat U8439-1.

As this device is comprised of two glass wafers compression bonded together it is important when applying the underfill that any fillet and residue around the device remain below the joint between the two halves (300 um from base). Figure 7 illustrates this critical constraint.

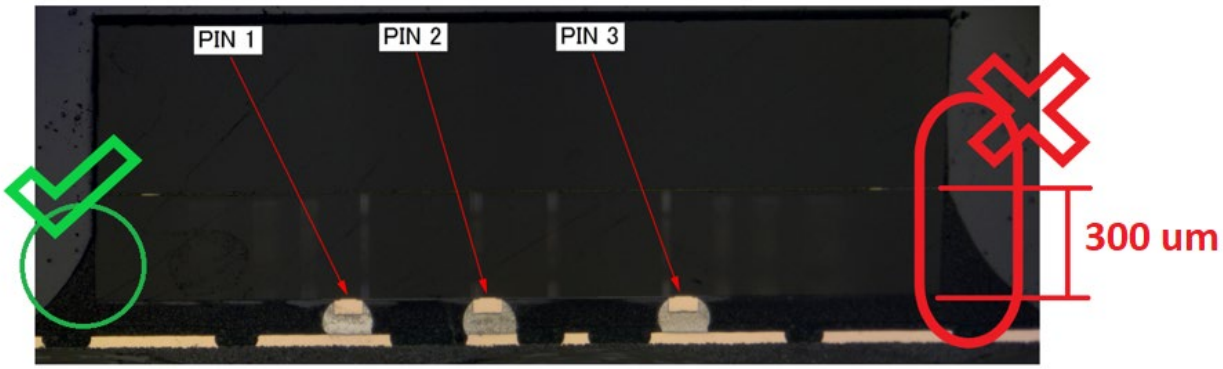

Figure 7: Underfill Application