menlomicro

The Ideal Switch®

Enabling the electrification of everything:

Milliwatts-to-kilowatts, DC-to-light.

High-Speed Digital Products

September 2025

TOC

Menlo Micro Company Overview

The Ideal Switch® is the most revolutionary electronics component invention since the transistor

- **Company:**
  - Founded in Dec, 2016
  - Irvine, CA (Headquarters);
  - Albany, NY (SUNY) (Advanced R&D)
  - Employees – 70+ in the US
- **Capitalization:**
  - $228M raised through series C
  - Closed series C $151M Feb 2022

Our investors

standard investments · PALADIN · FUTURESHAPE · VERTICAL VENTURE PARTNERS · PIVA · DBL PARTNERS DOUBLE BOTTOM LINE VENTURE CAPITAL · Fidelity INVESTMENTS · Adage

- **The Ideal Switch® Technology:**
  - World's smallest, most reliable, most efficient micro-electro-mechanical switch (MEMS) for RF and Power
  - Developed over 12+ years at GE Research and 7+ years of commercialization by Menlo Micro
  - Ideal Switch 8" wafer manufacturing line in production since Q4 2020
- **Intellectual Property:**
  - Fundamental material science-based IP licensed exclusively from GE, 65 patent families
- **Markets:**
  - Semiconductor Test, Test & Measurement
  - Aerospace and Defense
  - Wireless Infrastructure
  - Energy Distribution

What's new at Menlo Micro:

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- Four years of production on Ideal Switch® 8" manufacturing line. Over 820k units shipped through 2024
- 2023 to 2024 YOY $ growth: **3x increase**, 2024 to 2025 forecast YOY $ growth: **2x increase**
- "Ideal Fab" buildout has commenced, in process

ideal switch® Gaining Traction!

(8) products now released to production!

- MM5130 (Nov-2020), MM5600 (Nov-2021)
- MM5120, MM5140 (Aug-2022), MM101 (Dec-2022)
- MM5620 (April-2023), MM5622 (Sep-2024), MM5230 (Mar-2025)

Next products to be introduced in 2025:

- RF Products: MM5625, MM5815, MM5130-EDC
- Power Products: MM9200 (300V/10A)

Key Initiatives for 2025:

- Launch next long-term product developments for 2026/2027 growth, MM56xx and MM12xx

Ideal Fab™

menlomicro ideal fab™

- Announced on 11th July 2023
- Target online CY2027
- Up to 2k WPM capacity

- Focus of the new Ideal Fab:
  - Onshore the Ideal Switch® technology to protect and control critical IP access
  - Manage and control the Menlo Microsystems supply chain
  - Cost, yield, lead-time improvements

It all started with the Wizard of Menlo Park…

1870 to 1890
Menlo Park, NJ
Thomas Edison generates >200 inventions/patents around switches, relays & circuit-breakers

Today, switches are everywhere.

It’s the most ubiquitous electronic component.

In our homes.

- Managing our heat, AC, & lights.
- Our appliances are loaded with them.
- Circuit breakers that keep it all safe.

At work.

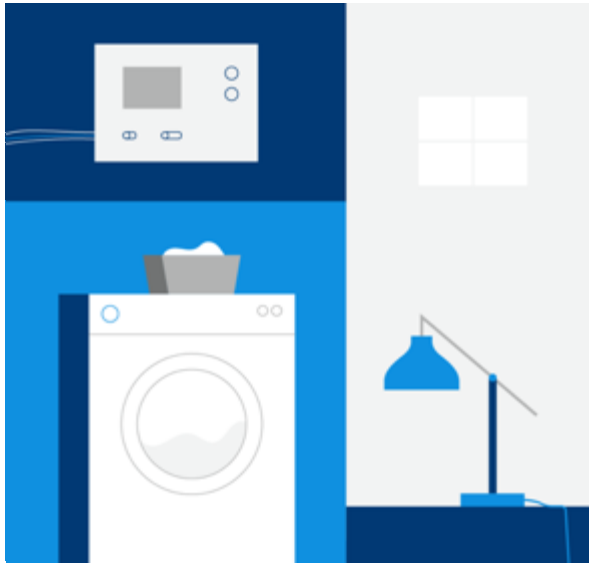
- Control the elevators, lighting, HVAC.
- All our computers, servers, comms.
- Manage factories and all equipment inside them.

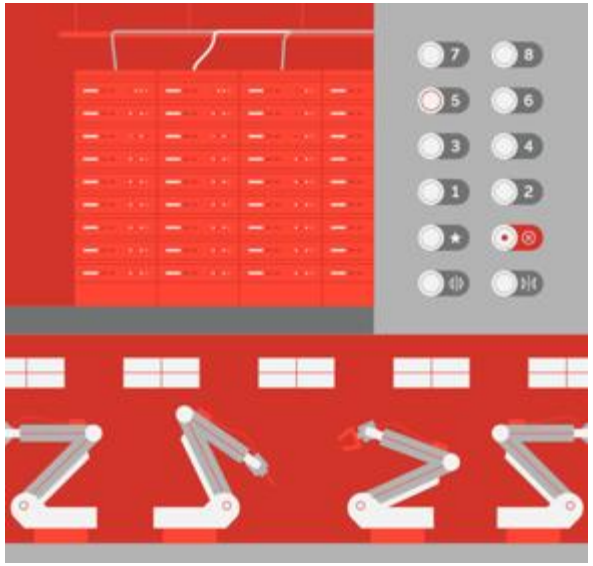
In our cars.

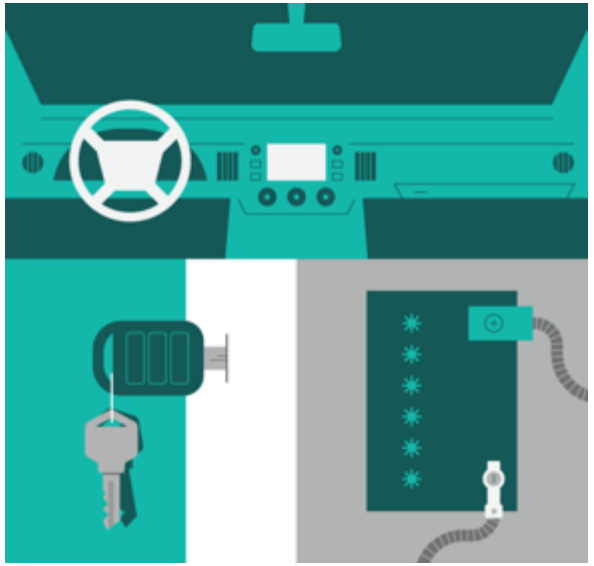
- Unlock the doors and start the engine.
- Turn on and tune the radio.
- Control the wipers, windows.
- Manage the battery.

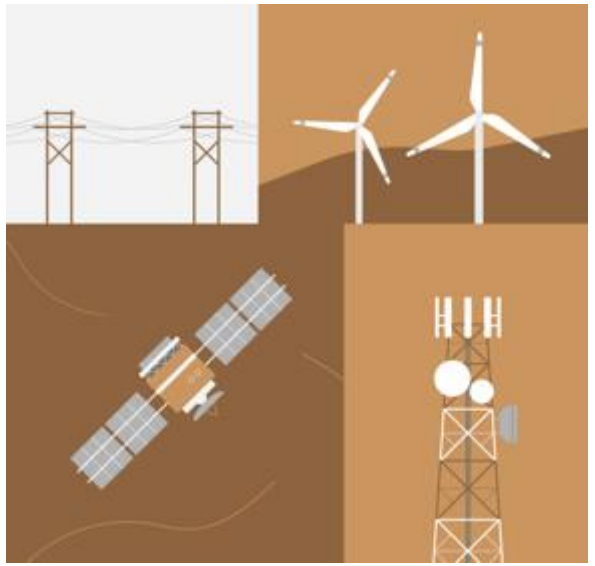
The world at large.

- Switches control the electricity flowing from power plants to the grid to our homes.
- Switches control the data zipping around the world to our computers and smartphones.







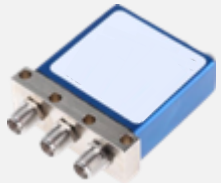


Two types of switches power today's world.

But they're full of compromises.

ELECTROMECHANICAL

RF



High Power RF Coax
High Isolation
Low Insertion Loss

RF Surface Mount
High Isolation
Low Insertion Loss

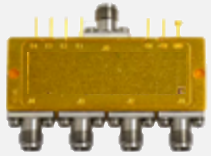
POWER

AC/DC Power Relay

Surface Mount Signal Relay

SOLID STATE

RF



PIN diode
High Power
Fast Switching
Long Life

CMOS
Low Power
Fast Switching
Long Life

POWER

AC/DC SSR w/heatsink
High Voltage
High Current

DC SSR w/heatsink
High Current

The Good: Can handle lots of power

- Metal contacts: low loss and great linearity for RF signals.
- Can handle high power, eg circuit breakers or RF relays.
- "On" - doesn't generate heat under high currents.
- "Off" - air-gap open, fully isolated.

The Bad: Big, slow, clunky and expensive

- Moving parts limit switch rate, speed and reliability.
- Manufacturing inconsistencies (some are still assembled by hand).
- Sensitive to mechanical shock, vibration and humidity.

The Good: Small, fast

- Small size allows for lightweight, tighter packing.
- Inexpensive to manufacture at scale.
- Fast, silent switching.
- Immune to mechanical shock, vibration, humidity.

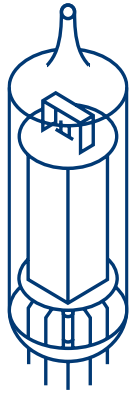
The Bad: It's a semiconductor, not a conductor

- "On" - non-zero losses, generates heat requiring large heatsinks.
- "Off" - always on, leakage currents, waste power.
- Non-linear effects of transistor distorts RF signal integrity.

But we're still using technology from the 1830s.

And the last major step-change is from the 1970s.

1835
Electromechanical Relay

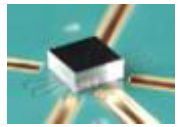


1904
Vacuum Tube

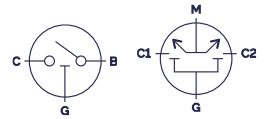
1947
Transistor

1960s–70s
Solid-State "Chip"

An entirely new "tool" for system designers to deploy.



2016
ideal switch®



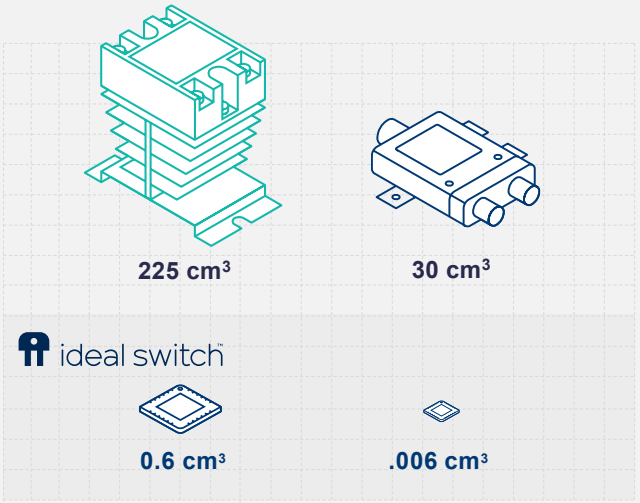
The perfect switch has been industry's Holy Grail

The perfect switch: In theory	VS	ideal switch®
When "ON" it's a wire with zero resistance		Below 0.005Ω (5 Milli-Ohms)
When "OFF" it's an open circuit, infinite resistance		Greater than 10,000,000,000Ω (10 Giga-Ohms)
It takes no power to turn it on and keep it on		Less than 0.000000000025 (25 Pico-amps)
It's small, fast, silent, and lasts forever.		Small, fast, silent, and can switch 3B+ actuations.
Costs $0 to make.		Built with low-cost, scalable ***semiconductor*** process . . . but is a true metal-on-metal ***conductor***.

Menlo’s “Rule of 99”

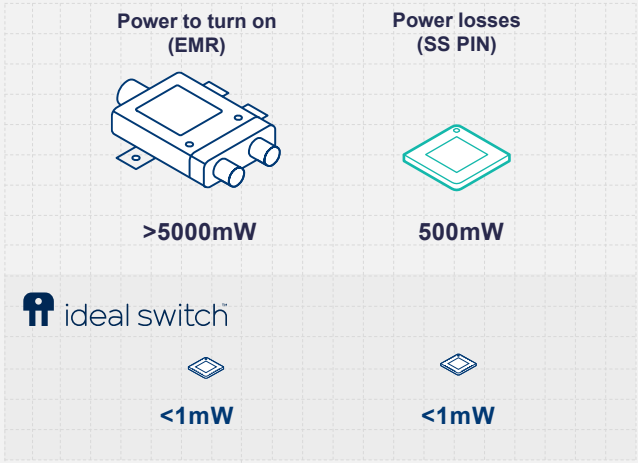
The Ideal Switch delivers game-changing improvements to Size, Weight, Power and Cost (SWAP-C)

Size & Weight



>99% Reduction

Power Consumption



>99% Reduction

Total Cost of Ownership

Other major spec improvements enable even more cost savings for system designers.

ideal switch

Switching Speed	Lifetime	Linearity
999x Faster	**999x Longer Lasting**	**999x More Linear**

The Ideal Switch story.

It starts, as most things do, with Thomas Edison.

1879

Edison patents the circuit breaker.

1892

General Electric formed, combining Edison's various companies.

Over 100 years of experience in high voltage, high reliability industrial controls.

2004

GE starts effort to reinvent the circuit breaker with a Micro-mechanical switch.

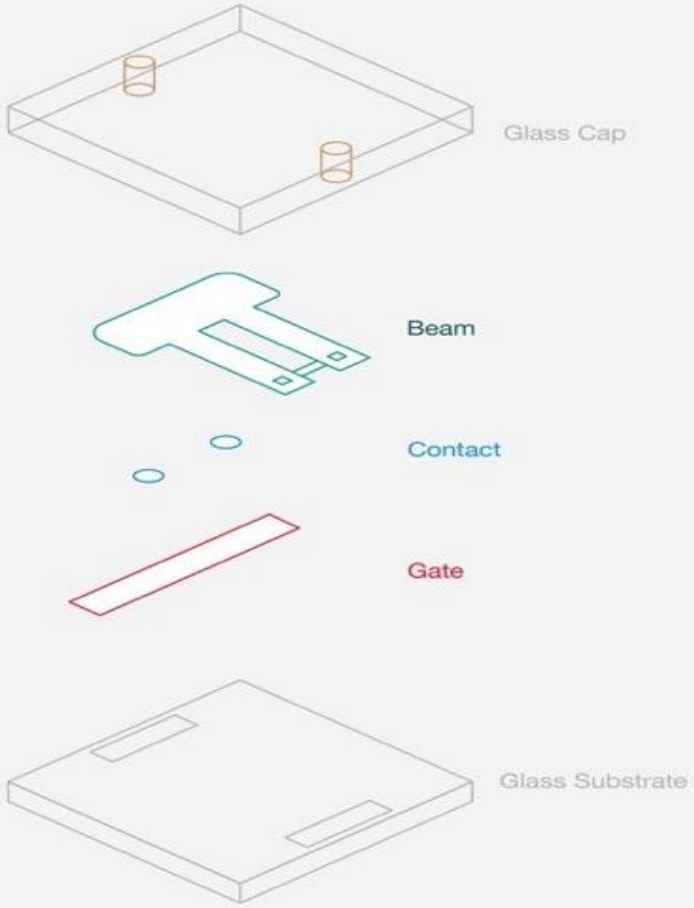
GE develops core IP, including high temperature, high reliability metal alloy science.

2016

Menlo Micro is formed

Introducing the Ideal Switch™

Technology platform with breakthrough innovations in materials and processing



Unique Glass Packaging

Improved RF & thermal performances
High RF power handling

Through-Glass-Via

Low parasitics and resistance
Small-size package

High Reliability

>3B switching cycles
Hermetic-sealed package

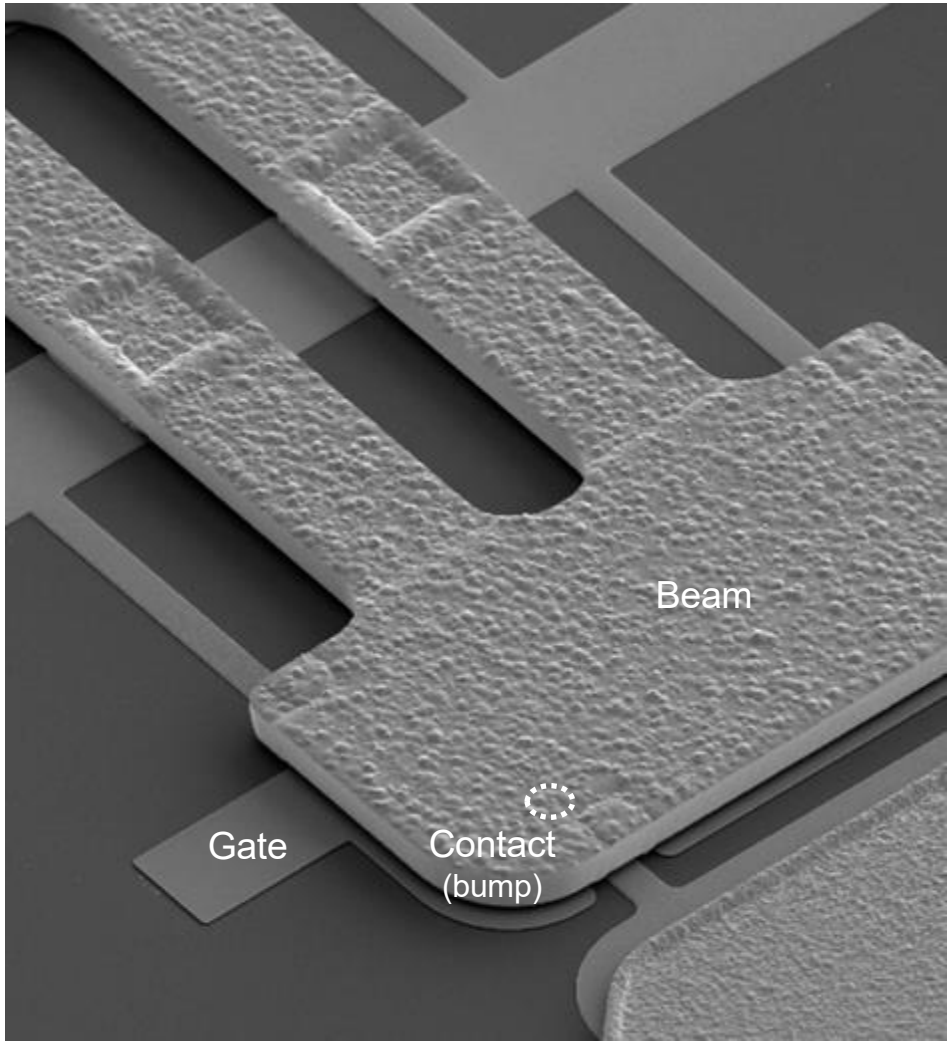
Scalability

100µm x 100µm (unit cell)

Scalable switch arrays for high voltage, high current, high power

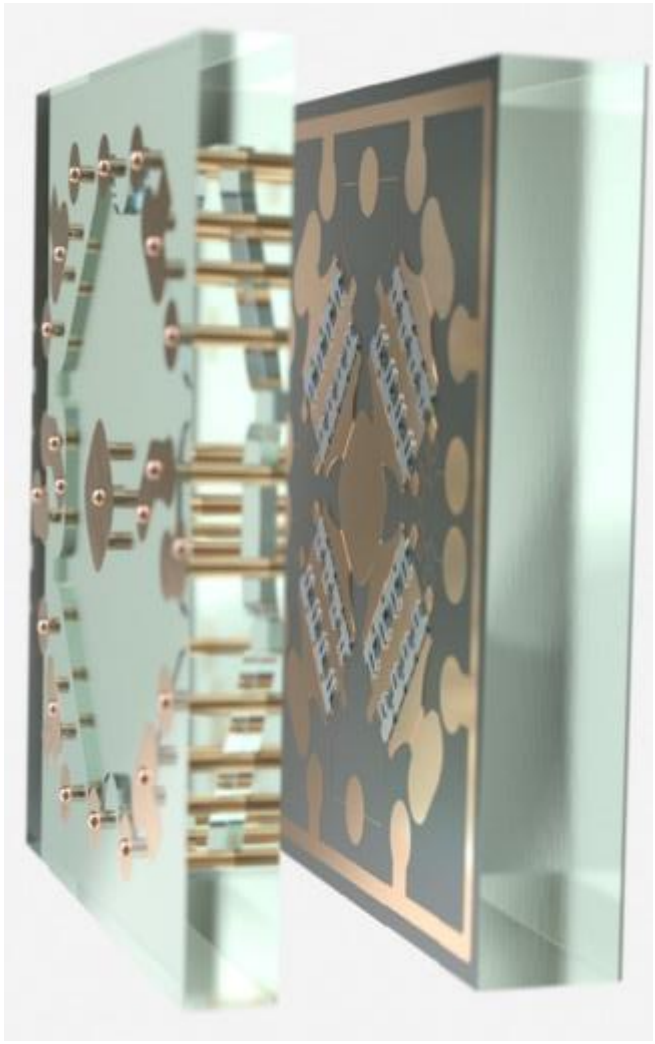
The Beam

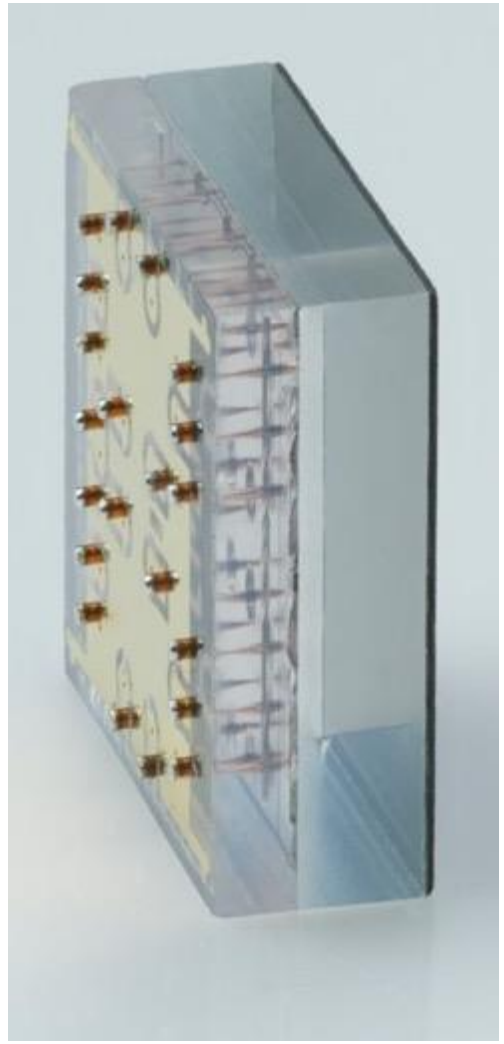
Smaller than a human hair, can handle >400 V



System-In-Glass Packaging

Close-up view of Through-Glass-Vias and hermetically sealed package





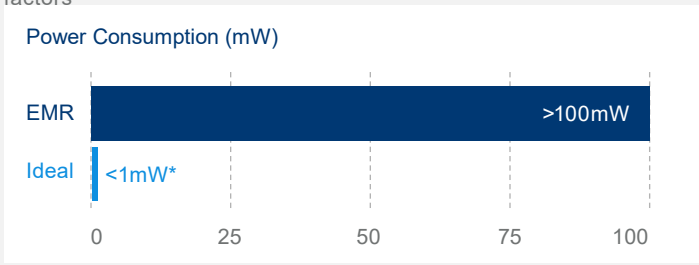
Ideal Switch vs. Electromechanical Relay.

These improvements aren't incremental. They're paradigm shifts.

PERFORMANCE

100X LESS POWER

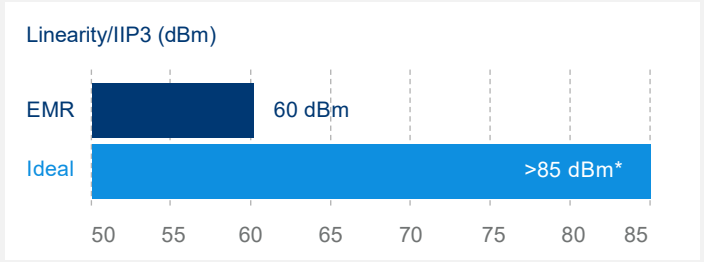
Longer battery life, less heat, new form factors



*Power needed to actuate a single switch

100X HIGHER LINEARITY

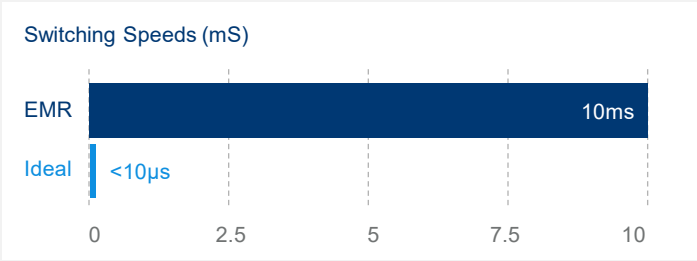
Distortion-free RF signal



*Menlo RF switch compared to typical RF coax switch performance.

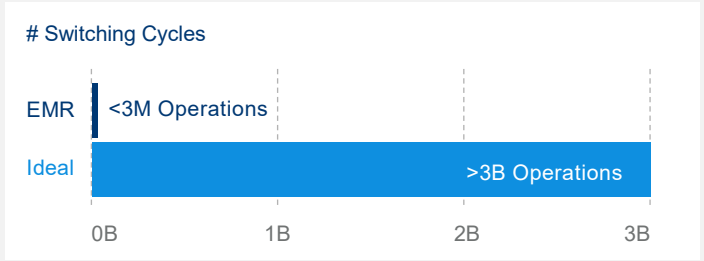
SWITCHES 1000X FASTER

New capabilities, New applications



1000X LONGER LIFE

Massive reliability gain



SIZE

Conventional EMRs

71 cm³

24 cm³

1 cm³

ideal switch™

0.6 cm³

240V/20A relay with integrated protection

0.4 cm³

48V/10A relay with integrated protection

.08 cm³

200V/2A signal relay

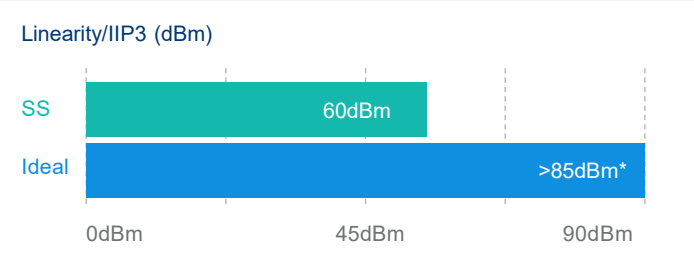
Ideal Switch vs. **Solid State.**

If nano-second switching speed isn't required, Menlo's Ideal Switch is always the better option.

PERFORMANCE

100X MAGNITUDE BETTER LINEARITY

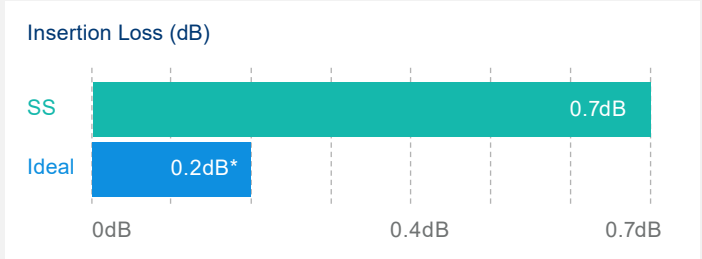
More bandwidth, higher data-rates



*Menlo RF switch compared to typical GaN & PIN

>0.5DB LOWER LOSS

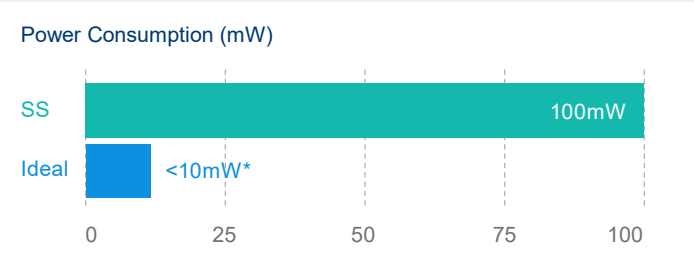
Longer battery life, no big, heavy heatsinks



*Menlo RF switch compared to typical GaN & PIN diode switch performance.

10X LESS POWER

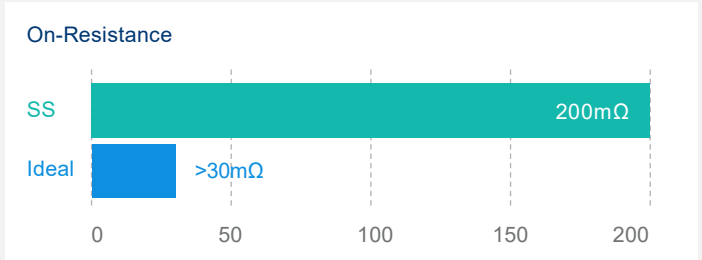
Longer battery life, less heat, new form factors



*Power needed to actuate a single "smart" switch

85% LESS RESISTANCE = NO HEATSINKS

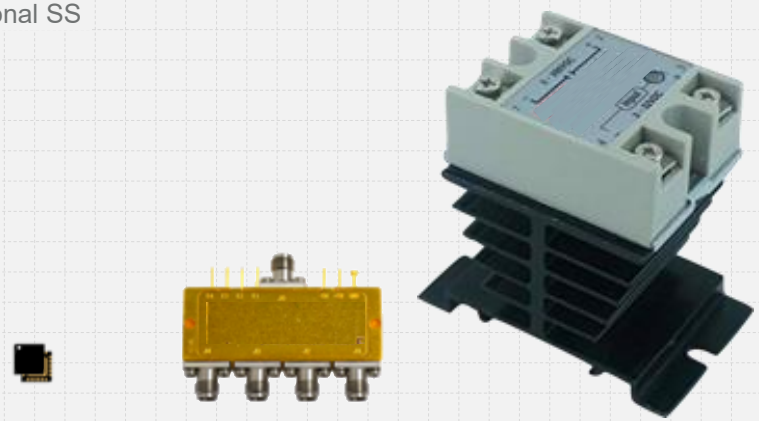
No heatsinks = massive weight, size and cost savings



*Typical Menlo Ron for >200 contacts compared to typical SSR.

SIZE

Conventional SS



<10 mm³ | **10 cm³** | **305 cm³**

ideal switch™

<10 mm³
SP4T RF switch with integrated driver

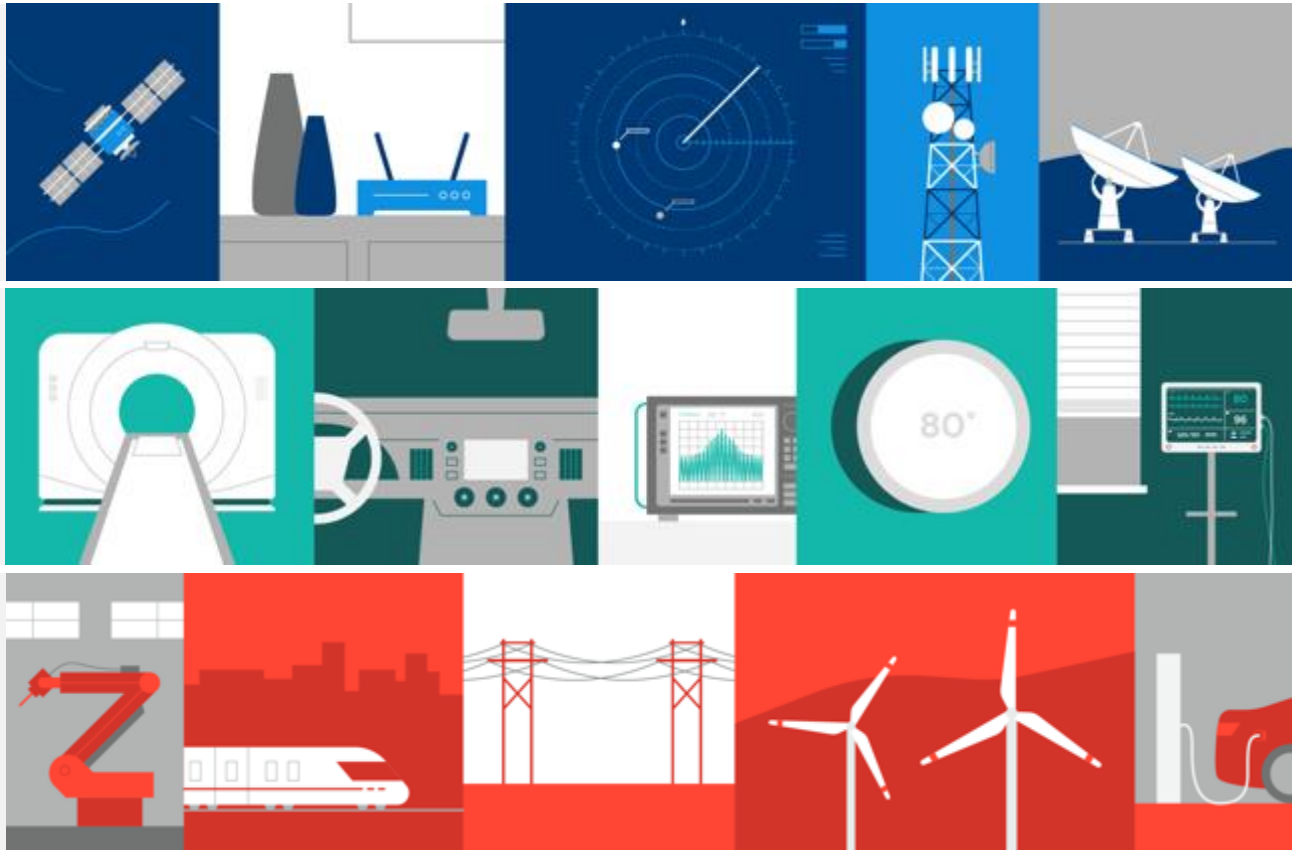
0.03 cm³
High power SP4T RF switch w/driver

0.6 cm³
200V/20A relay with integrated protection

The world of Ideal Switch applications

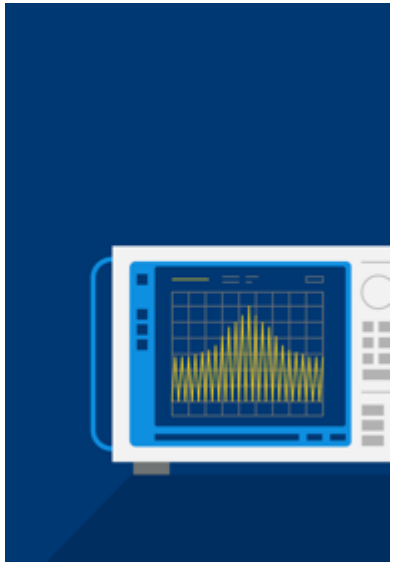
Everything will be smaller, waste less electricity, and be more cost-effective.

	APPLICATIONS	NEEDS
RF/MICROWAVE SWITCHING	5G cell networks Radio Radar Satellite WiFi/Connectivity	Reliability Low distortion Low signal losses DC to mmWave frequency Power efficiency
SIGNAL RELAYS	Telecom Test & Measurement Medical Automotive Consumer	Reliability Fast switching DC & Low frequency Power efficiency Small, light, cheap
SMART AC/DC POWER SWITCHING	Industrial IoT Home automation Battery management Transportation Motor control	Low losses, no heat Speed & reliability Power efficiency Lightweight Smart controls

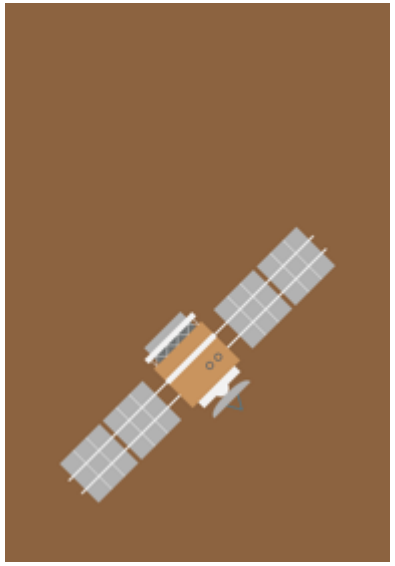


Target Markets

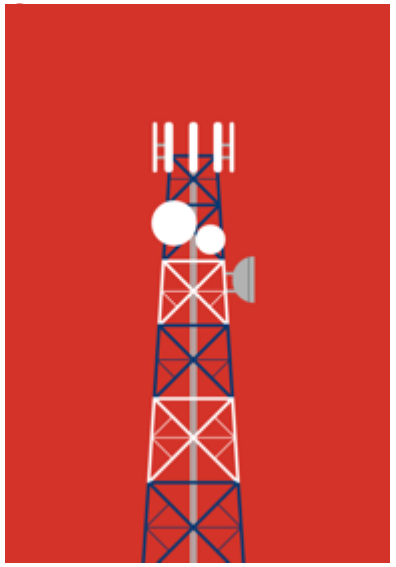
Test & Measurement



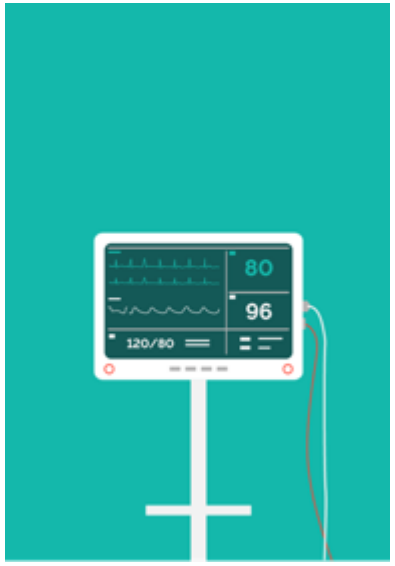
Aerospace & Defense



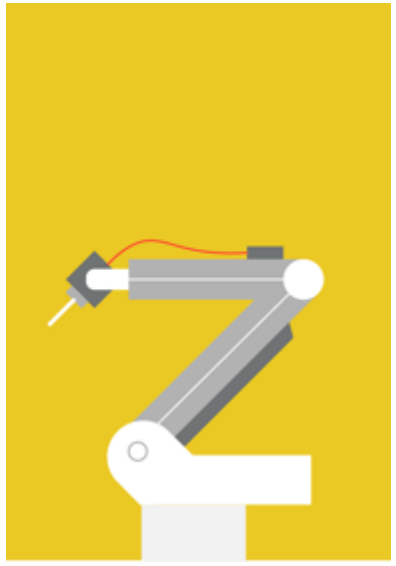
5G & Communication



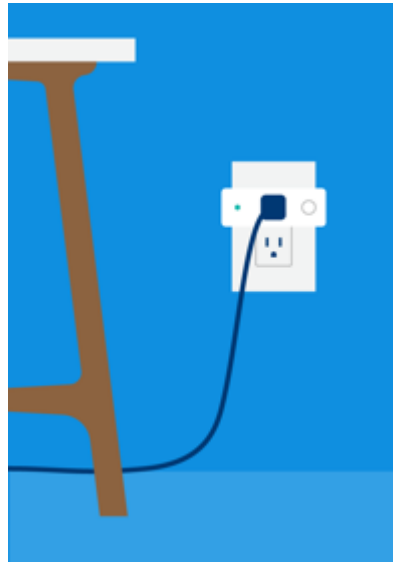
Medical



Industrial IoT



Consumer



Ideal Switch® Products

Product Portfolio – RF & Microwave Products

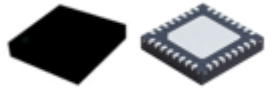


	RF & Microwave				
	MM5230	**MM5130-EDC**	**MM5120**	**MM5140**	**MM5815**
Markets	Telecommunication, Wireless Systems, Aerospace & Defense, Test & Measurement				
Applications	Tunable & Programmable Filters, High-Power Low-Loss RF Switch Matrices, Programmable RF Beam Steering				Rx protection, co-site interference
Switch Type	SP4T				SPST
Frequency Range	DC – 26 GHz		DC – 18 GHz	DC – 8 GHz	DC – 18 GHz
RF Power	25 W (CW), 150 W (pulsed)				500 W blocking (pulsed)
Insertion Loss	0.3 dB @ 6 GHz		0.4 dB @ 6 GHz	0.3 dB @ 3 GHz	0.4 dB @ 6 GHz
Linearity (IP3)	>90 dBm				
Control	Direct HV		SPI/GPIO	SPI/GPIO	Direct HV
DC Supply	89 V (gate)		3.3 V (ctrl), 5 V (V_{CP})	3.3 V (ctrl), 5 V (V_{CP})	89 V (gate)
Lifetime	>3B cycles				>100M cycles
Package	2.5 mm x 2.5 mm 21-pin WLCSP	2.5 mm x 2.5 mm 29-pin WLCSP	5.2 mm x 4.2 mm LGA		5 mm x 4 mm LGA
Operating Temp	-40C to 85C	-40C to 125C	-40C to 85C		-40C to 85C
Availability	**In production**	**Samples: Available** **Prod: Q4 2025**	**In production**		**Samples: Available** **Prod: Q3 2025**

Product Portfolio – High-Speed Products

	High-Speed Digital			
	MM5600	**MM5620**	**MM5622**	**MM5625**
Markets	Semiconductor Test & Measurement, Automated Test Equipment, Aerospace & Defense Equipment			
Applications	High-Speed Digital SoC Loopback Testing, PCIe Gen6, DDR5, MIPI, USB-C, High-Speed Ethernet, etc			
Switch Type	DPDT	2x DP3T Diff **AC** Coupled	2x DP3T Diff **DC** Coupled	2x DP3T Diff **AC** Coupled
Max Data Rate PAM4	40 Gbps	64 Gbps	80 Gbps+	80 Gbps+
Insertion Loss	1.3 dB @ 10 GHz	1.5 dB @ 16 GHz	2.2 dB @ 20 GHz	2.7 dB @ 20 GHz
Control	Serial to Parallel	SPI/GPIO		SPI
DC Supply	5 V (control), 89 V (gate)	3.3 V (control), 5 V (V_{CP})		
Lifetime	> 3B cycles			
Package	8 mm x 8 mm LGA	8.2 mm x 8.2 mm LGA		
Operating Temp	-40C to 85C			
Availability	**In production**			

Product Portfolio – Drivers & Power



	Drivers	Power Chip	Power Module
	MM101	**MM92xx**	**DC Module xx**
Markets	All	Hi-Rel, Data Center, Industrial Automation	Hi-Rel, Data Center, Industrial Automation
Applications	All	Replacement for Electro-Mechanical relays, contactors and circuit breakers	Replacement for Electro-Mechanical relays, contactors and circuit breakers
Switch Type	High voltage CP + 8-channel driver	SPST	SPST
DC Current		15 A (AC or DC), 10 mΩ*	30A, 15 mΩ*
DC Carry/Standoff Voltage	---	400 V (AC or DC)*	800 VDC
Control	SPI/GPIO	Direct	Direct
DC Supply	3.3 V (control), 5 V (V_{CP})	90 V (gate)	90V
Lifetime	---	>100M cycles	>10M cycles
Package	5 mm x 5 mm QFN 1.6 mm x 2.4 mm WLCSP	5 mm x 5 mm WLCSP	14 pin 40 x 30 mm*
Operating Temp	-40C to 85C		
Availability	**In production**	**Engr. Samples: Q2, 2027** **Production: Q4 2027**	**Engr. Samples: Q1, 2027**

Product Roadmap

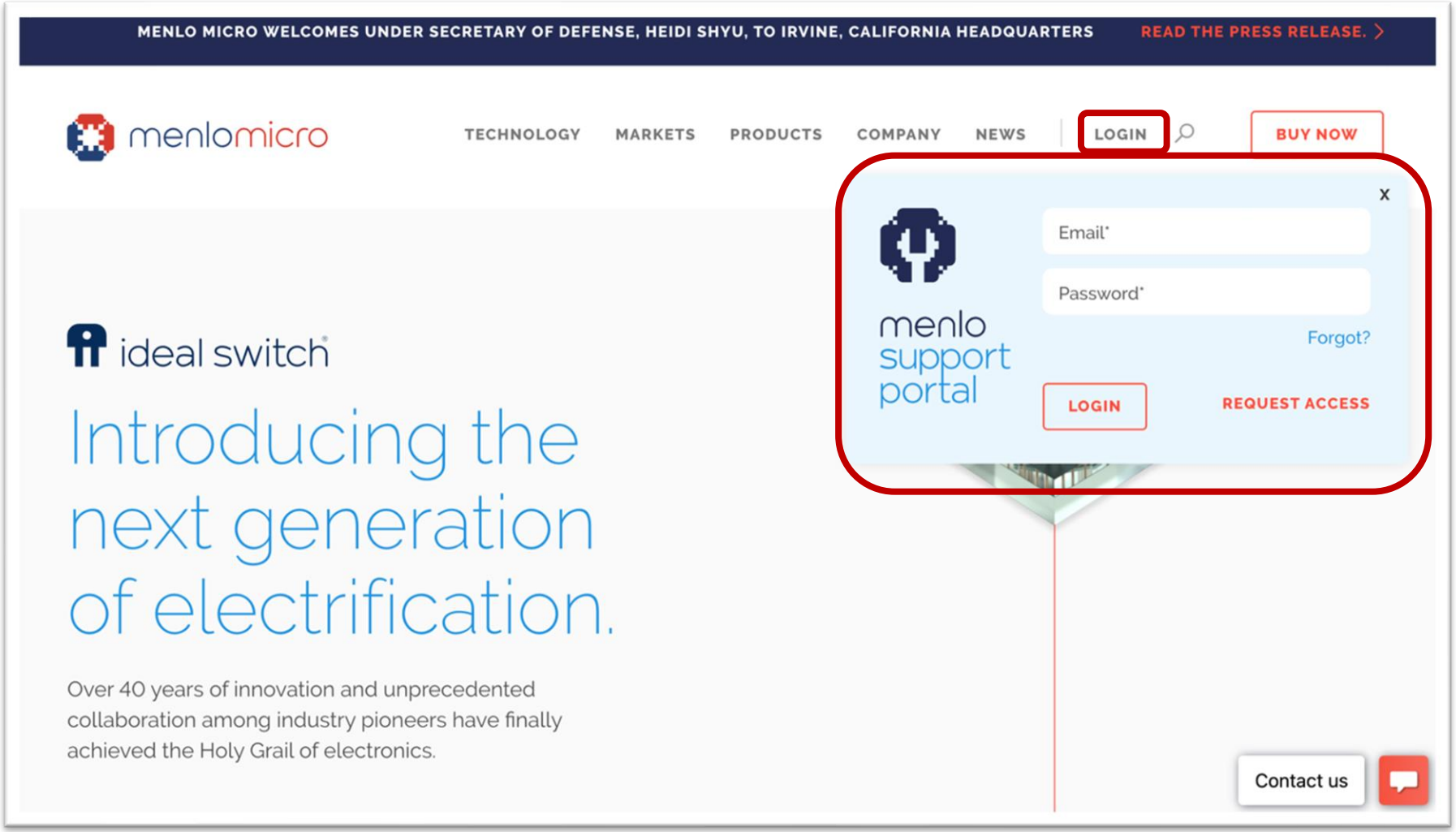
Driving and accelerating product roadmap based on our customers' most challenging requirements

	Current Products	2025 Roadmap	Future Product Roadmap
RF & MICROWAVE SWITCHES	**MM5130** DC-26GHz 25W, SP4T **MM5120** DC-12GHz SP4T w/CP **MM5140** DC-8GHz SP4T w/CP **MM5230** DC-26GHz 25W, SP4T **MM5130-EDC** DC-26GHz 25W, SP4T **MM5815** 400W RF Limiter SPST **MM5170** DC-40GHz SP4T **MM58xx** SPDT,70GHz+	**MM60xx** DC-18GHz Switched & Tunable Filters **MM61xx** DC-18GHz TDU, Beam-formers	• Higher frequency, isolation • Smaller form factors • Higher reliability • System-in-package (SiP) heterogeneous integration with RF/digital/mixed signal ICs • 3D glass integration with passive devices
HIGH SPEED DIGITAL LOOPBACK	**MM5600** 40Gbps DPDT **MM5620** 64Gbps Diff. Loop. AC Coup. **MM5622** 64Gbps Diff. Loop. DC Coup. **MM5625** 64Gbps Asymmetric AC/DC Coup. **MM56xx** 128Gbps-224Gbps 50% package shrink AC/DC coup		• Higher data rate (PCIe Gen7, and 224Gbps) • Smaller form factor, higher density • Custom/multichip switch configurations
LF SIGNAL RELAY	True replacement for high volume, low-cost PhotoMOS relays, EMR, reed relays	**MM12xx** DC-3GHz 4xSPST 500mA	• Smallest form factor, highest density • Highest elec. performance over all key specs • Multiple switch configurations planned
POWER SWITCHES		**MM92xx** 39mm² 400V/15A <10mΩ, SPST **MM9xxx** 800V/30A DC Module	• Higher voltage, current, & power density • Smaller form factor • Lower Ron/mm² • Modules with integrated sense & control

Website Resources – The Menlo Support Portal

Additional product support/documentation can be found by logging in through Menlo's website http://www.menlomicro.com/

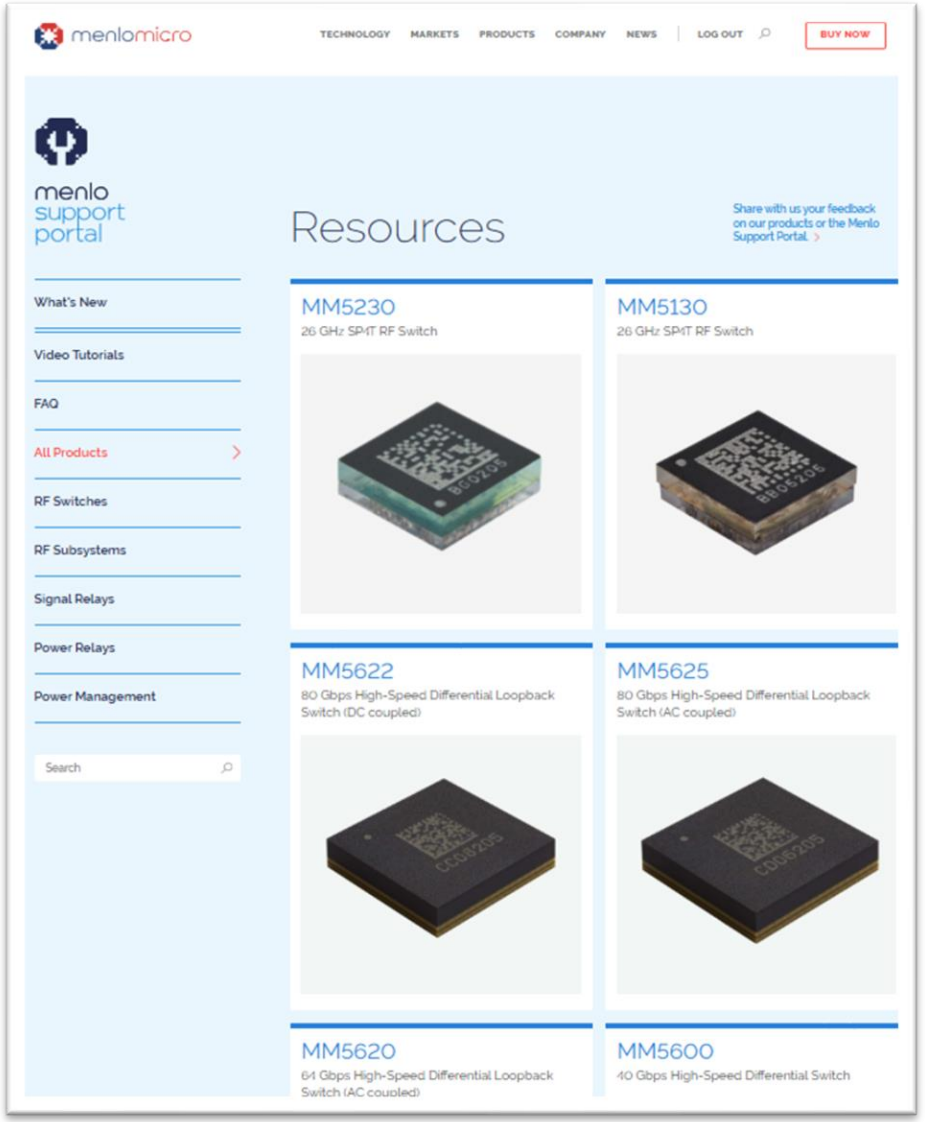
- Users can sign up by clicking on "Login" and then "Request Access"
- Access is typically granted within 24hrs



Website Resources – The Menlo Support Portal

Each Series consists of the following where you can find:

- Product Briefs
- Application Notes
- Qualification Reports
- S-Parameters
- Transmission Line Models
- CAD Drawings
- Assembly Instructions
- RoHS/REACH Certificates
- Eval Board GUI
- Eval Board Instructions
- Video Tutorials
- FAQs
- Product Images



Menlo having a major impact in the semiconductor test market

Working to solve the most critical, high-performance test challenges in the semiconductor market

- Menlo Micro has gained significant traction with the world's most advanced semiconductor companies, helping them to increase their test coverage and drastically reduce cost, for testing the highest performance ICs in the market
- Menlo Micro has ***over 20 major companies*** adopting our highly integrated high-speed I/O loopback relays (MM56xx family), ***testing PCIe Gen6 (64Gbps) in production***
- Menlo's customers cover AI/ML, GPU, CPU, Network processors, Memory controllers, and many other SOCs which have high-speed ports that need to be tested, at speed, in high volume production. This includes both final test and wafer sort solutions
- Beyond HPC market, we have a growing base of customers for RFIC and Mixed-Signal/Analog & Power test solutions

Partners for production

** Over 2000 production load boards built in 2024 **

Proactively building relationships with PCB supply chain to ensure DFM & smooth transition to production

PCB Partner	Experience Level	Menlo Products	PCB Partner	Experience Level	Menlo Products
CHPT	Production (4 years)	MM5130, 5230, 5140, 5620	PTSL	Design (Prod 2025)	MM5620, MM5625
R&D Altanova	Production (3 years)	MM5130, 5230, 5140, 5620, 5622, 5625	SYNERGIE CAD GROUP	Design (Prod 2025)	MM5620, MM5622
GORILLA circuits	Production (5 years)	MM5130, 5120, 5140, 5230, 5620, 5622	DIS TECH	Design (Prod 2025)	MM5622
雍智科技股份有限公司 KEYSTONE MICROTECH CORPORATION	Production (3 years)	MM5130, 5230	TECHNOPROBE	Design (Prod 2025)	MM5620
TESSOLVE	Production (1 year)	MM5620	StepSystem	Design	MM5130, 5120, 5620
ZERONE	Design (Prod 2025)	MM5600, 5620	TSE	Design	MM5620
DTS	Design (Prod 2025)	MM5620	FormFactor™	TBD	TBD

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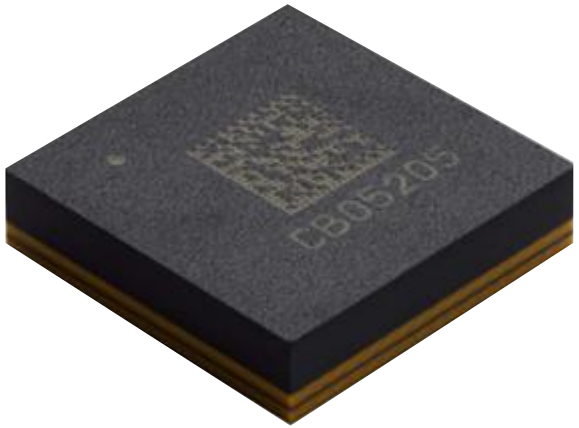
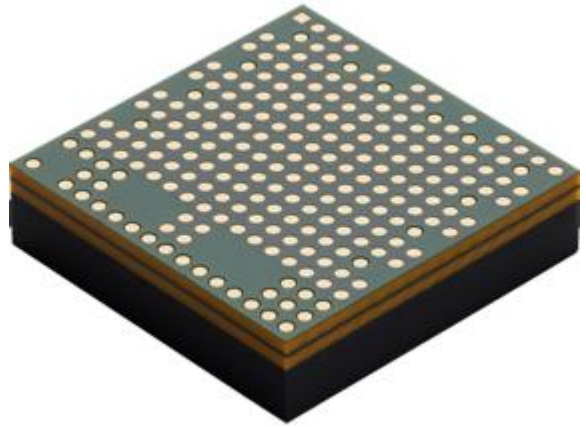
MM562x HSD Product Introduction

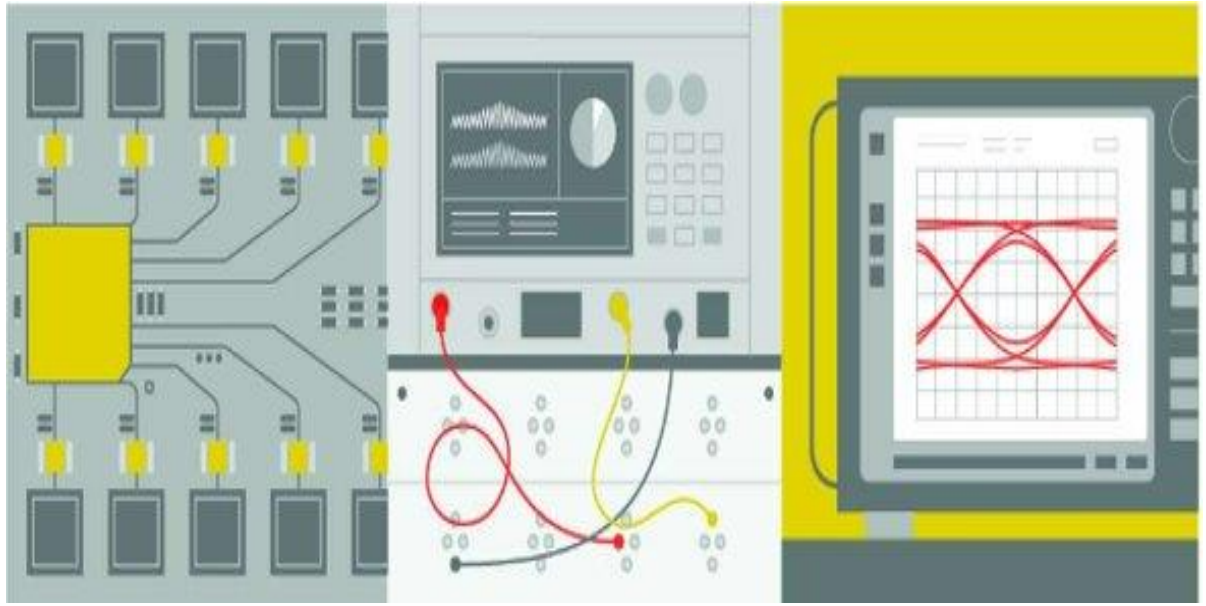




MM562x – Target Markets & Applications

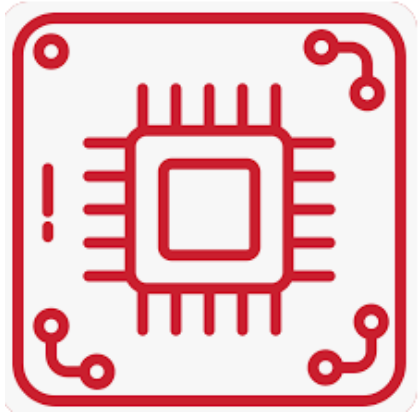
Target Markets

- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Testing
- Compliance and Loopback Testing
- Aerospace & Defense Equipment



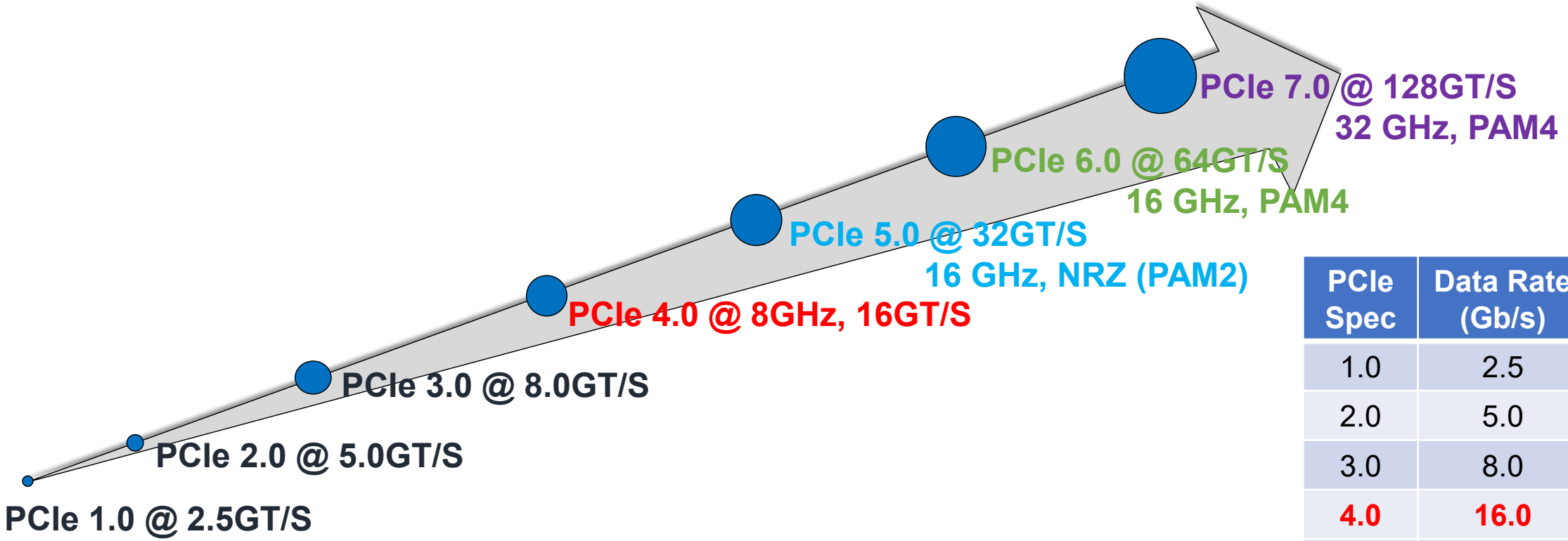
Target Applications

- High-Speed Digital SoC Testing
  PCIe Gen 5 & 6, SerDes, USBx.x, InfiniBand, HDMI…
- Optical-Electrical Module Testing
- High Speed Signal Routing
- Differential Switch Matrices



The History of PCI Express

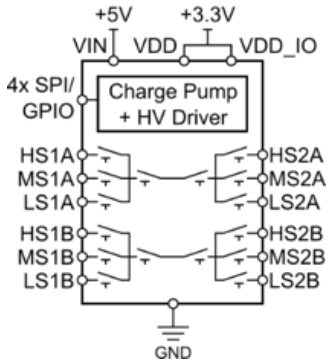
Doubling the Data Rate every 2 to 4 years



PCIe Spec	Data Rate (Gb/s)	Year
1.0	2.5	2003
2.0	5.0	2007
3.0	8.0	2010
4.0	16.0	2017
5.0	32.0	2019
6.0	64.0	2021
7.0	128.0	2025

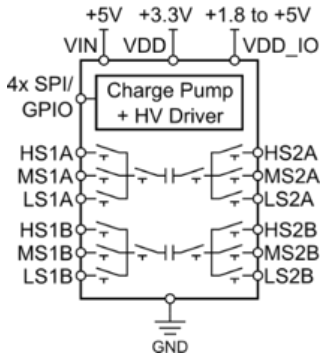
Not just PCIe, but Ethernet at 224Gbps and will double again… **soon**!

High-Speed Digital Loopback Roadmap



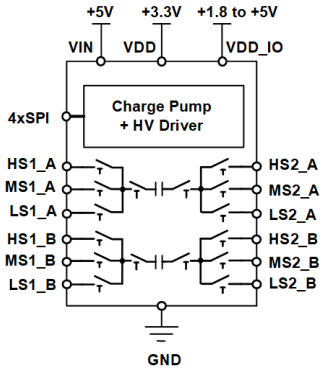
MM5620

Released in Apr 2023



MM5622

Released in Sep 2024



MM5625

Enhanced RF + 7 HV Gate Control

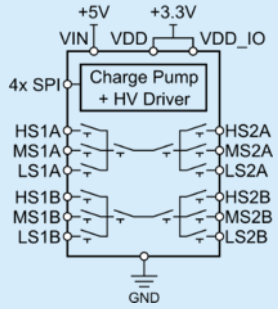
Released in June 2025

Supports asymmetric buses

MM5627

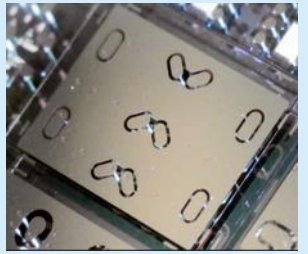
Enhanced RF + 7 CTRL

2nd Half 2025



Additional control flexibility for testing asymmetric buses

2026



MM56XX

224 Gbps Device

Mid 2026

Step-function improvement in size and performance
AC & DC, 85ohm & 100ohm versions planned

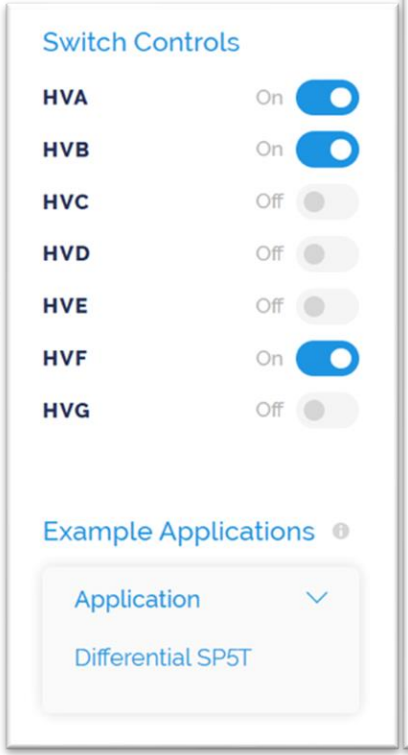
https://menlomicro.com/products/high-speed-loopback-solutions

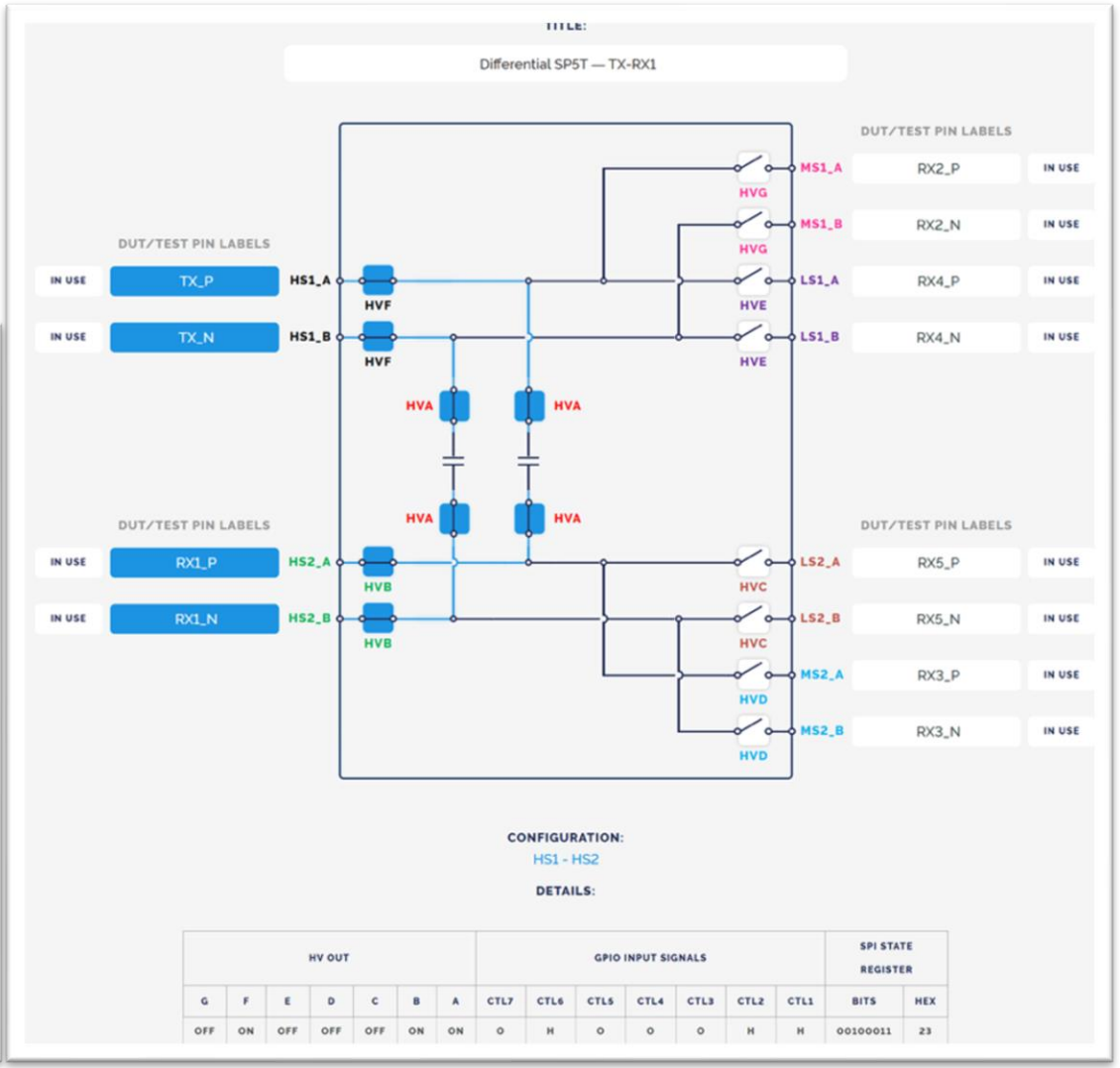
Tools & Guidelines to Implement onto Test Boards

Software Tools in Board Design and Planning:

- The number of high-speed channels, combined with all the various connection options makes for a highly flexible, yet complex switching system
- The goal of Menlo's Ideal Switch® HSIO SignalFlow Studio interactive web tool is to:
  - Clearly show how these highly sophisticated loopback switching systems can be configured, from end application point-of-view
  - Come pre-loaded with common use cases like PCIe, USB, DDR5, CXL, etc.
  - Reduce errors at schematic level and optimize the usage before boards get built

Ideal Switch®
HSIO SignalFlow
Studio





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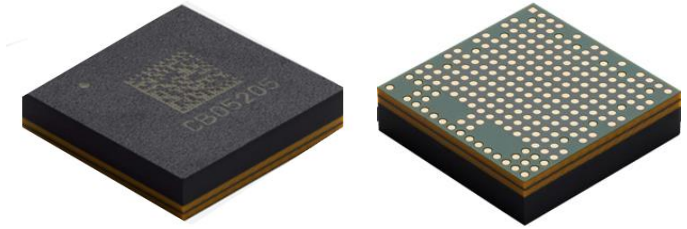
MM5620

- 64 Gbps High-Speed Differential Loopback Switch (AC coupled)



MM5622

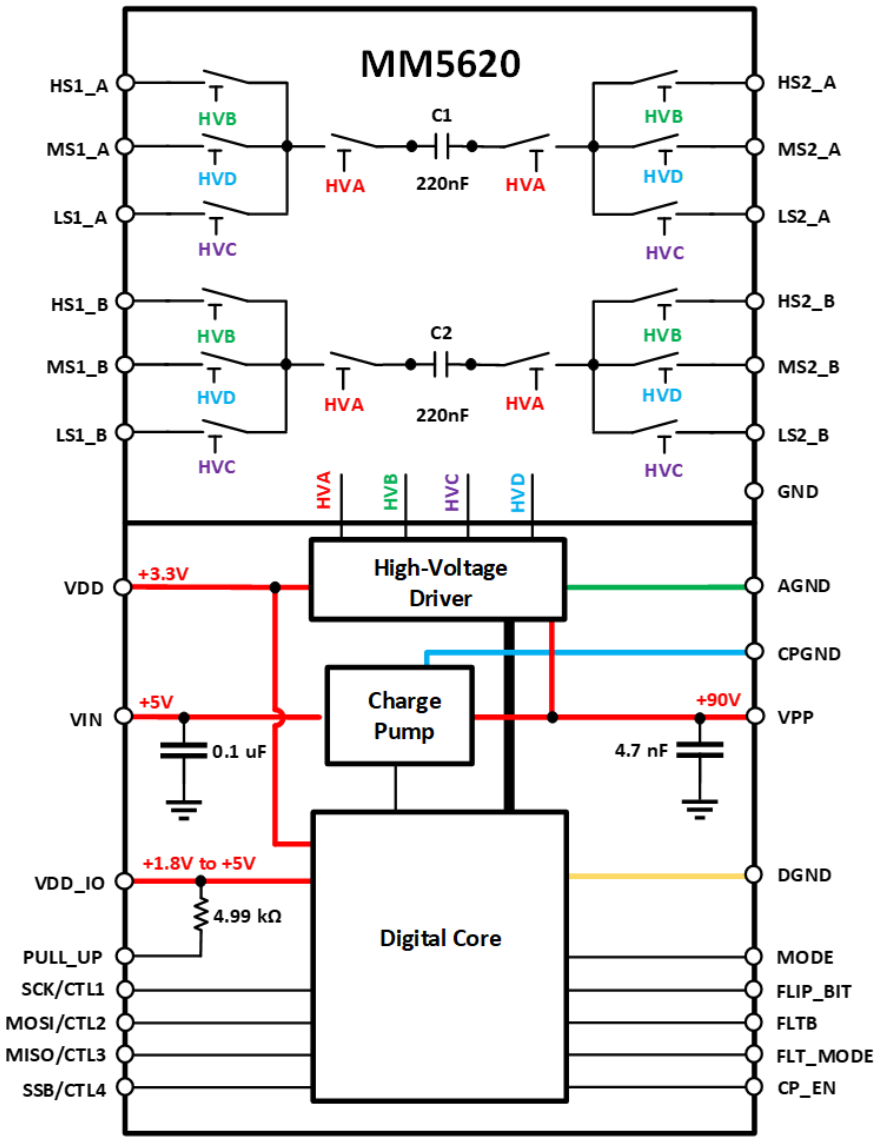
- 80 Gbps+ High-Speed Differential Loopback Switch (DC coupled)

MM5620 – Product Highlights

- DC to 20 GHz range
- DP3T (differential mode) with Loopback Mode
- Built-in AC coupling capacitors
- Integrated charge pump & high-voltage driver
- Power supply 5 V (voltage booster) 3.3 V (analog)
- SPI and GPIO interface
- Built-in passive components
  - Internal VPP capacitor
  - Internal 4.99k pullup resistor
  - Internal 0.1uF/10V VIN to CPGND bypass capacitor
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA

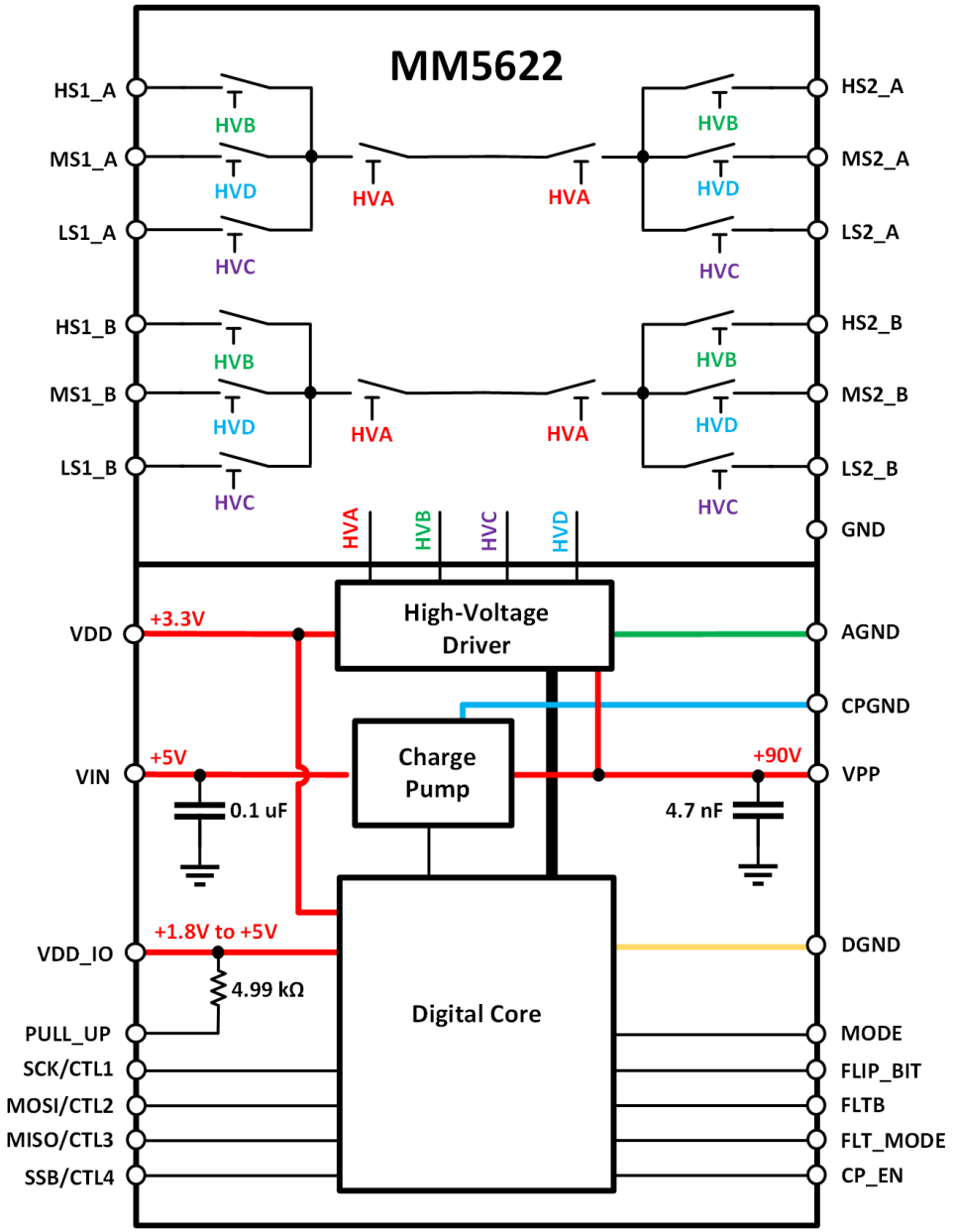
[Menlo MM5620 Datasheet (menlomicro.com)]

[MM5620-01NDB_Qual_and_Characterization_Report_Rev-1.pdf (menlomicro.com)]



MM5622-01NBX – Product Highlights

- DC to 20 GHz range
- DP3T (differential mode) with Loopback Mode
- DC coupled Signal Paths only
- Integrated charge pump & high-voltage driver
- Power supply 5 V (voltage booster) 3.3 V (analog)
- SPI and GPIO interface
- Built-in passive components
  - Internal VPP capacitor
  - Internal 4.99k pullup resistor
  - Internal 0.1uF/10V VIN to CPGND bypass capacitor
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA

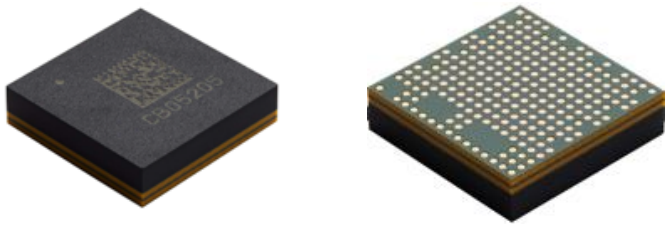


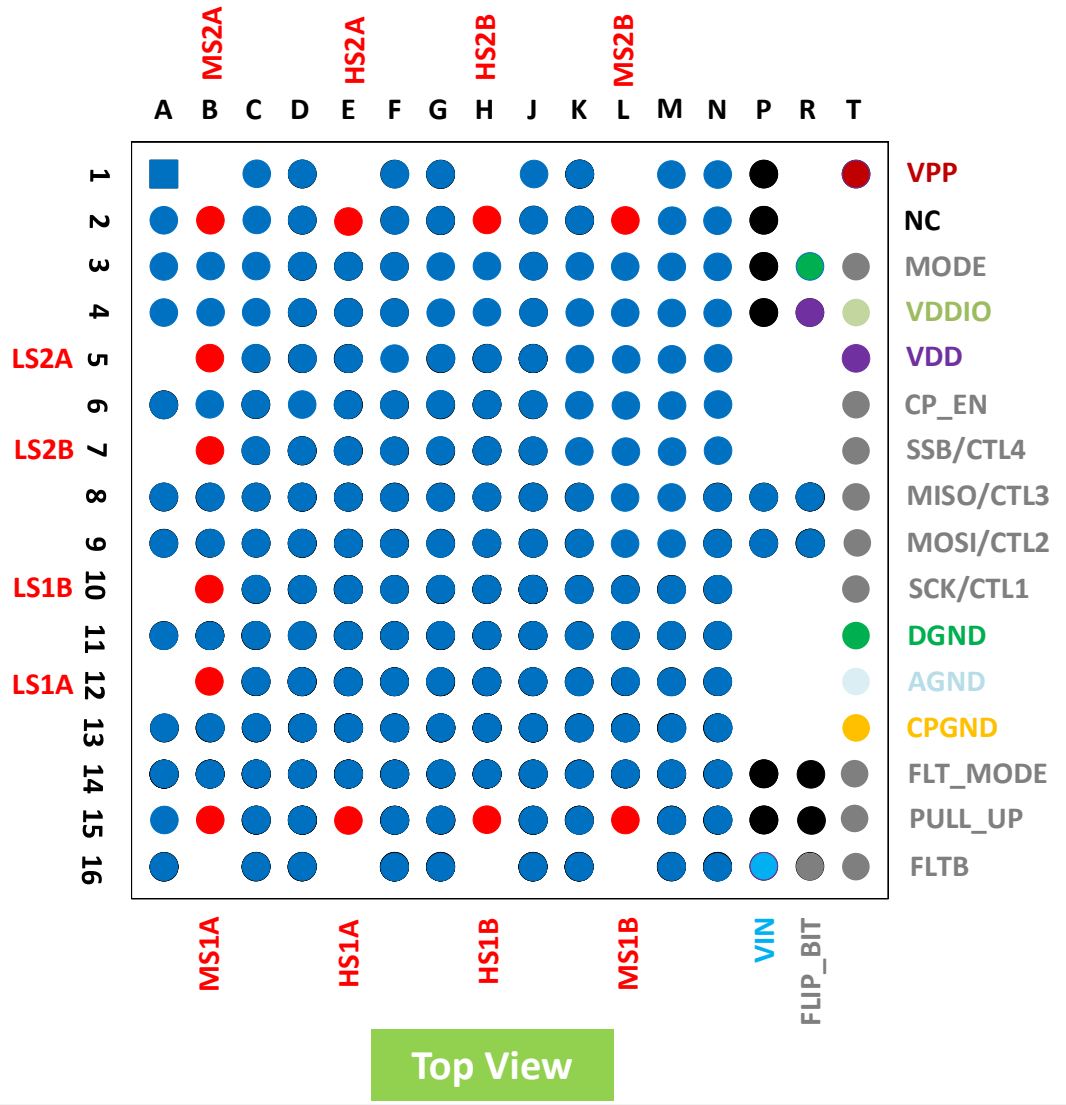
[Menlo MM5622-01NBX_Datasheet (menlomicro.com)]
[MM5622-01NBX_Qual_and_Characterization_Report_Rev-1_1]

MM5620/MM5622 - LGA 16x16 Footprint Diagram

Key Features

- Size: 8.2 x 8.2 mm^2
- 16x16 LGA array
- 0.5 mm pitch / 0.3mm pad diameter
- Internal VPP capacitor
- Internal 4.9k pullup resistor
- Internal 0.1uF/10V VIN/CPGND cap



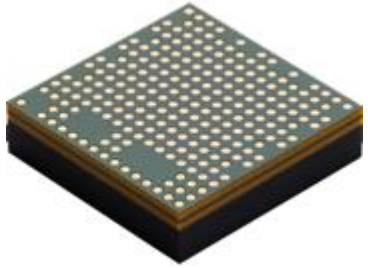


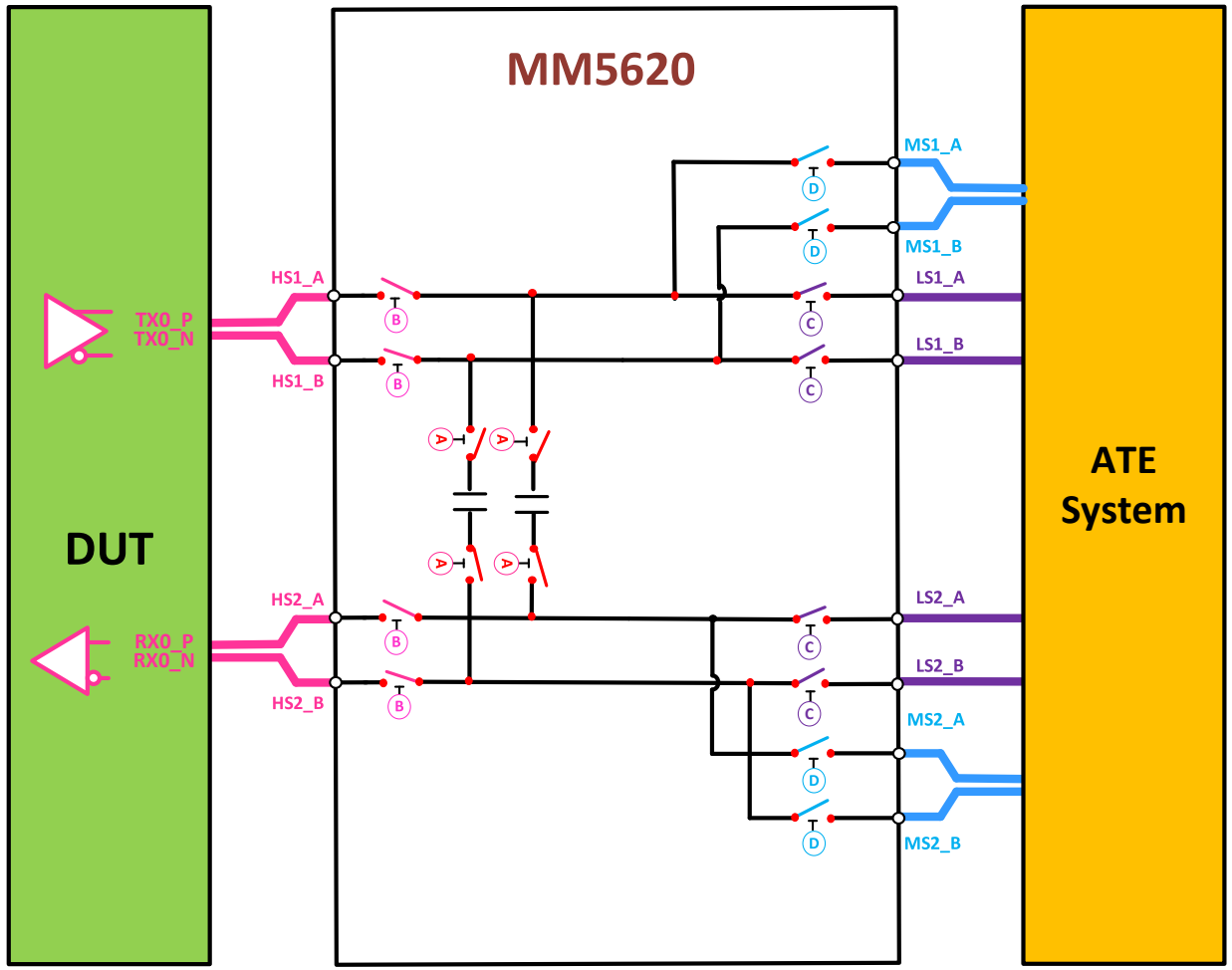
Top View

MM5620 – Only way to perform (3) key tasks in production

1. High-Speed Path (HS) allows for full compliance at-speed testing with DUT loopback
2. Med-Speed Path (MS) allows for scan and digital patterns sourced from ATE
3. Low-Speed Path (LS) allows for full DC parametric testing from ATE

- All functions enabled with a single, flexible high performance relay
- NO NEED FOR DUAL-INSERTION TESTING
- All critical routing built in with AC coupling caps drastically simplifying layout for PCB designer, easing SI challenges at high-speeds



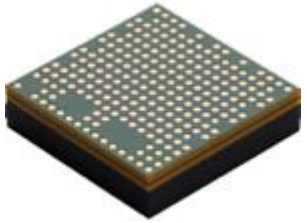


Enabling the Production of the World's Most Complex ICs

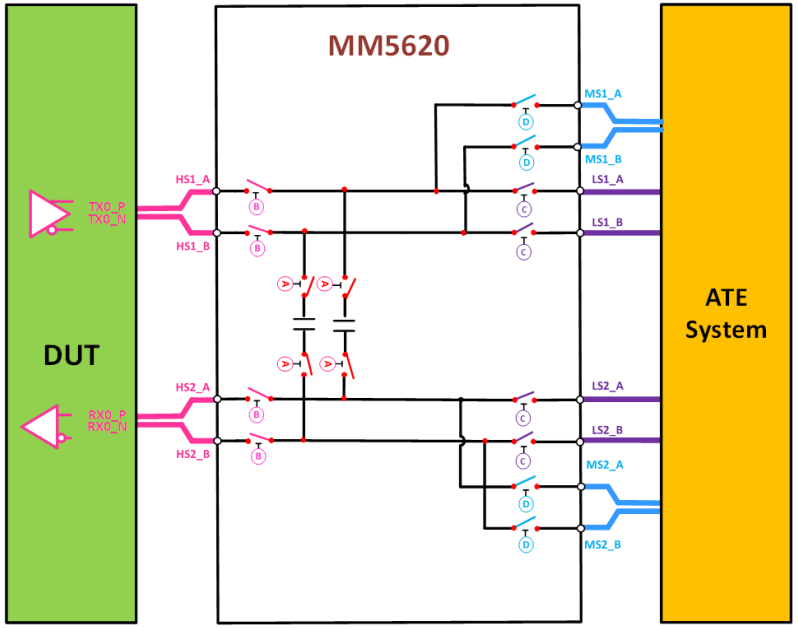
The explosion of high-speed digital interfaces on AI/ML chips and other processors is creating significant challenges

- **The Problem**: Explosion of high-speed digital interfaces in High-Performance-Computing (HPC) devices is challenging to test cost-effectively in production.
  * Relays are too big, can't achieve the speeds
  * Semiconductor switches can't pass DC or high speeds
- **Applications:** GPU/CPU, AI/ML Data Center, Mobile Processors, HBM Interfaces
- **Buses:** PCIeGen5/6, DDR5, DisplayPort, USB-C, Ethernet

- **The Solution:** Miniature relay "systems" based on Ideal Switch technology, on *production test boards*



MM5620

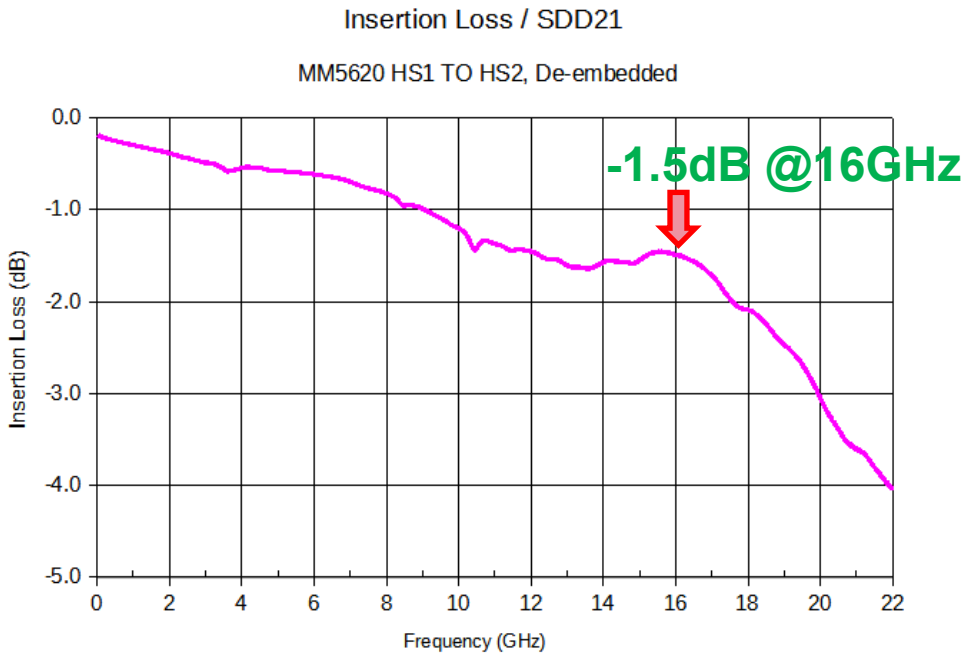


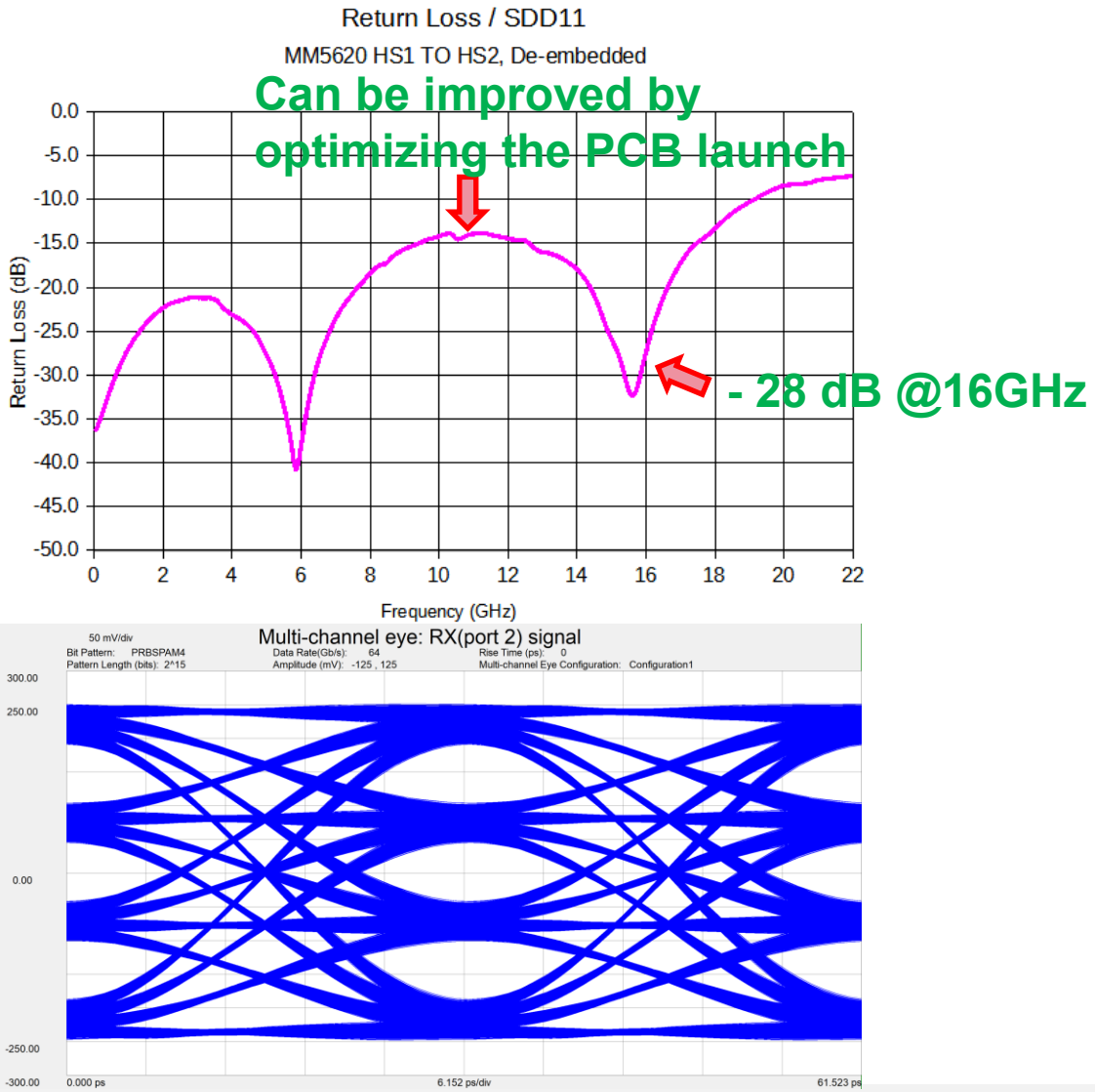
- **Benefits/Impact**:
  - *Full compliance testing* via direct loopback for all digital buses to 64Gbps, including PCIe Gen5,6
  - Ability to simultaneously connect to Automated Test Equipment for *full DC* and *Digital* test sequences
  - This unique "all-in-one" digital multiplexing solution can eliminate multiple test insertions as well as the need to build multiple versions of extremely expensive test boards (> $100k each)

The Ideal Switch® is the only technology capable of enabling the full characterization of the world's latest generation processors, while simultaneously saving > $100k in operational costs

MM5620 S-Parameter Performance (HS1 to HS2 Signal Path)

Frequency Domain Analysis





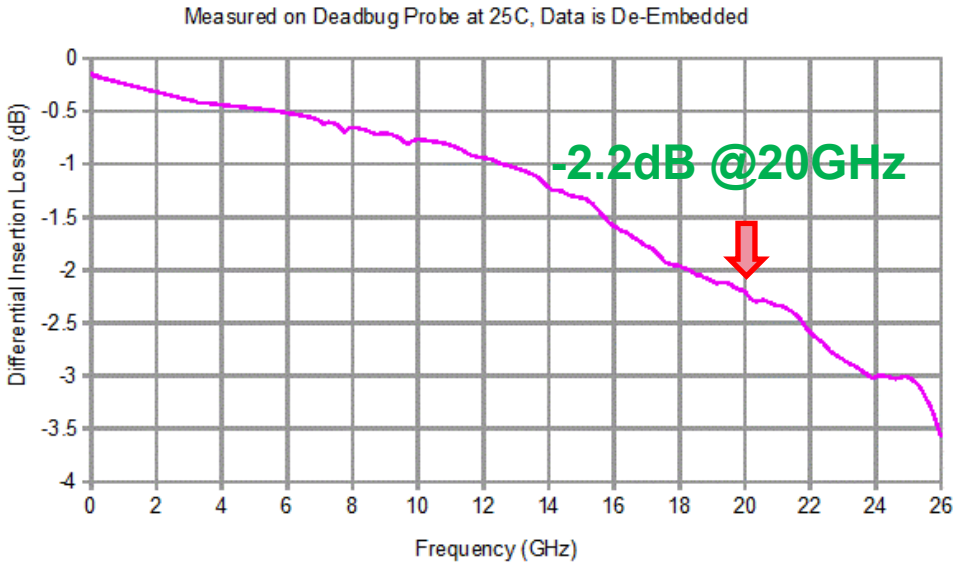
Time Domain Analysis

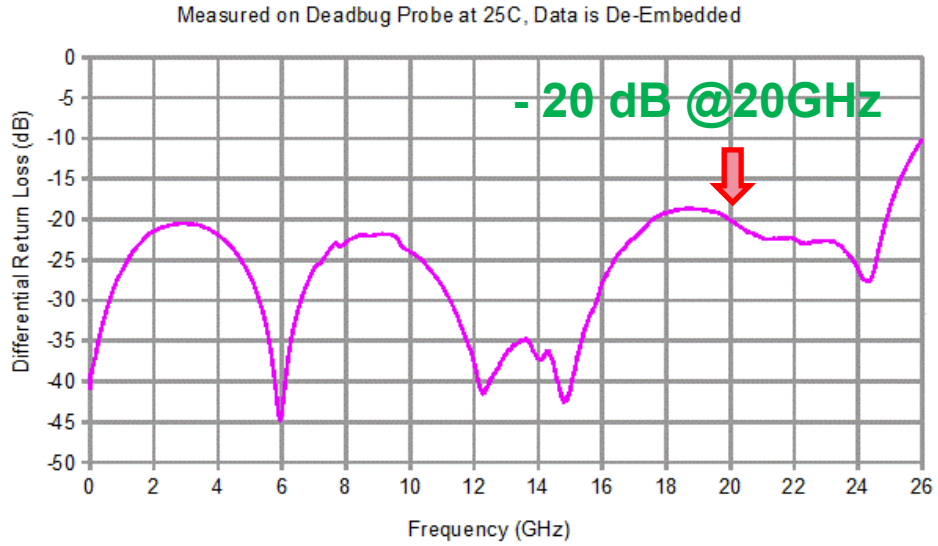
Eye-Diagram Test Conditions

- PCIe Gen6
- PAM4, 32 Gbaud (64Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)

MM5622-01NBX S-Parameter Performance (HS1 to HS2 Signal Path)

Frequency Domain Analysis

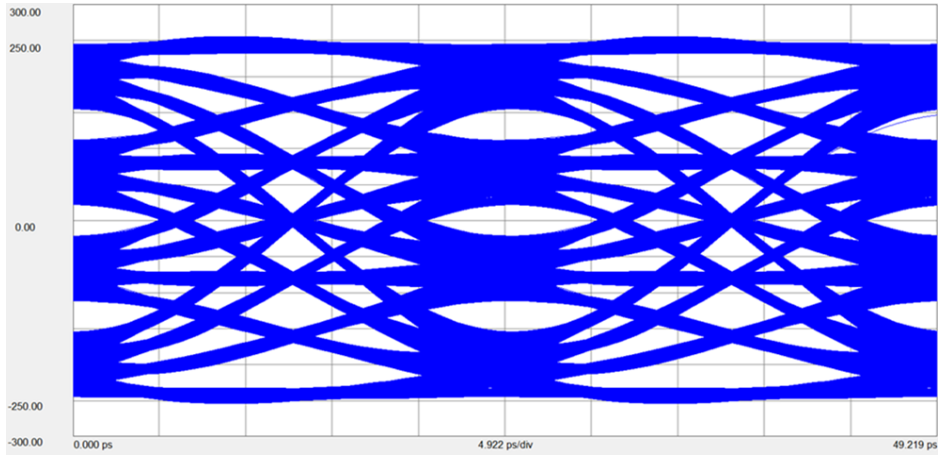




Time Domain Analysis

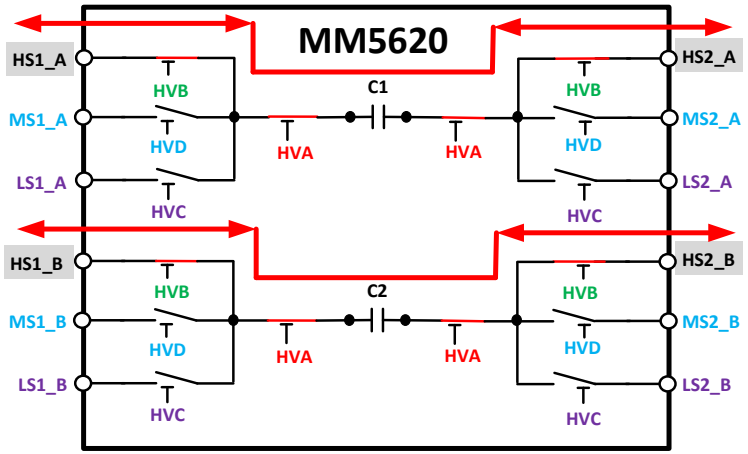
Eye-Diagram Test Conditions

- PAM4, 40 Gbaud (80Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)



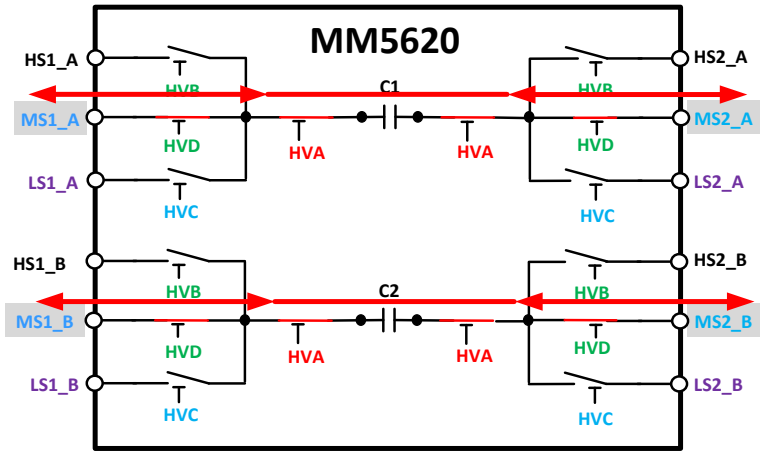
MM5620/MM5622 – Six Major Differential Signal Paths

- Three signal paths going through the AC- coupling capacitors for the MM5620 device
  - Case 1: High Speed 1 to High Speed 2
  - Case 2: Medium Speed 1 to Medium Speed 2
  - Case 3: Low Speed 1 to Low Speed 2



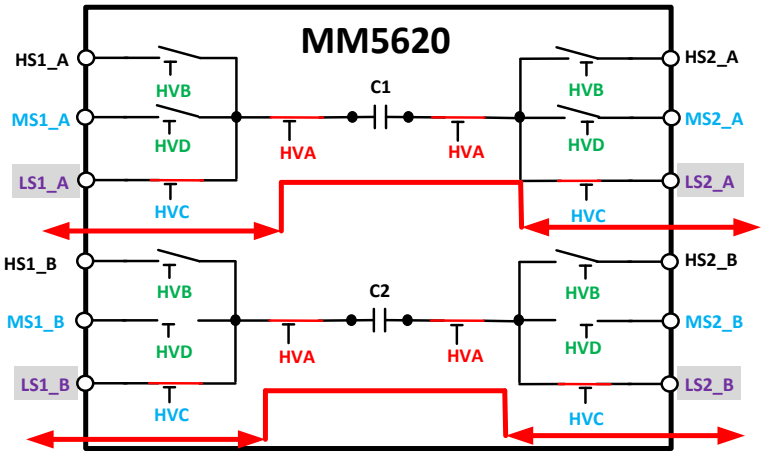
HS1 ↔ HS2

Case 1



MS1 ↔ MS2

Case 2

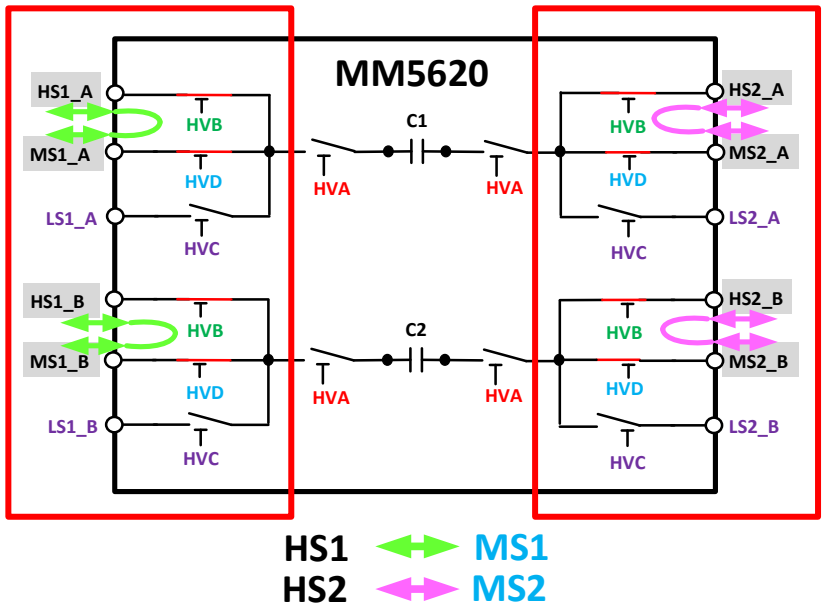


LS1 ↔ LS2

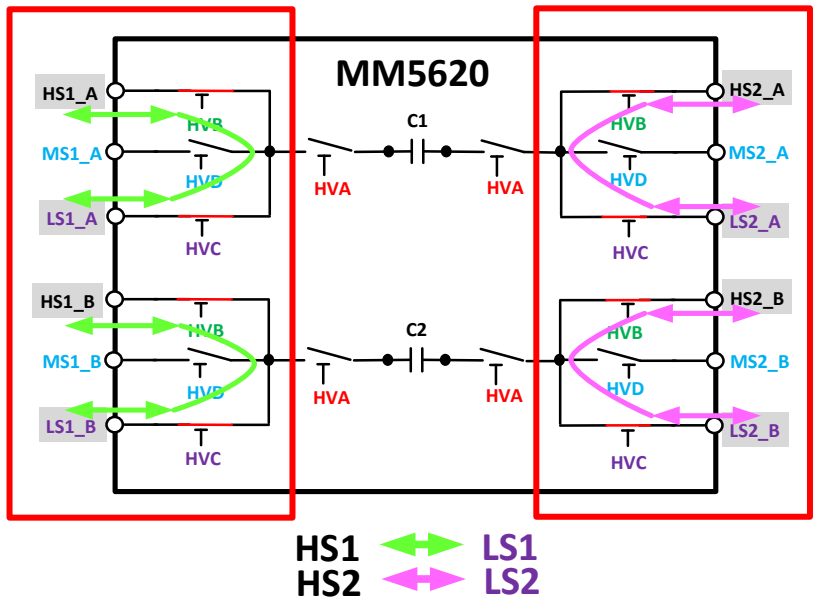
Case 3

MM5620/MM5622 – Six Major Differential Signal Paths

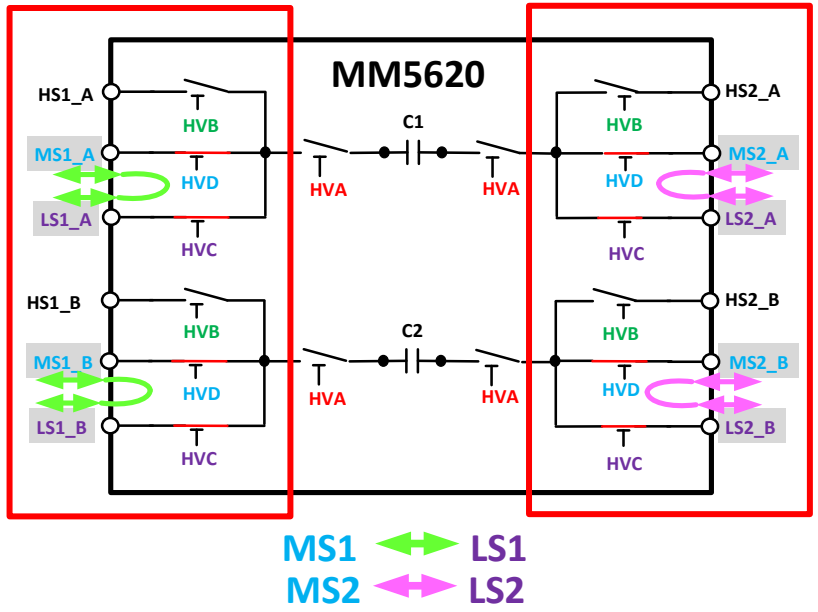
- Additional three DC-coupled signal paths for the MM5620
  - Case 4: High Speed 1 to Medium Speed 1 and High Speed 2 to Medium Speed 2
  - Case 5: High Speed 1 to Low Speed 1 and High Speed 2 to Low Speed 2
  - Case 6: Medium Speed 1 to Low Speed 1 and Medium Speed 2 to Low Speed 2



Case 4



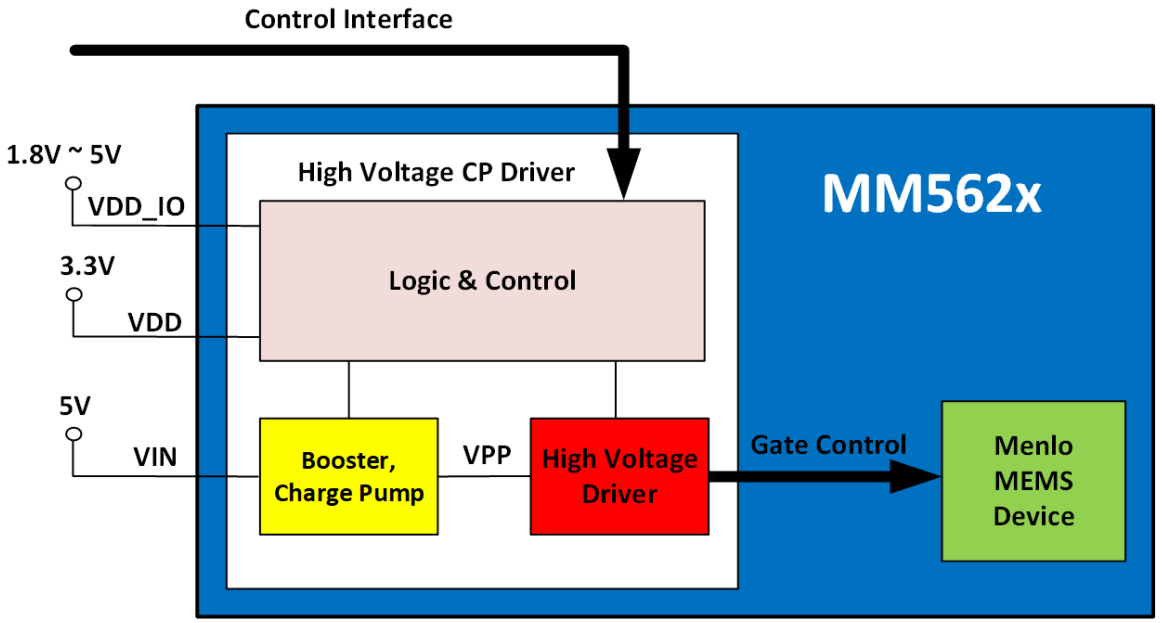
Case 5



Case 6

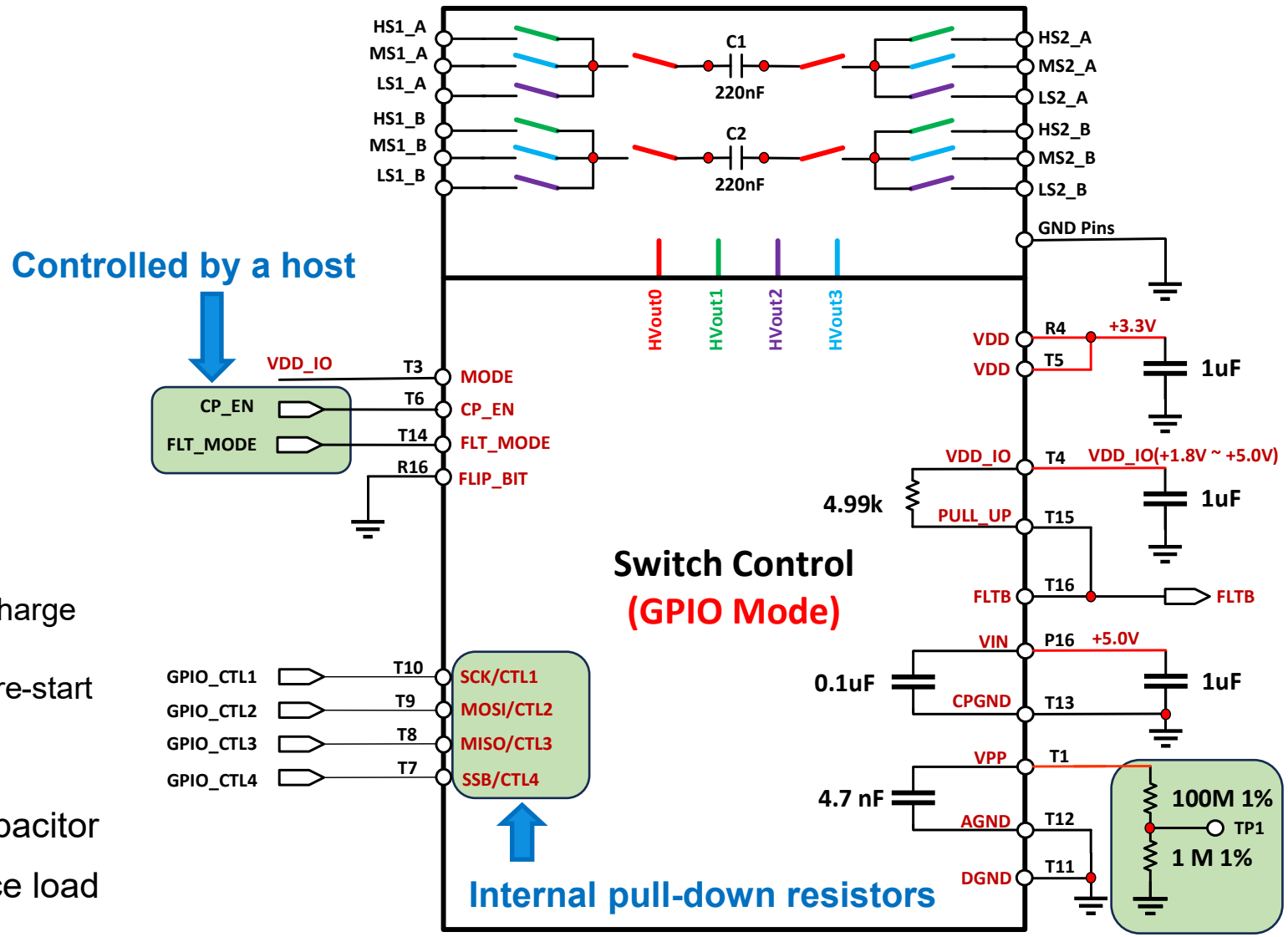
MM5620/MM5622 - MEMS Switch Control Block Diagram

- The communication interface:
  - GPIO or SPI for MM5620/MM5622
- VDD_IO: Digital I/O supply (+1.8V to +5.0V)
- VDD: +3.3V supply to analog circuits
- VIN: +5V supply to the internal charge pump
- Should not need to sequence the power supplies



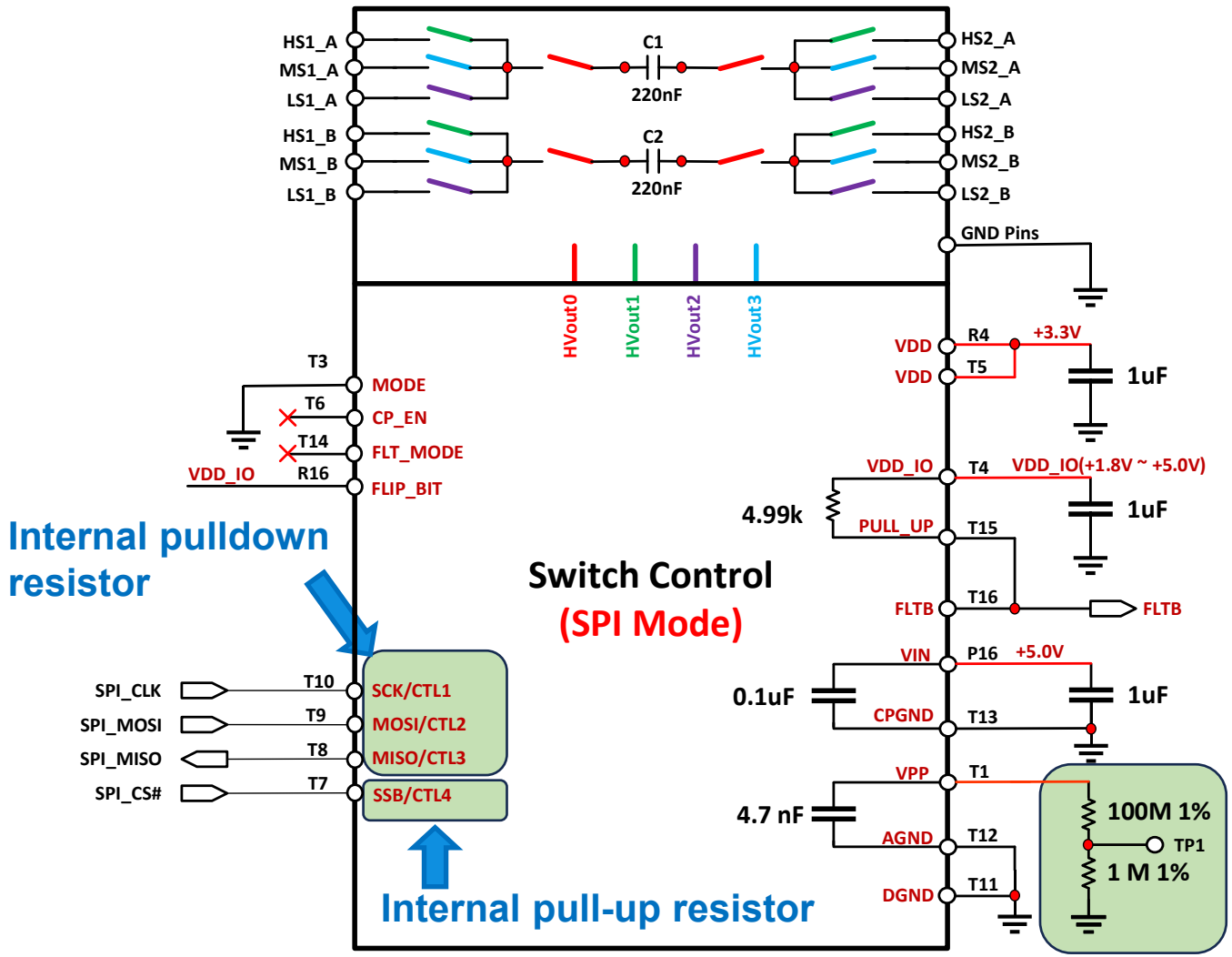
MM5620/MM5622 – External Circuit for GPIO Mode

- Enable the GPIO Mode:
  - MODE: Connect to VDD_IO
  - FLIP_BIT: Connect to GND
- Enable the Charge Pump
  - CP_EN: Connect to VDD_IO
- Disable the Fault Mode:
  - FLT_MODE: Connect to VDD_IO
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CP_EN pin low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor
- VPP can be probed with a high resistance load



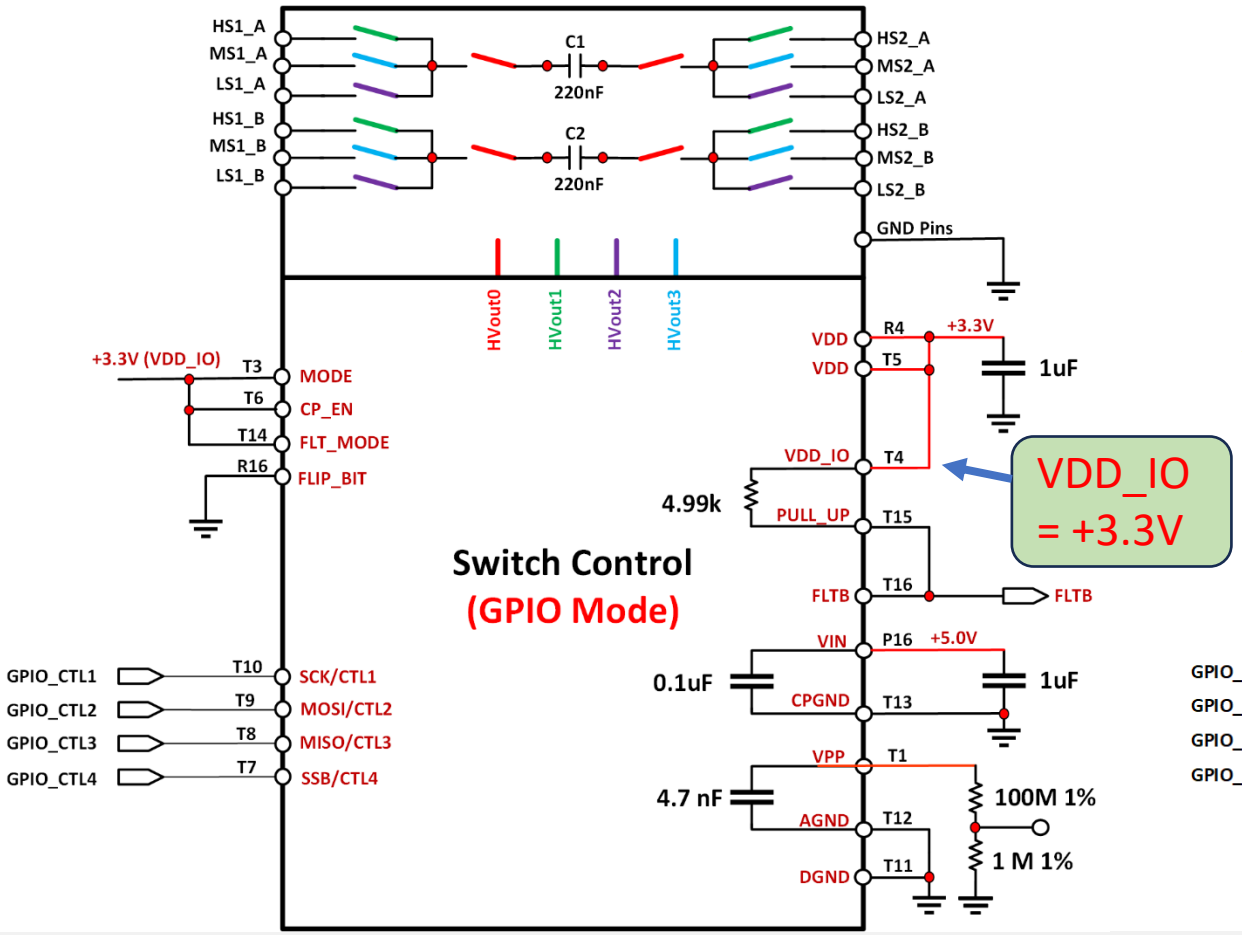
MM5620/MM5622 – External Circuit for SPI Mode

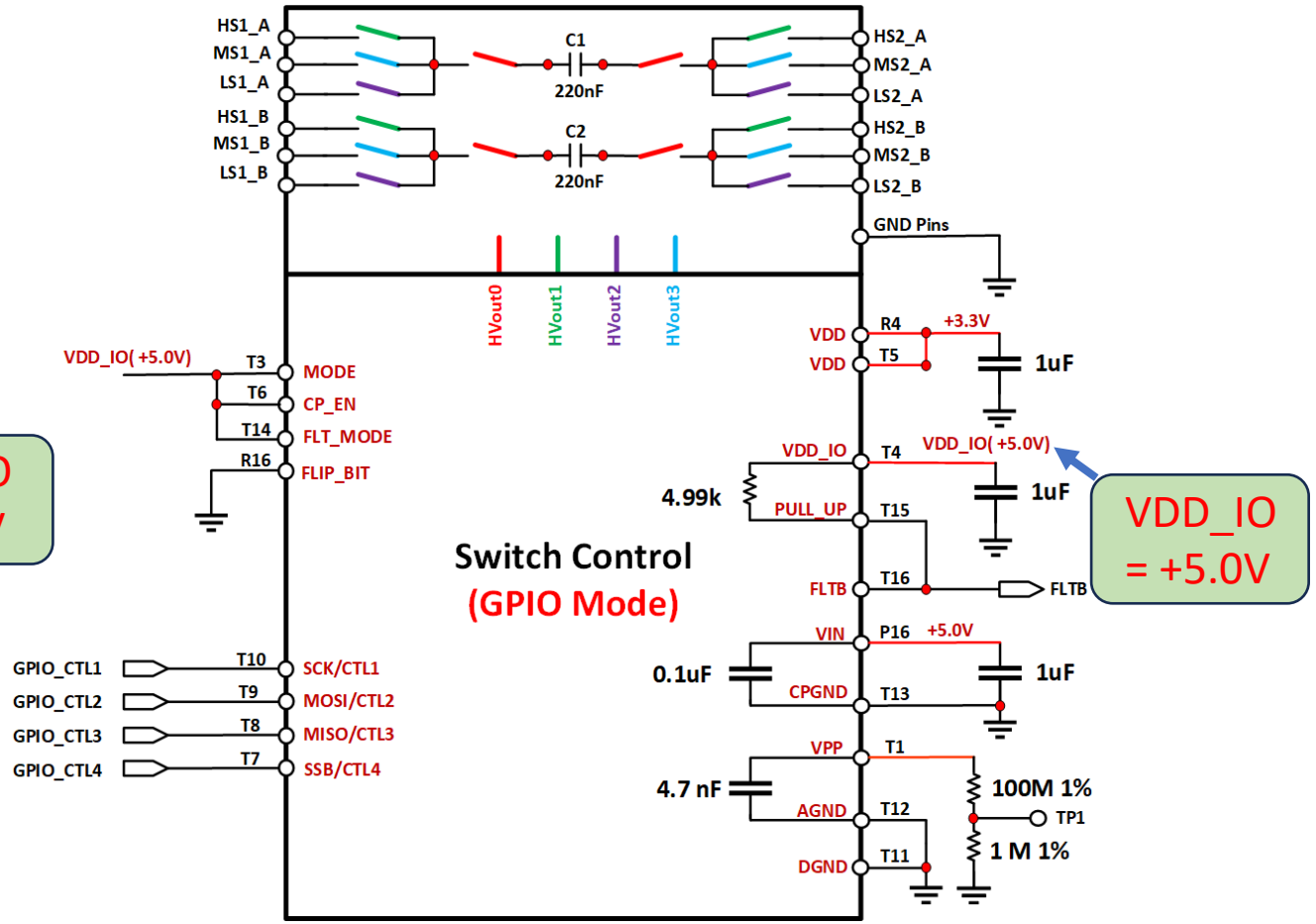
- Enable the SPI Mode:
  - MODE: Connect to GND
- Enable Spread Spectrum:
  - FLIP_BIT: Connect to VDD_IO
- Enable the Charge Pump
  - CP_EN pin: No connect, set the CPEN bit to 1
- Disable the Fault Mode:
  - FLT_MODE pin: No connect, Set the FLTMODE bit to 1
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CPEN bit low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor
- VPP can be probed with a high resistance load



MM5620/MM5622 – External Circuit for GPIO Mode

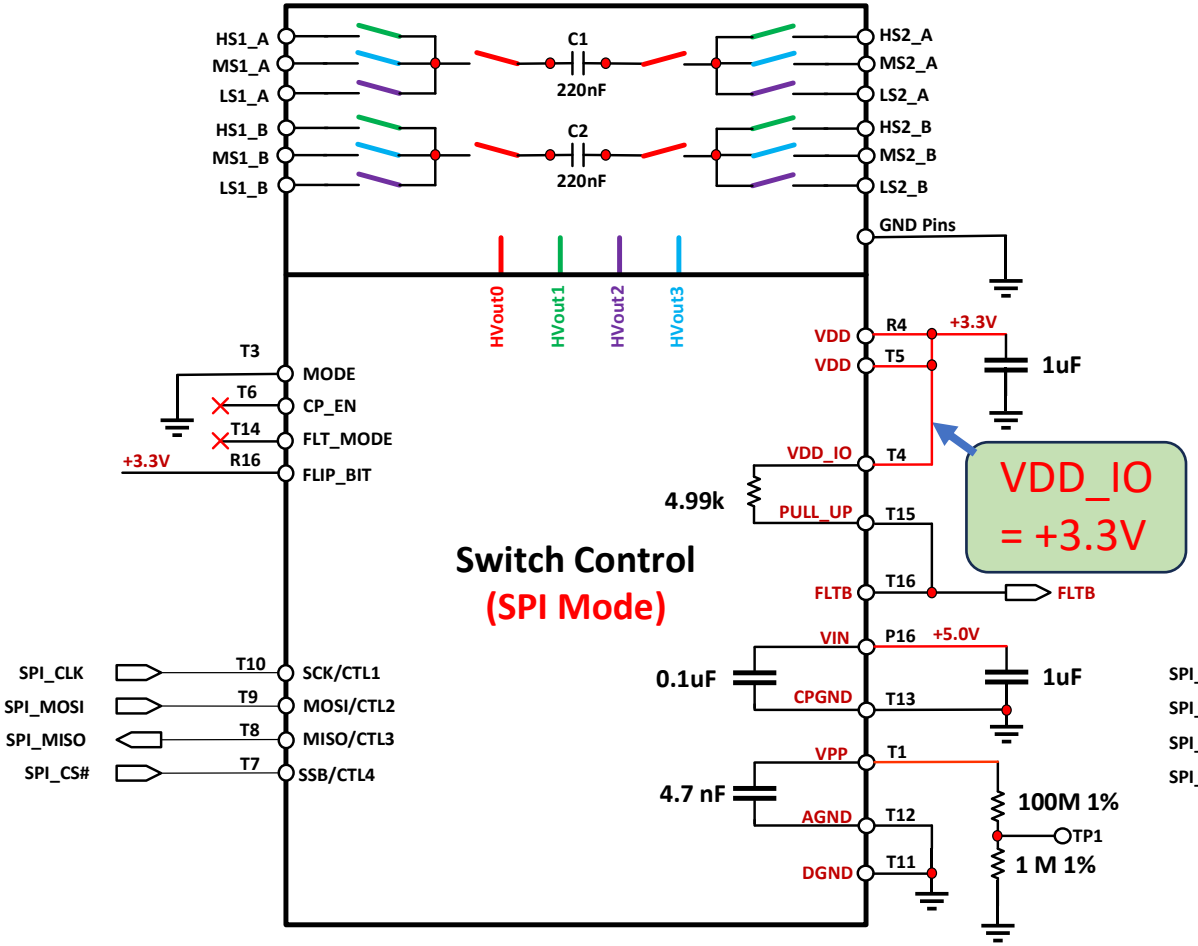
- The Charge Pump is enabled and the Fault Mode is disabled
- If resource is available, make the CP_EN input controllable - Toggling the CPEN pin to restart the charge pump when the fault event occurred

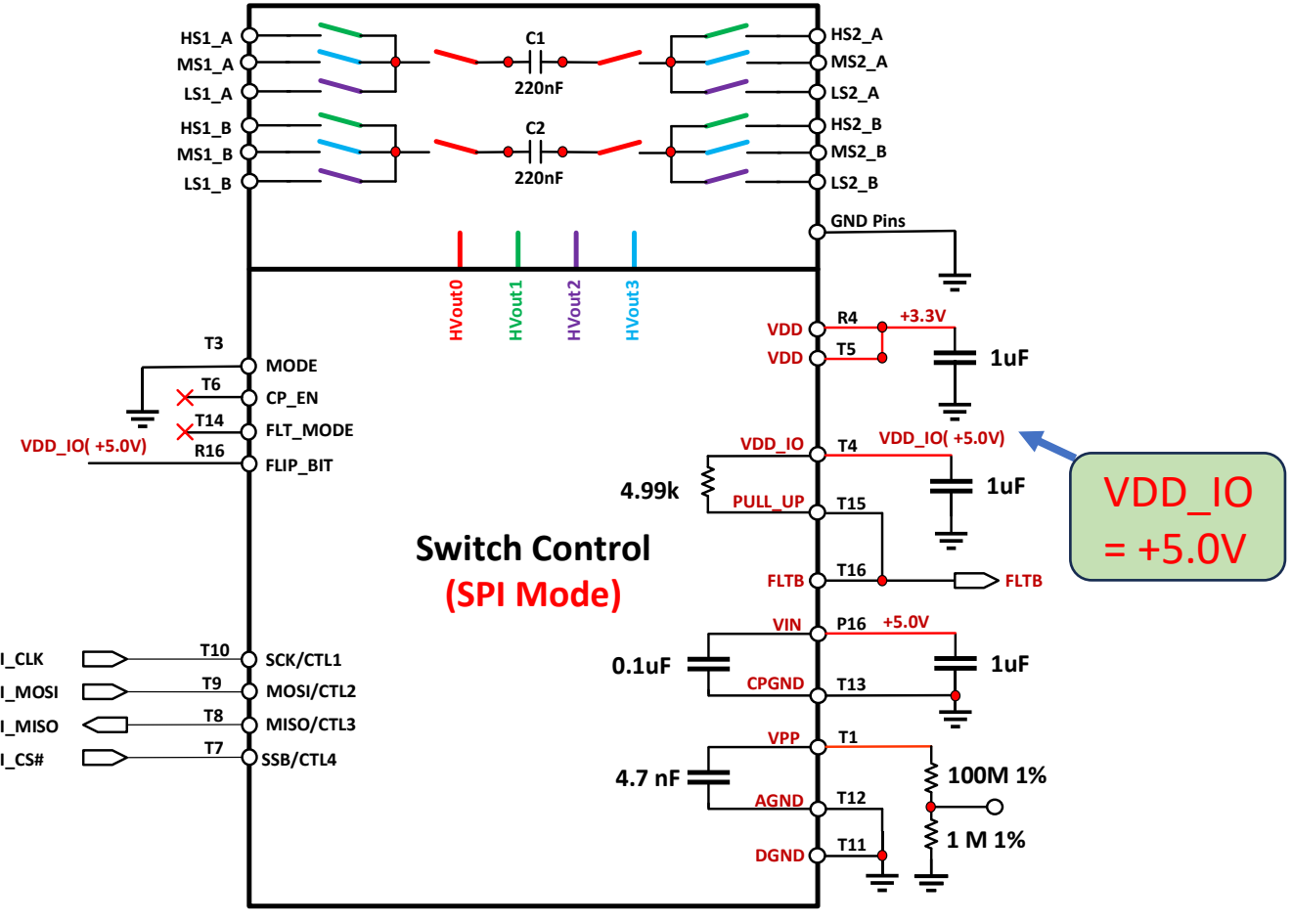




MM5620/MM5622 – External Circuit for SPI Mode

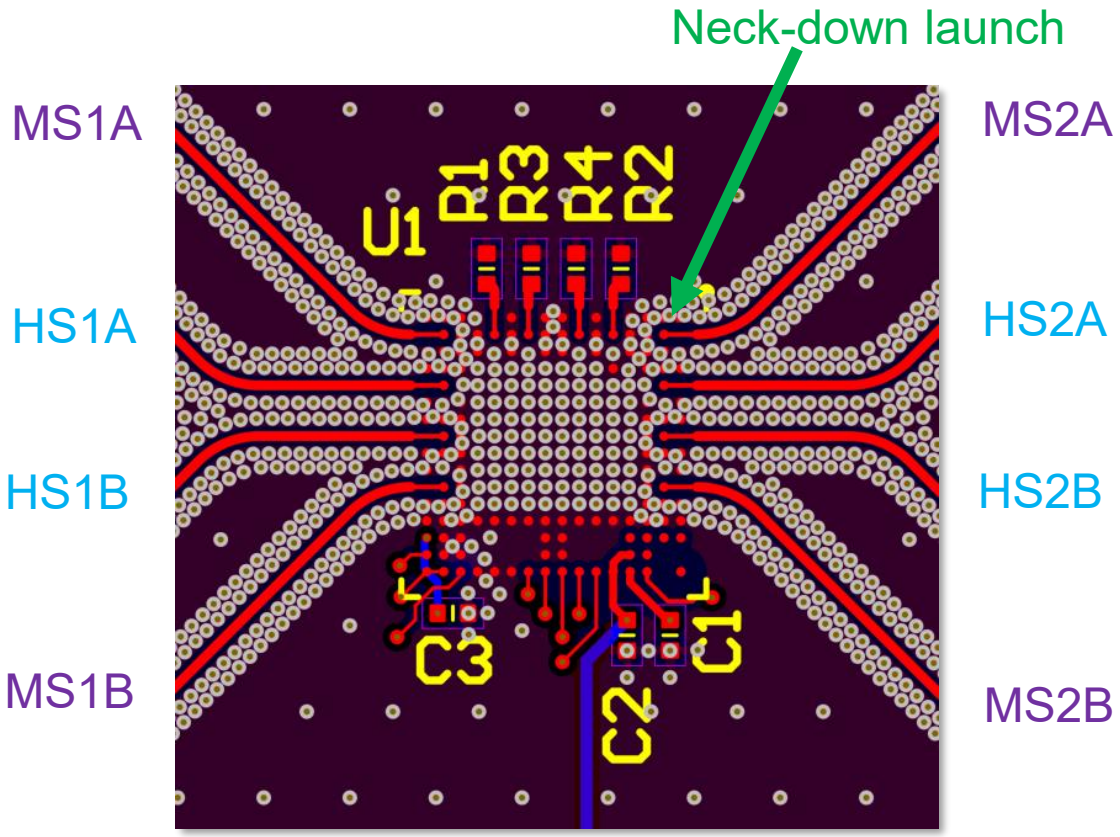
- The Charge Pump needs to be enabled by setting the CPEN bit = 1 in SPI mode
- The Fault Mode can be deactivated by setting FLT_MODE bit = 1 in SPI mode



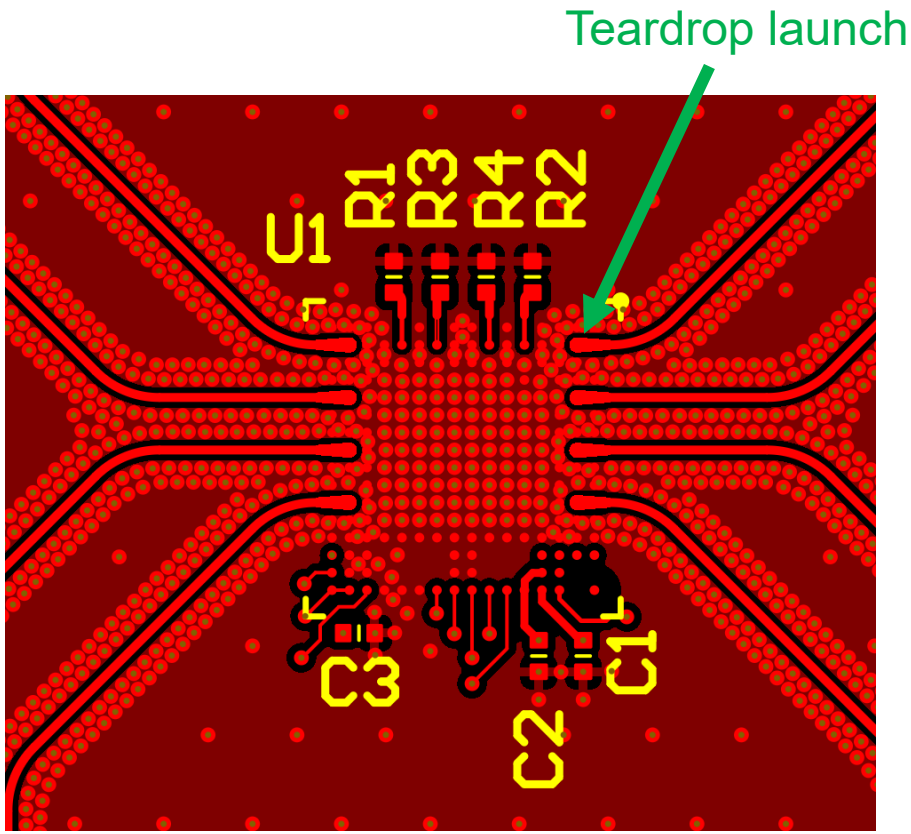


MM5620 – Customer Evaluation Board Rev4.0

- EVK performance is improved with optimized PCB launch
- Return loss is better than -18dB across frequencies up to 16GHz



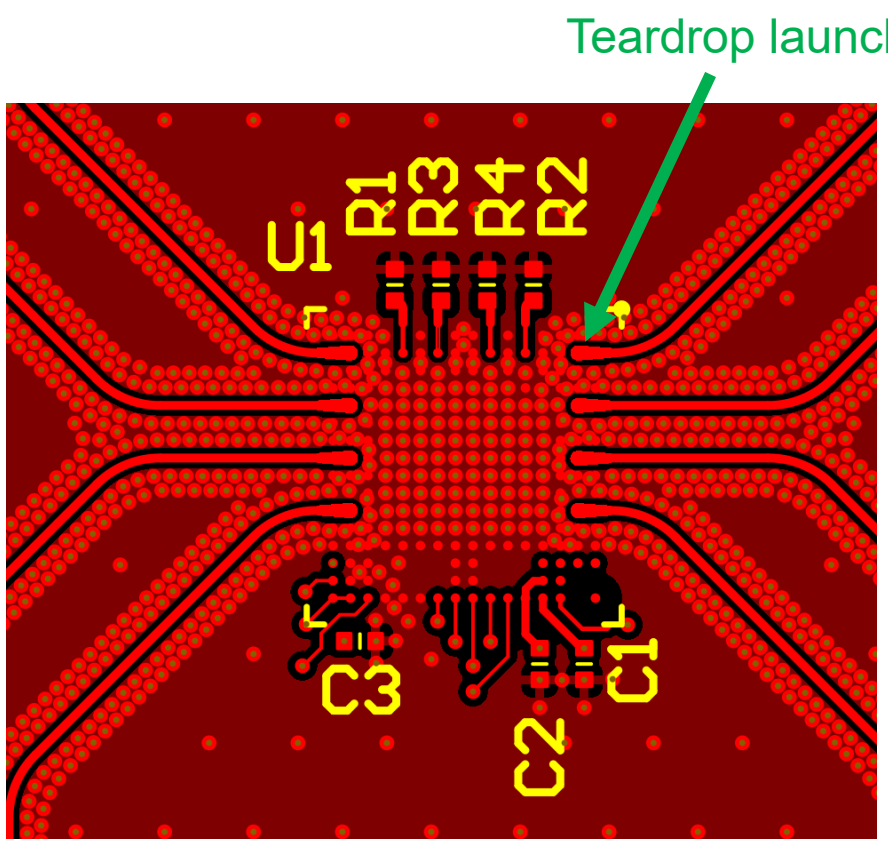
MM5620 EVK R1.0



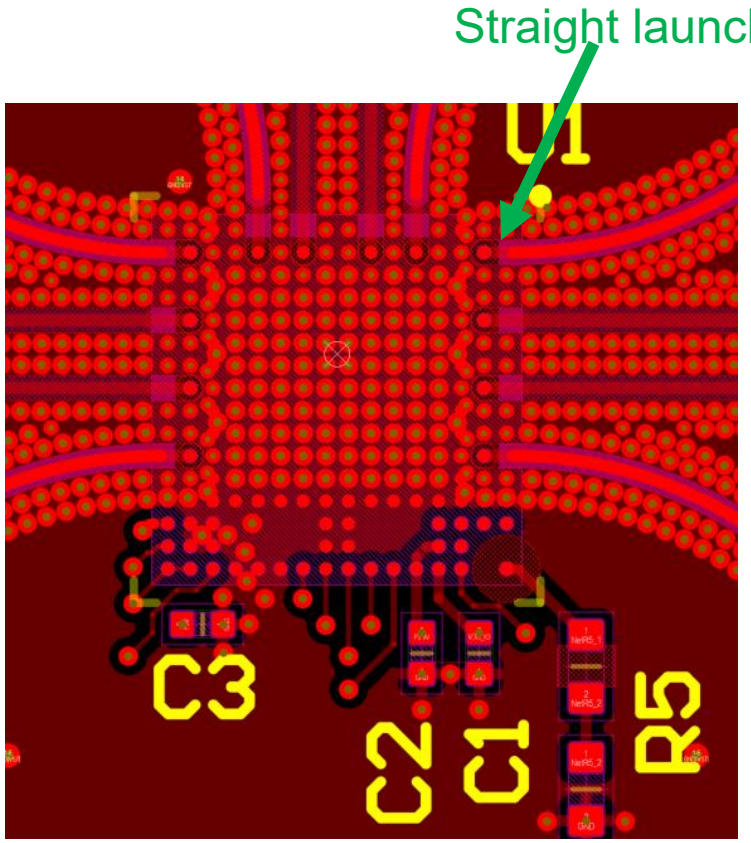
MM5620 EVK R4.0

MM5622-01NBX – Customer Evaluation Board

- EVK performance is improved with optimized PCB launch



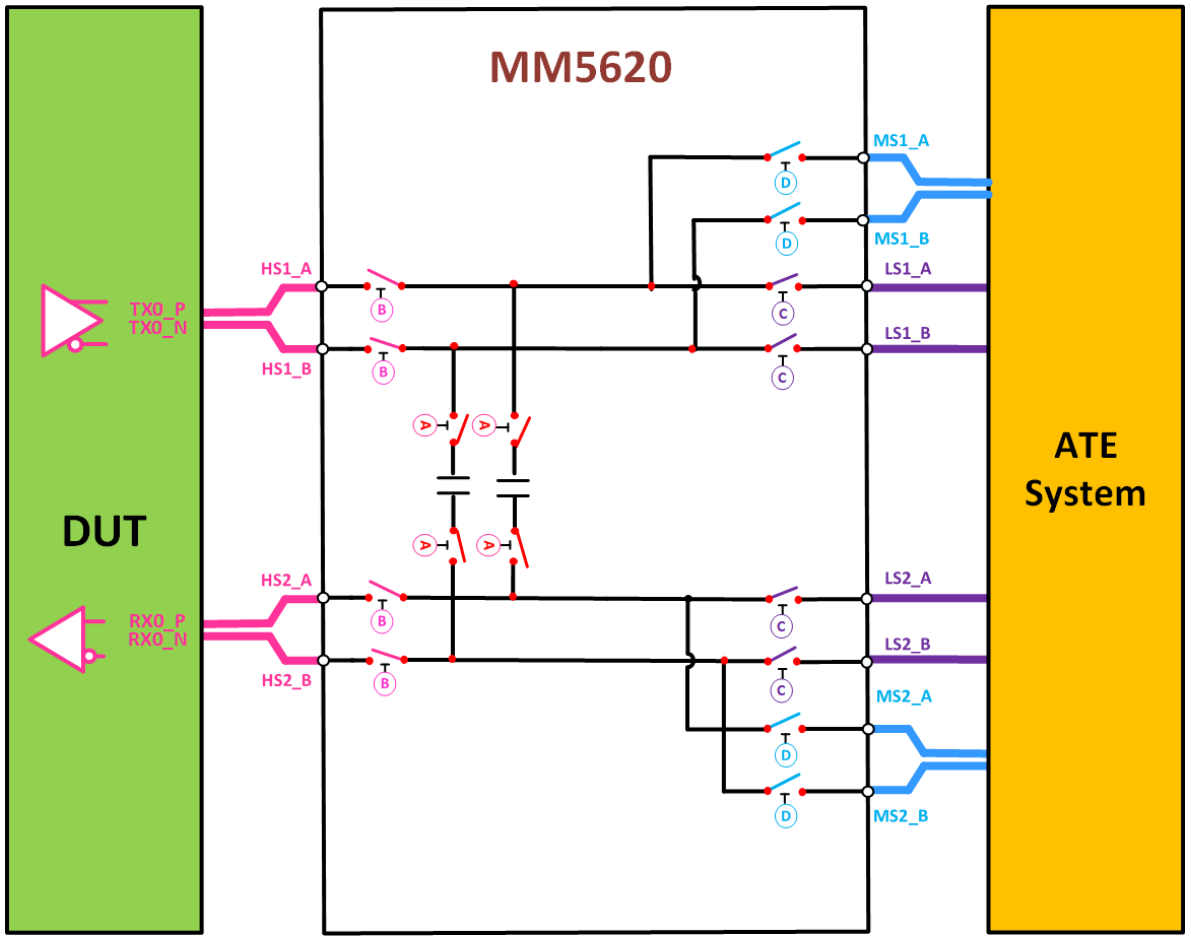
MM5620 EVK1 R4.0



MM5622-01NBX?MM5625 EVK

Application Use Cases – PCIe G5/G6 Loopback Test

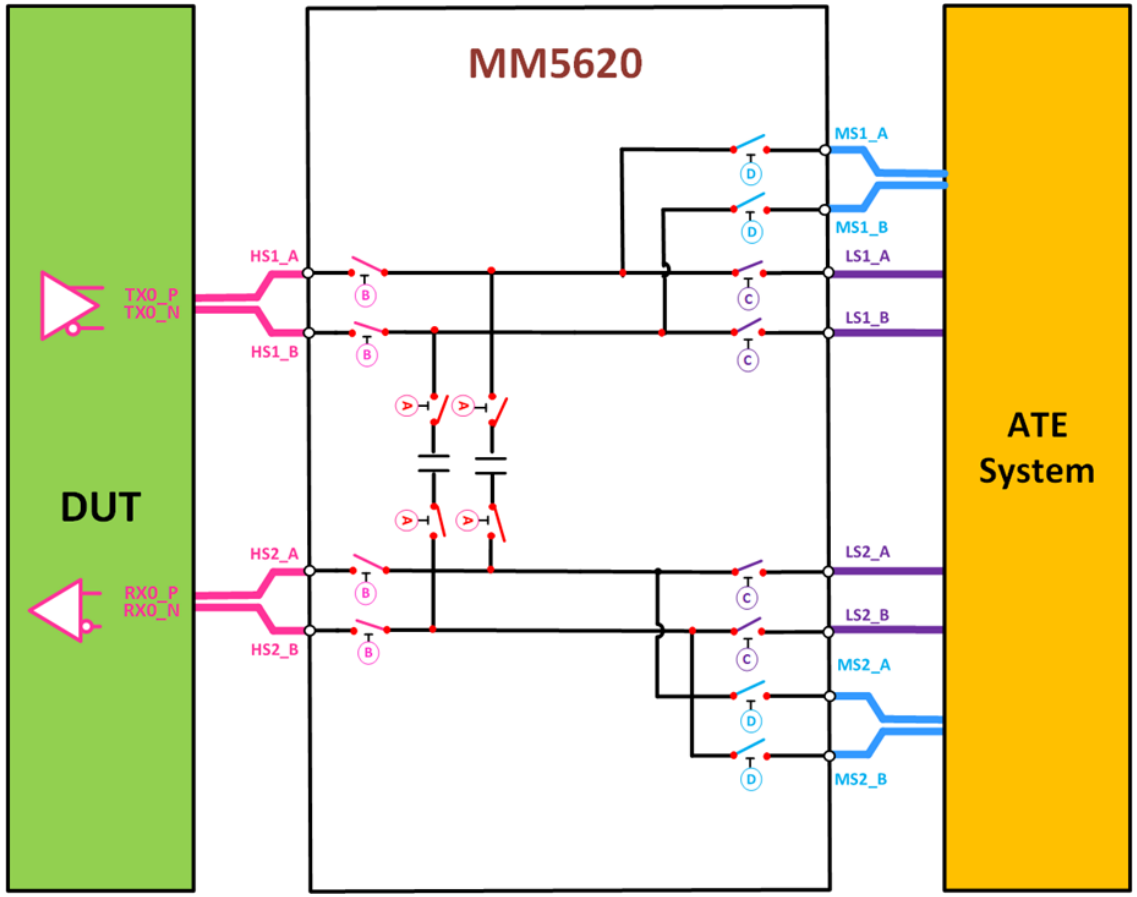
Graphics Processor Unit - Final package chipset test, Device Interface Board



Test Mode	HVA LB	HVB HS	HVC LS	HVD MS
PCIe G6 LB	ON	ON	OFF	OFF
Scan test	OFF	ON	OFF	ON
DC/Low freq test	OFF	ON	ON	OFF
All OFF	OFF	OFF	OFF	OFF

Application Use Cases – PCIe G5/CXL3.0 (Compute Express Link)

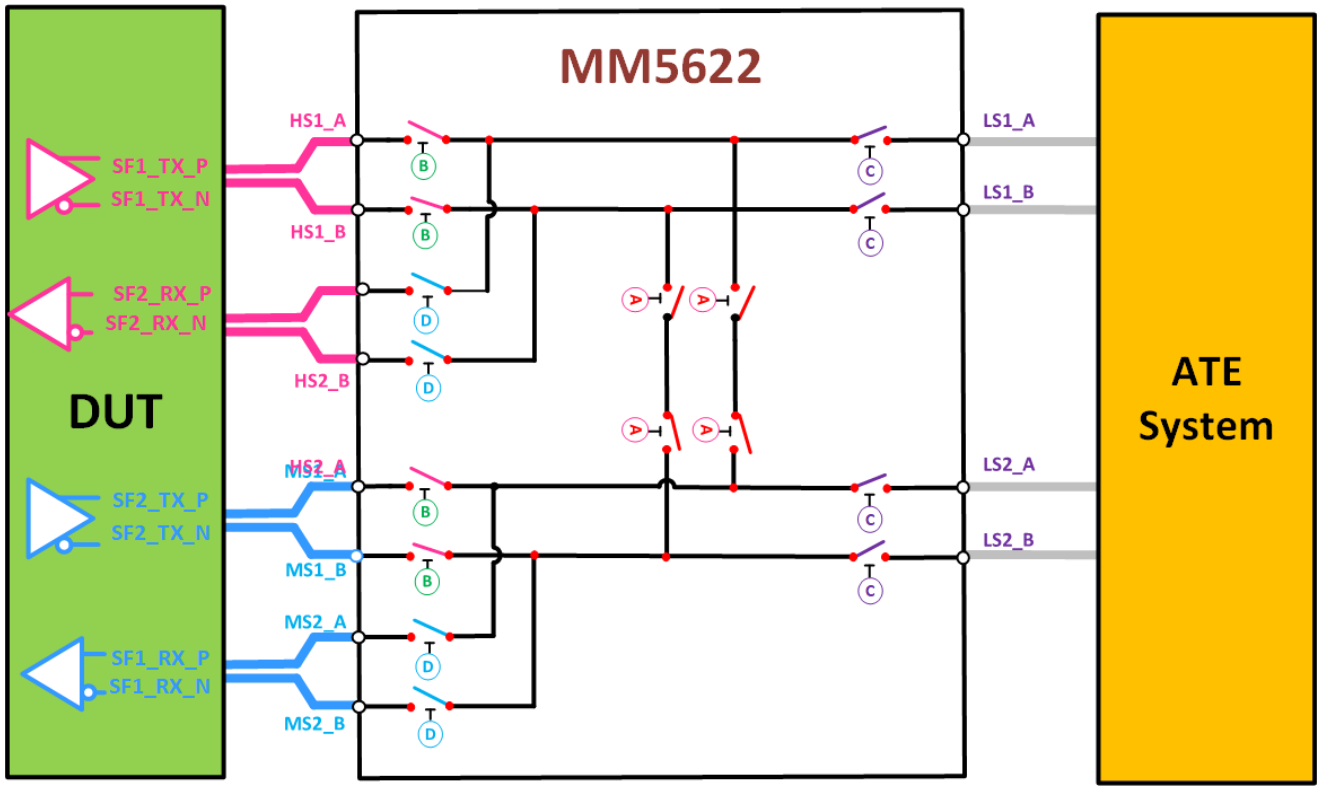
Application Processor- Final package chipset test, Device Interface Board



Test Mode	HVA LB	HVB HS	HVC LS	HVD MS
PCIe G5/CXL3 LB	ON	ON	OFF	OFF
PCI G3/4 LB	ON	OFF	OFF	ON
DC/Low freq test	OFF	ON	ON	OFF
All OFF	OFF	OFF	OFF	OFF

Application Use Cases – Fiber Optics, Two SFP test

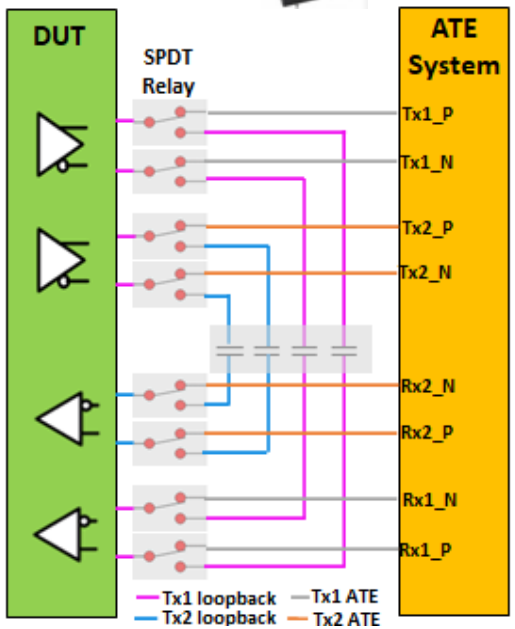
Two SFP Modules (25 Gbps, 12.5GHz) tested simultaneously, with Dual I/O mode



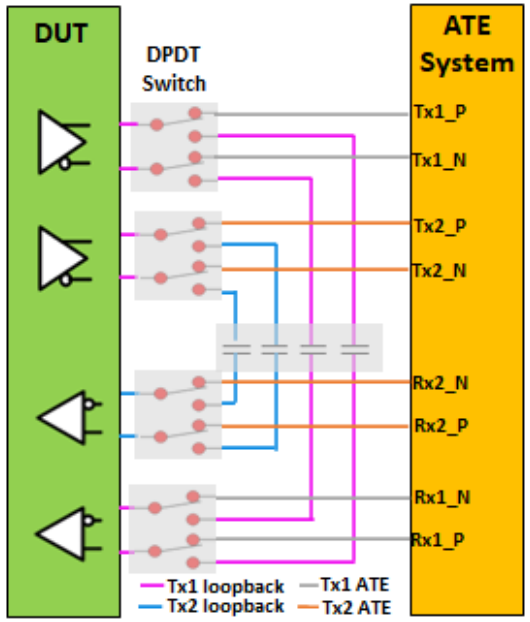
Test Mode	HVA LB	HVB HS	HVC LS	HVD MS
SF1/2 Loopback	OFF	ON	OFF	ON
All OFF	OFF	OFF	OFF	OFF

MM5620 – Application Benefits for Automated SoC Testing

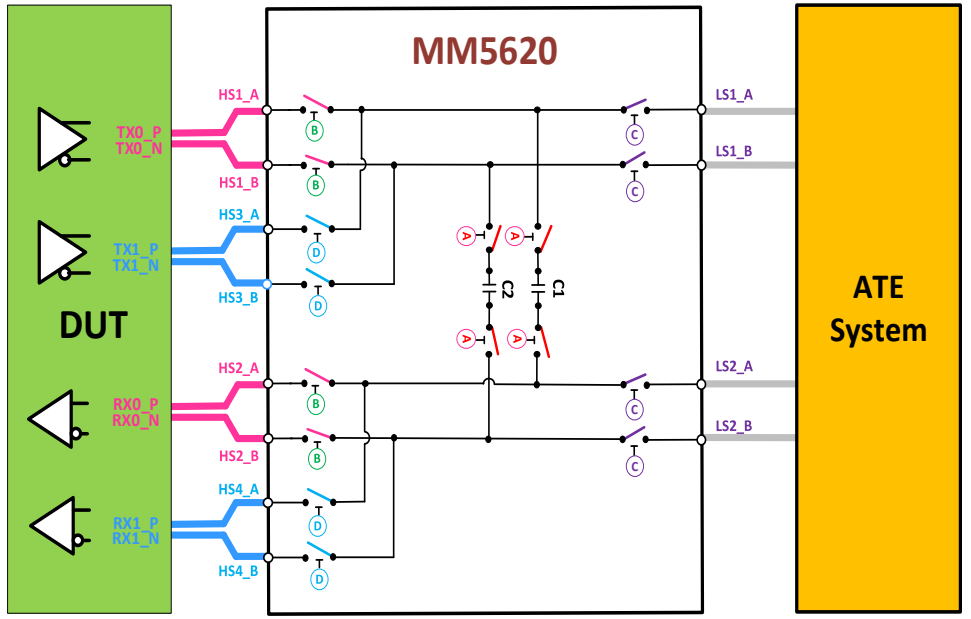
SPDT Relay



DPDT Switch

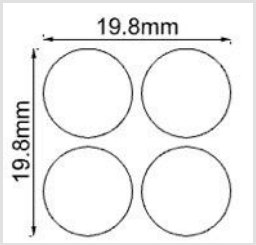
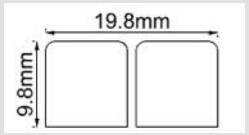
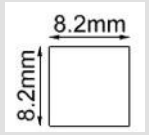
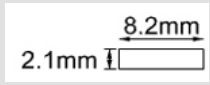


Menlo MM5620



Metrics	Parameters	SPDT Relay	DPDT Switch	Menlo MM5620
Performance	Loopback Channel Data Rate:	★★★★ 64 Gbps (PAM4)	★★ 36 Gbps (est: 2x BW)	★★★★ 64 Gbps (PAM4)
	ATE Test Channel Frequency Range:	★★ DC to 18 GHz ★	★★ DC to 18 GHz ★	★★★ DC to 20 GHz ★★★★
Versatility	Transmitters Sharing a Receiver:	★★★ No (need ext switches)	★ No (need ext switches)	★★★★ Yes
	Loopback-ATE Channel Isolation:	★ 32 dB (18 GHz)	★★ 16 dB (6 GHz)	★★★★ 50 dB (18 GHz)
Board Density	BOM Count:	★ 8x relays, 4x caps	★★ 4x switches, 4x caps	★★★★ 1x MM5620
	Footprint:	Large	Two 5mm x 4mm	One 8.2mm x 8.2mm

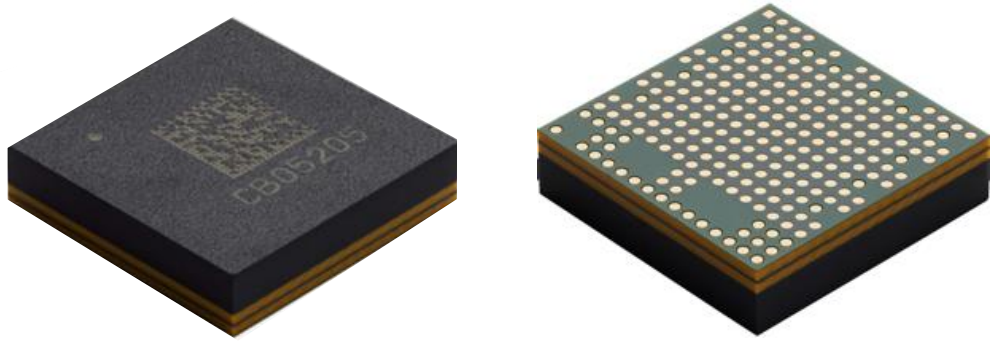
97% Reduction in volume compared to RF relays

	Typical RF EMR	MM5620/22	Key Menlo Benefits
Size/Ch. Density:	 **9.4 mm (d) x 9.8 mm (h)** 4 qty x RF EMR: 432.6 mm^2 TOP VIEW  SIDE VIEW  **Area: 432.6 mm^2** **Volume: 4239.8 mm^3**	 MM5620 **8.2 mm x 8.2 mm x 2.1 mm LGA** 1qty x MM5620/22: 67.2 mm^2 TOP VIEW  SIDE VIEW  **Area: 67.2 mm²** **Volume: 141.2 mm³**	**<u>85% board area reduction</u>** **<u>97% volume reduction</u>** enables more parallel test, more test coverage, easier routing, Top or bottom placement
Configuration:	1x DPDT, DC-6GHz	2x DP3T, DC-20 GHz (64 Gbps)	Simplifies routing; Dual DP3T with built-in loopback capacitor
Power Consumption:	200mW	10mW	**<u>99% reduction in power consumption</u>**
Reliability:	5M operations **<u>typical</u>**	>3B operations **<u>minimum</u>**	**<u>1000x increase in lifetime</u>**: reduced down-time, maintenance & cost
Switching speed:	6ms operation time	<30 us	**<u>1000x speed increase</u>** reduced test time & cost-of-test

menlomicro

MM5625

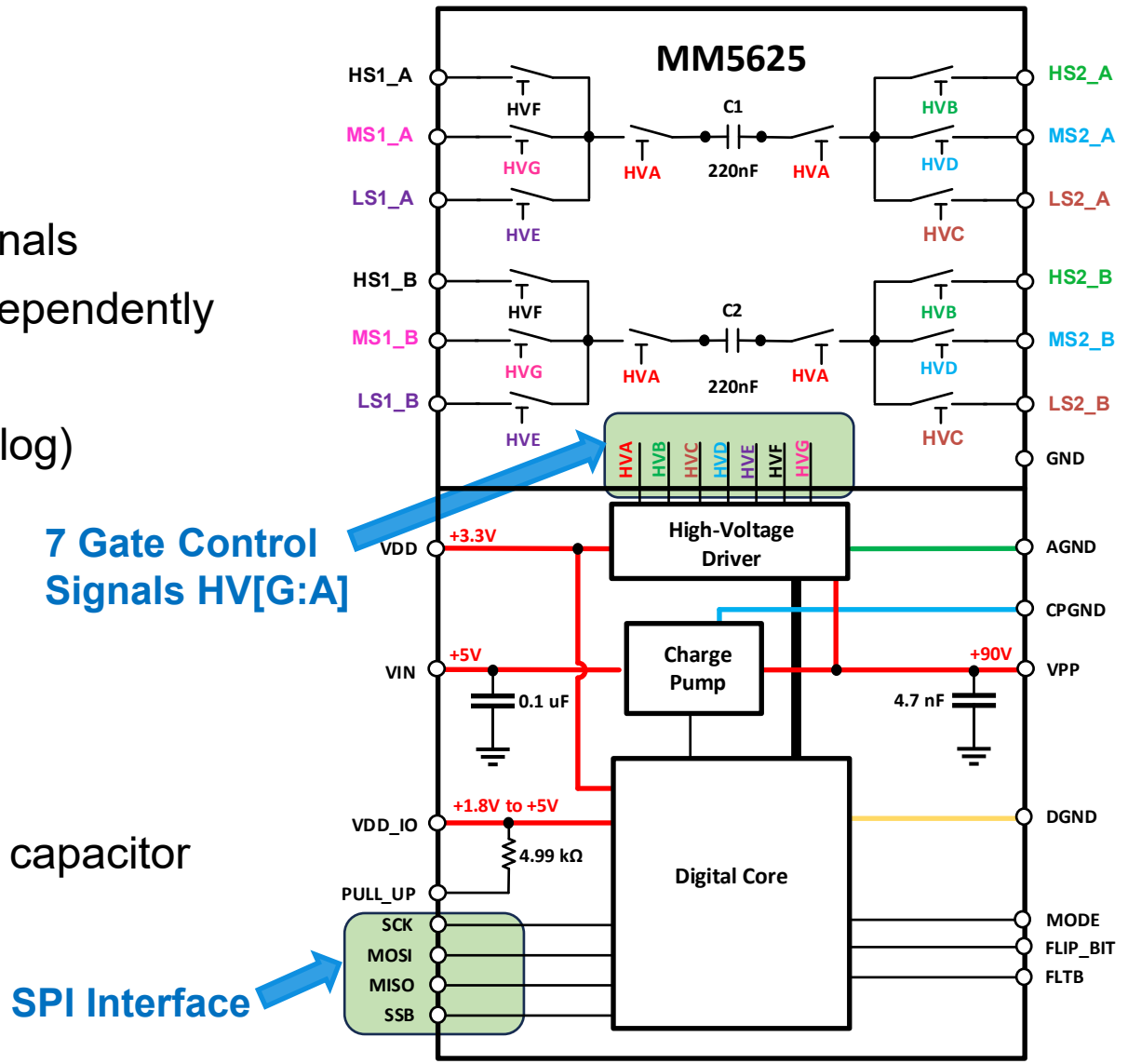
- 80 Gbps High-Speed Differential Loopback Switch (AC coupled)



MM5625 – Product Highlights

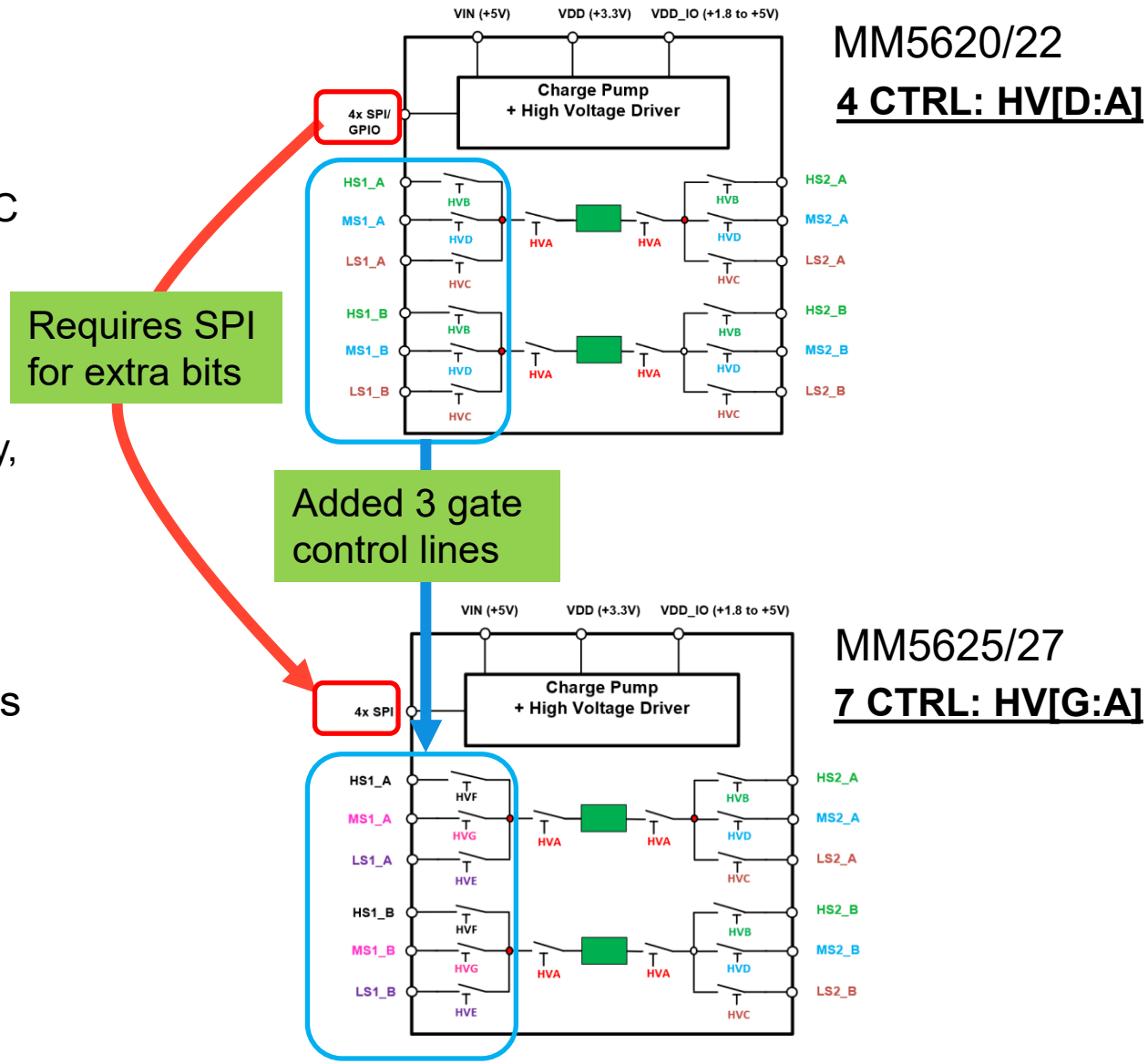
- DC to 20 GHz range
- Improved RF performance from MM5620
- Support 128 control states – 7 gate control signals
  - Each differential pair can be controlled independently
- Integrated charge pump & high-voltage driver
- Power supply 5 V (voltage booster) 3.3 V (analog)
- SPI control interface only
- Built-in passive components
  - DC blocking capacitors
  - Internal VPP capacitor
  - Internal 4.99k pullup resistor
  - Internal 0.1uF/10V VIN to CPGND bypass capacitor
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA

[Menlo MM5625_Datasheet (menlomicro.com)]



Why MM5625 & MM5627?

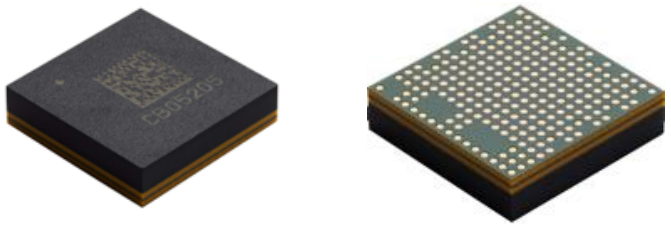
- Customer Requirement/Use case:
  - TX diff signals need to be routed to RX diff signals
  - Need to access all TX & RX pins through LS paths for DC Today, need to use cascaded/multiple MM562x devices
- Solution:
  - Add additional three gate control lines, total 7
  - With this, we can control each differential pair individually, with a single device
- MM5627 supports DC-coupled Signal Paths only
- MM5625/27 will support much more flexible use cases
- Footprint compatible with MM5620/MM5622
- MM5625 in production since June -2025

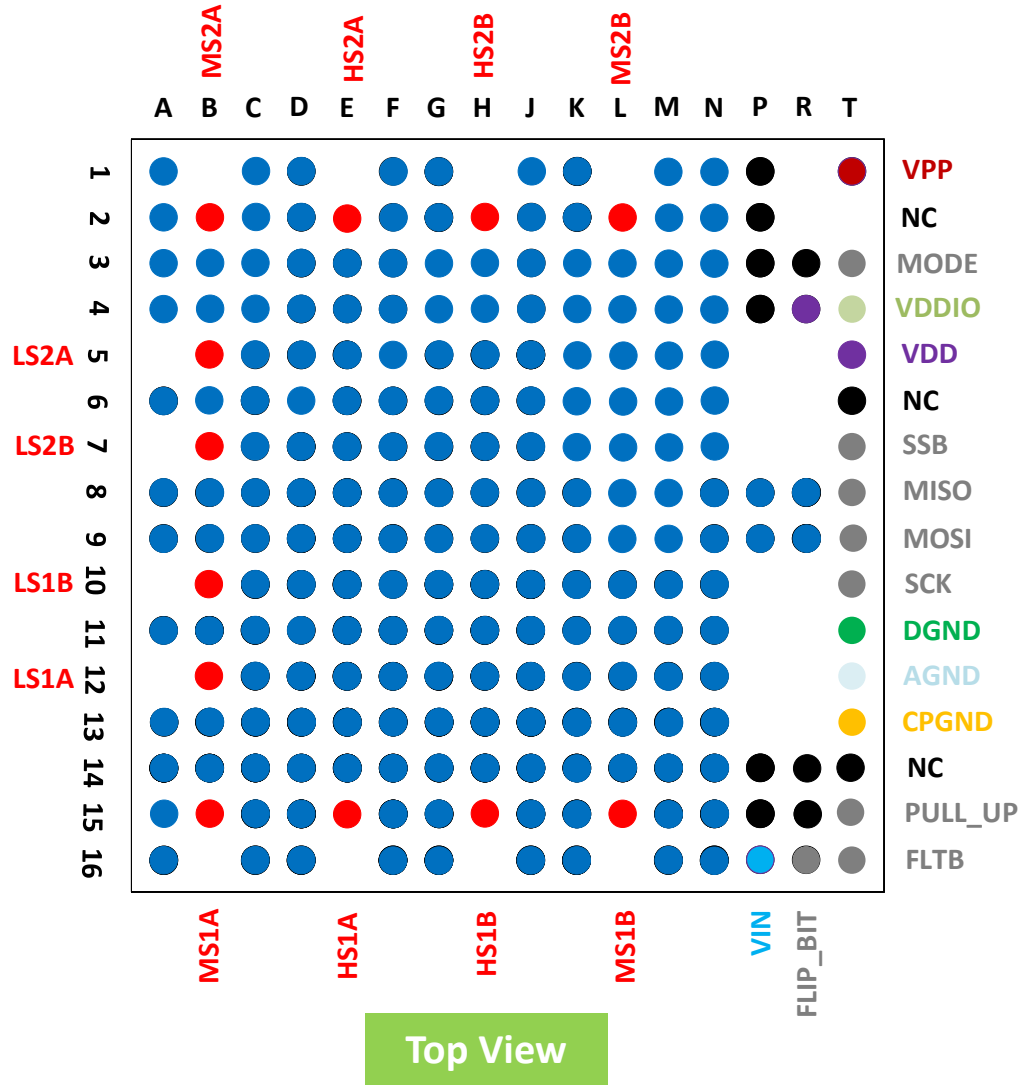


MM5625 - LGA 16x16 Footprint Diagram

Key Features

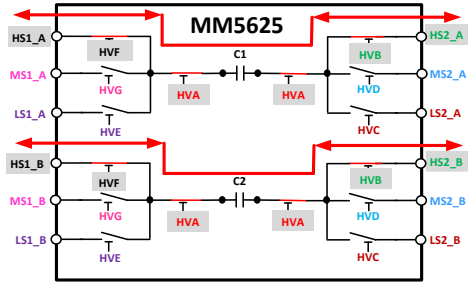
- Size: 8.2 x 8.2 mm^2
- 16x16 LGA array
- 0.5 mm pitch / 0.3mm pad diameter
- Internal VPP capacitor
- Internal 4.9k pullup resistor
- Internal 0.1uF/10V VIN/CPGND cap



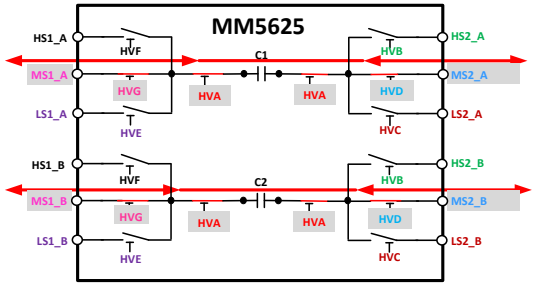


MM5625 – Major Differential Signal Paths

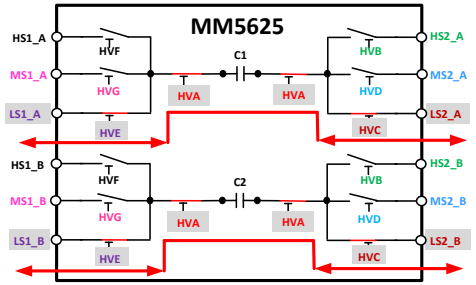
- Differential signal paths going through the AC- coupling capacitors



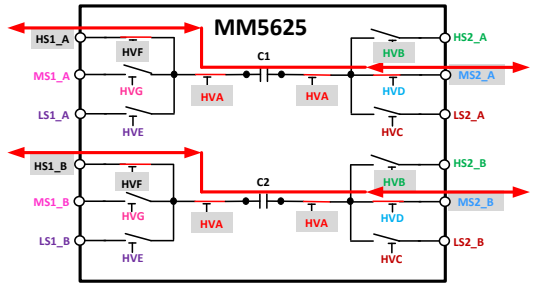
HS1 ↔ HS2



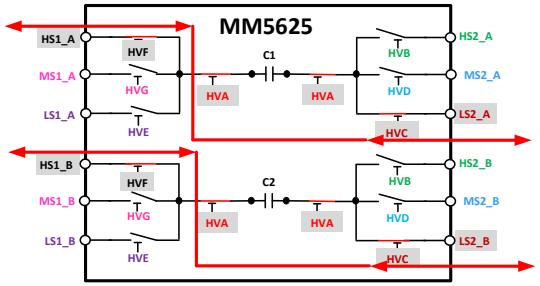
MS1 ↔ MS2



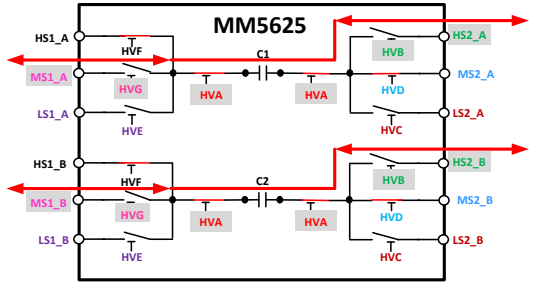
LS1 ↔ LS2



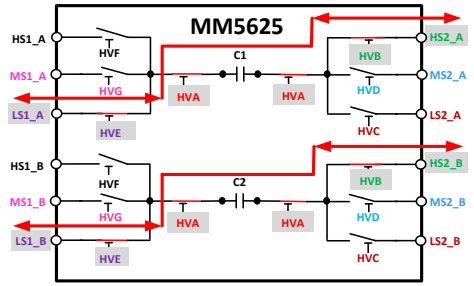
HS1 ↔ MS2



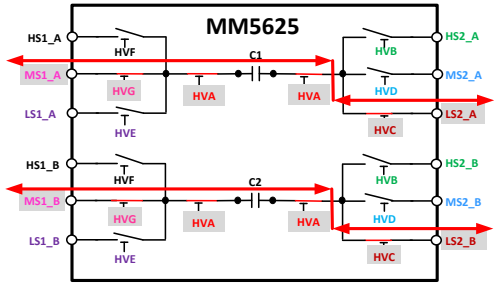
HS1 ↔ LS2



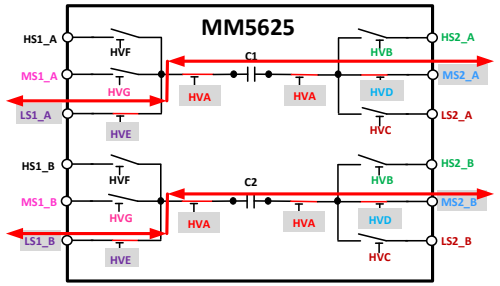
MS1 ↔ HS2



LS1 ↔ HS2



MS1 ↔ LS2

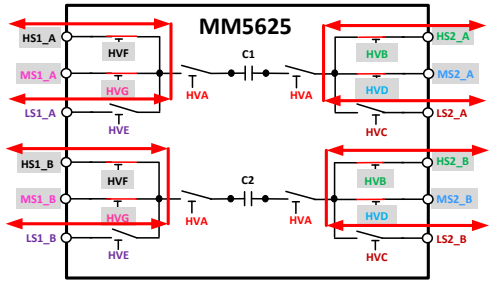


MS2 ↔ LS1

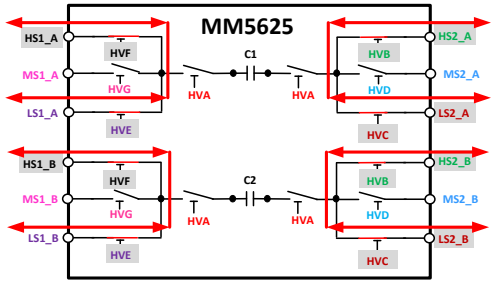
New connection schemes enabled by MM5625

MM5625 – Major Differential Signal Paths

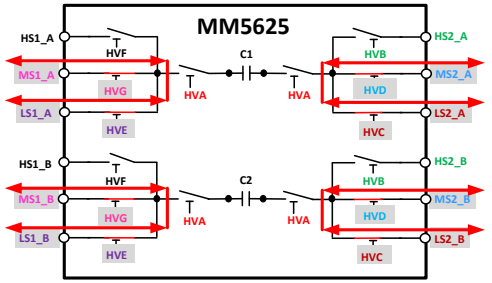
- DC-coupled differential signal paths



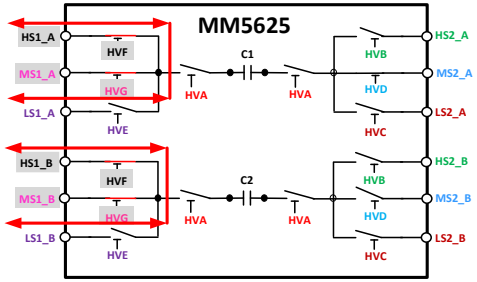
HS1 ↔ MS1
HS2 ↔ MS2



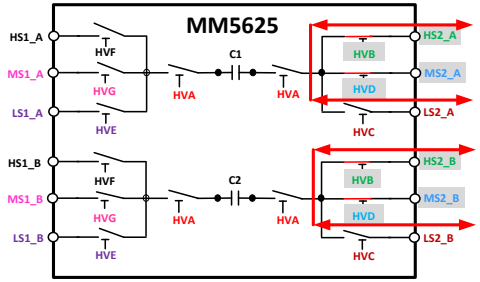
HS1 ↔ LS1
HS2 ↔ LS2



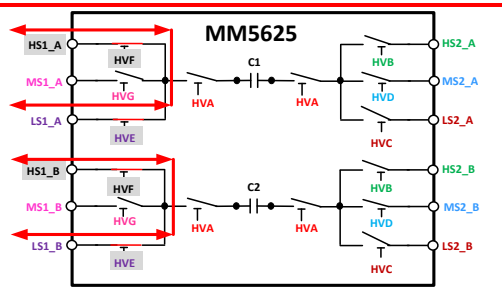
MS1 ↔ LS1
MS2 ↔ LS2



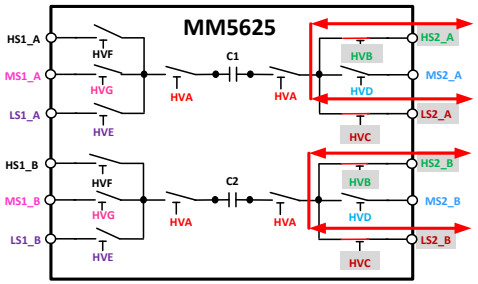
HS1 ↔ MS1



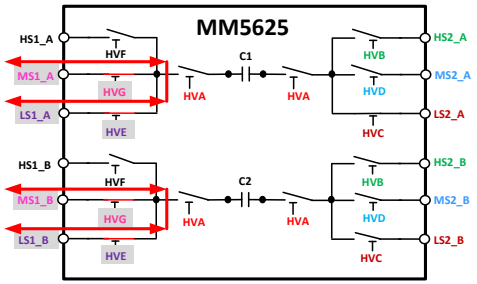
HS2 ↔ MS2



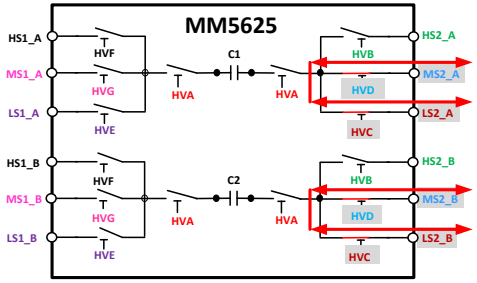
HS1 ↔ LS1



HS2 ↔ LS2



MS1 ↔ LS1

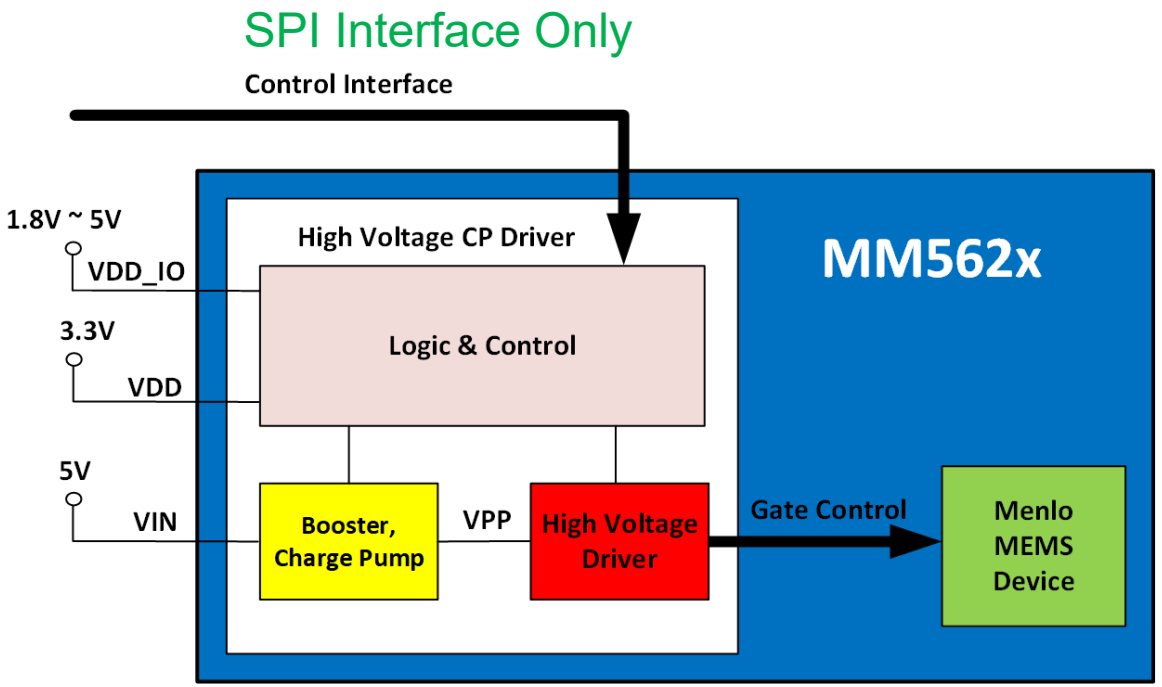


MS2 ↔ LS2

New connection schemes enabled by MM5625

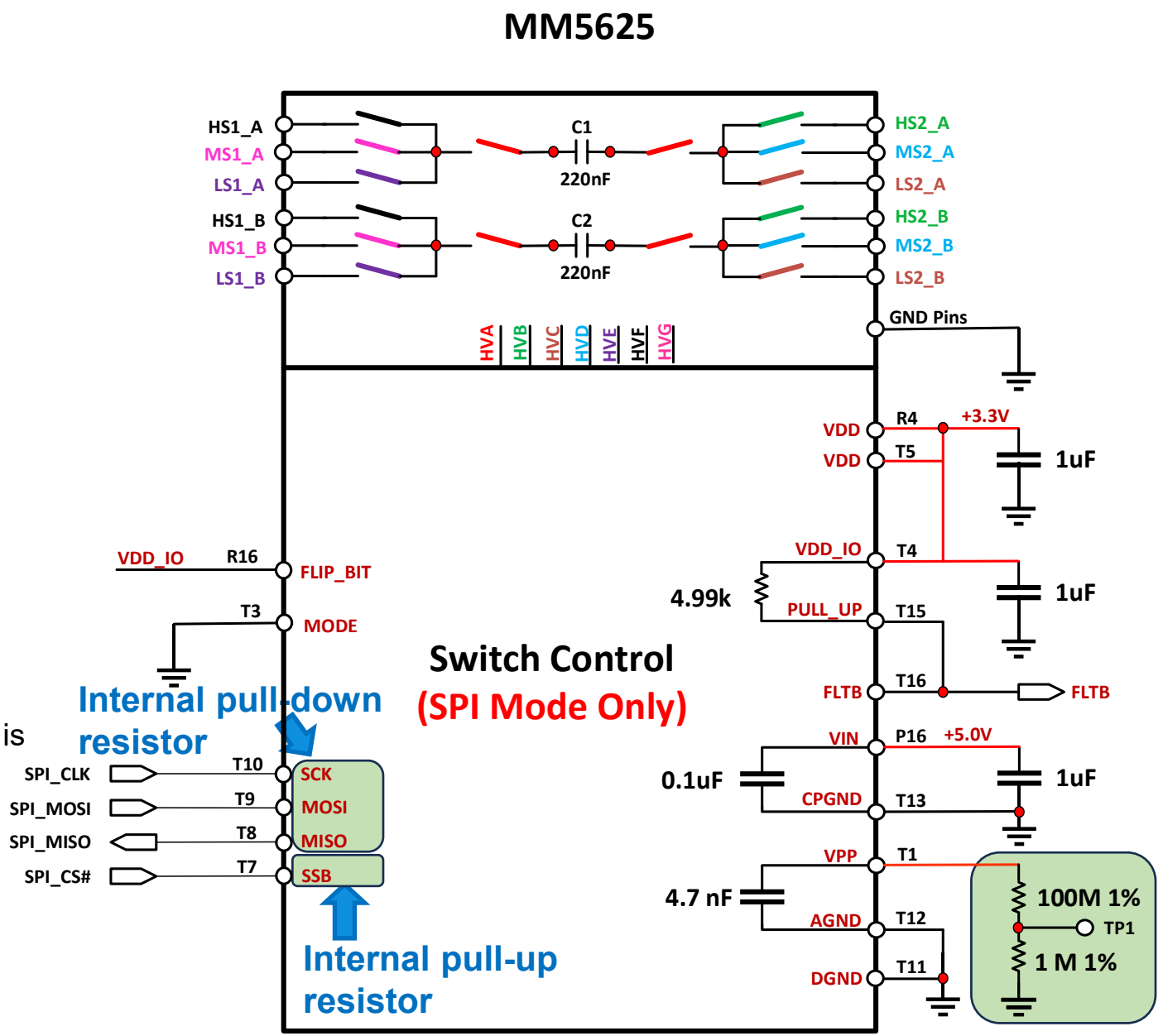
MM5625 - MEMS Switch Control Block Diagram

- The communication interface:
  - SPI Only for MM5625
- VDD_IO: Digital I/O supply (+1.8V to +5.0V)
- VDD: +3.3V supply to analog circuits
- VIN: +5V supply to the internal charge pump
- Should not need to sequence the power supplies



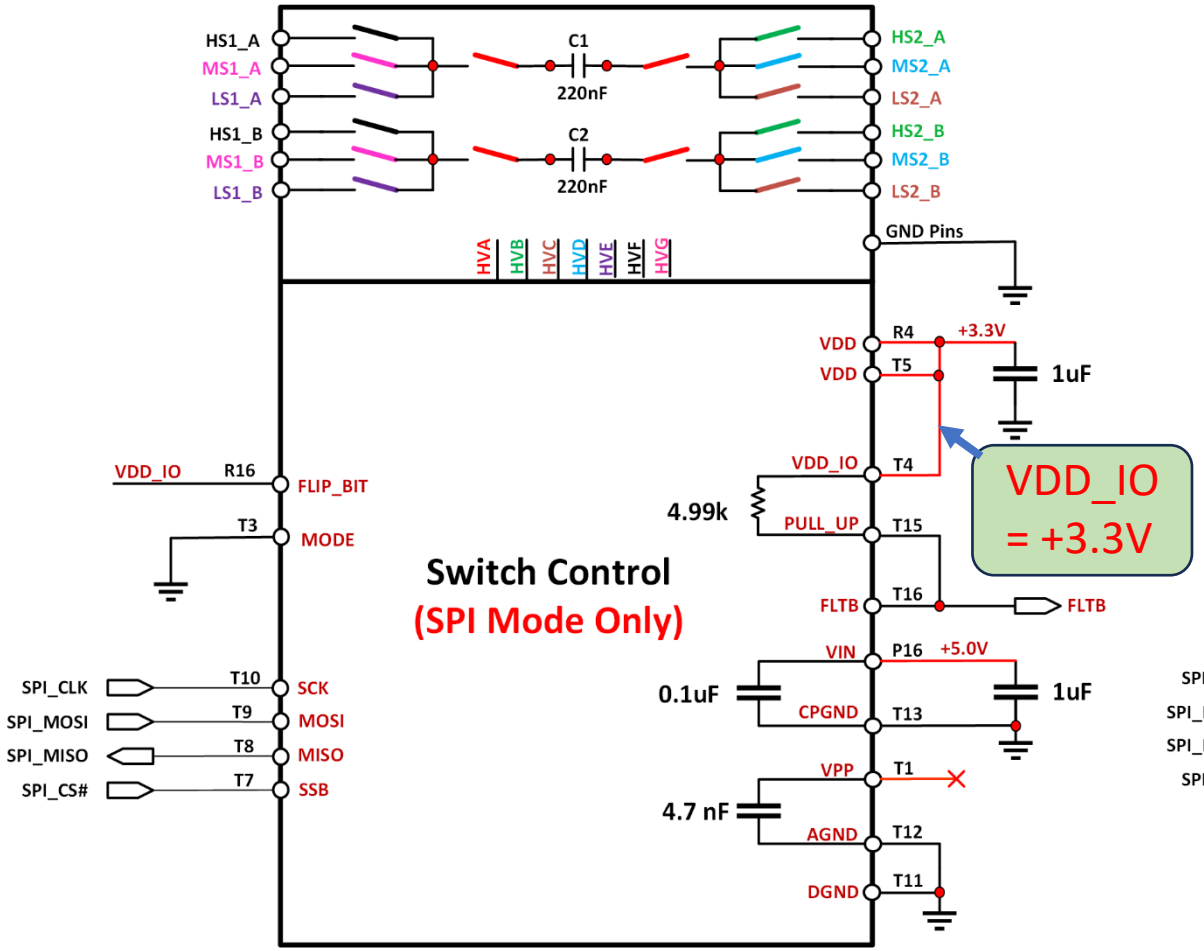
MM5625 – External Circuit

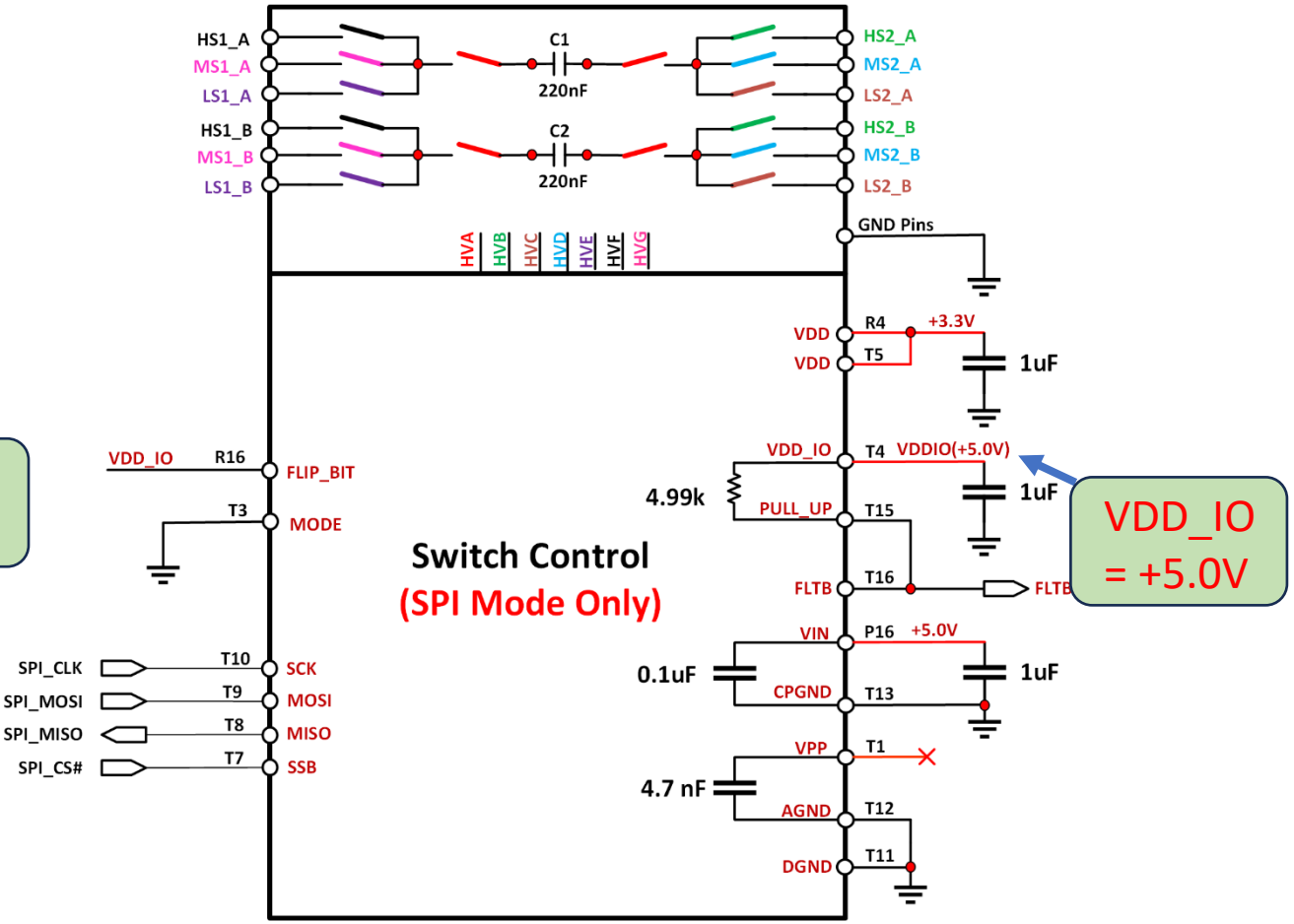
- Enable the SPI Mode:
  - MODE: Connect to GND
- Enable Spread Spectrum:
  - FLIP_BIT: Connect to VDD_IO
- Enable the Charge Pump
  - CP_EN pin: No connect, set the CPEN bit to 1
- Disable the Fault Mode:
  - FLT_MODE pin: No connect, Set the FLTMODE bit to 1
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CPEN bit low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor
- VPP can be probed with a high resistance load



MM5625 – External Circuit

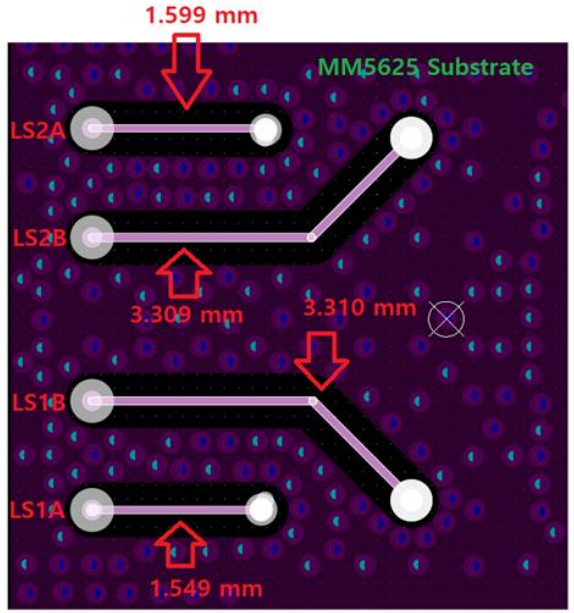
- The Charge Pump needs to be enabled by setting the CPEN bit = 1 in SPI mode
- The Fault Mode can be deactivated by setting FLT_MODE bit = 1 in SPI mode

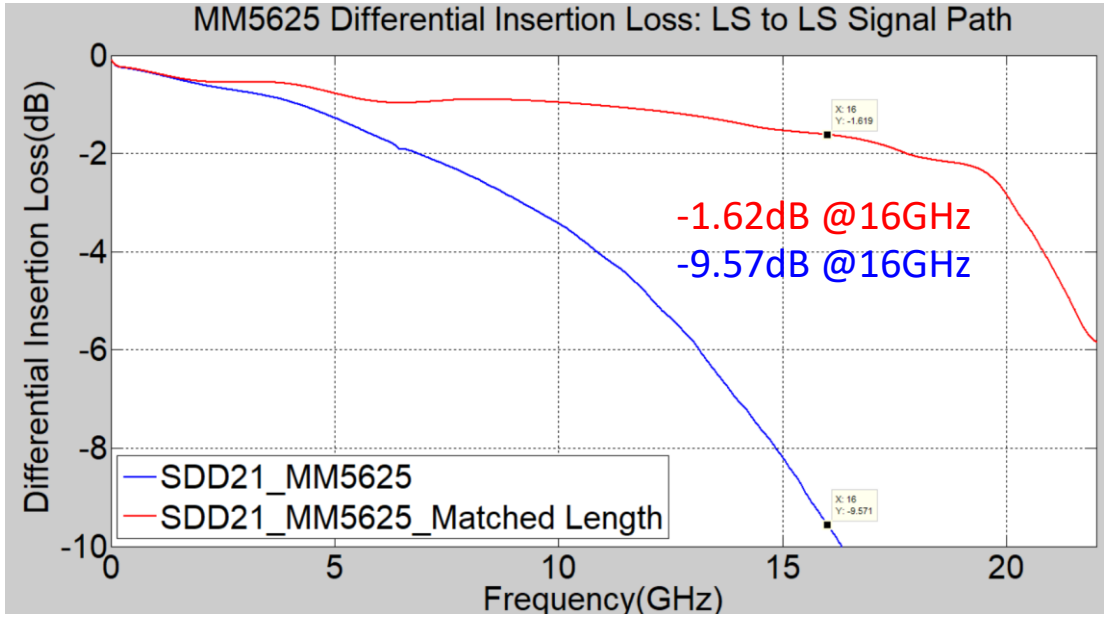


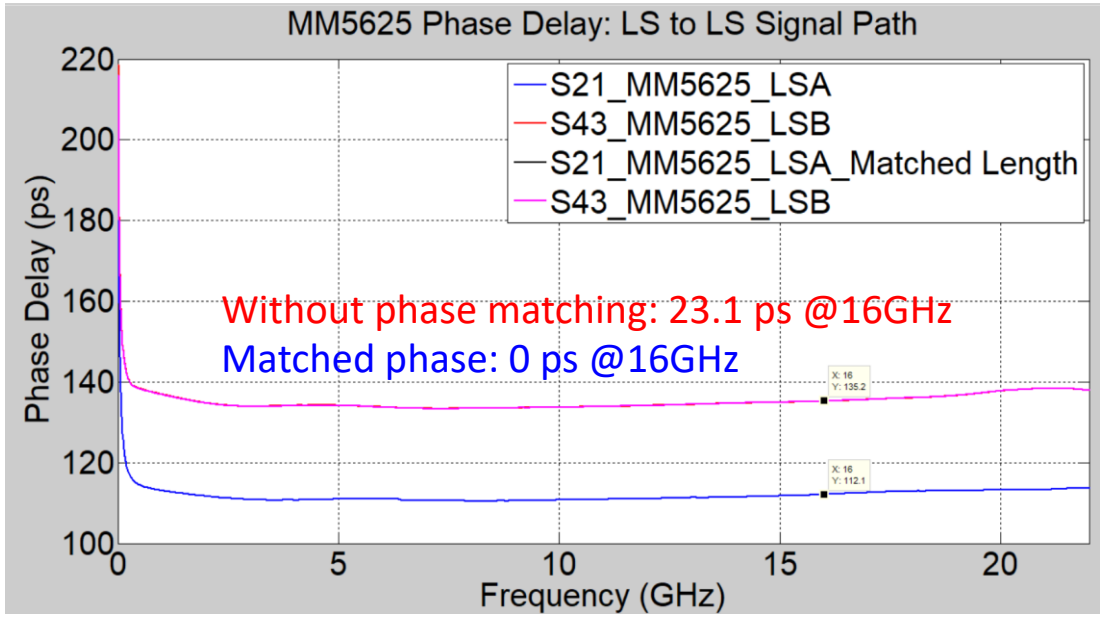


MM5625- LS Signal Path Optimization

- Trace length between LSA and LSB paths are slightly different
  - LS1A/LS2A path: 1.549mm /1.599 mm
  - LS1B/LS2B path: 3.310mm /3.309 mm
- The RF performance of the LS related signal paths can be improved by matching the phase delay between LSA and LSB externally to the MM5625
- Created a .s4p file by combining the identical S-parameter performance of the LS1B to LS2B path

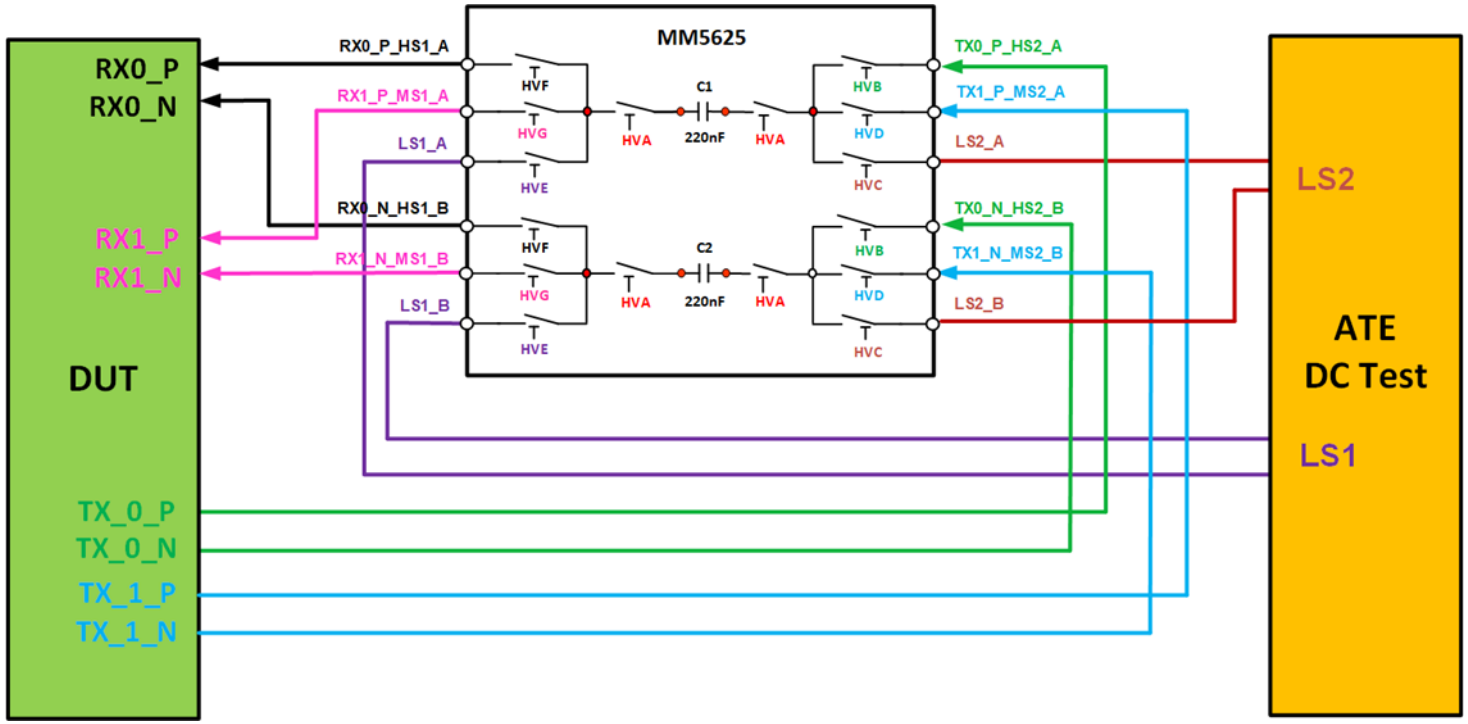






MM5625 Concept – 7 Gate Control Lines

Certain customer requirements can be met with a modified MM5620 design with additional control lines (7 vs. 4)



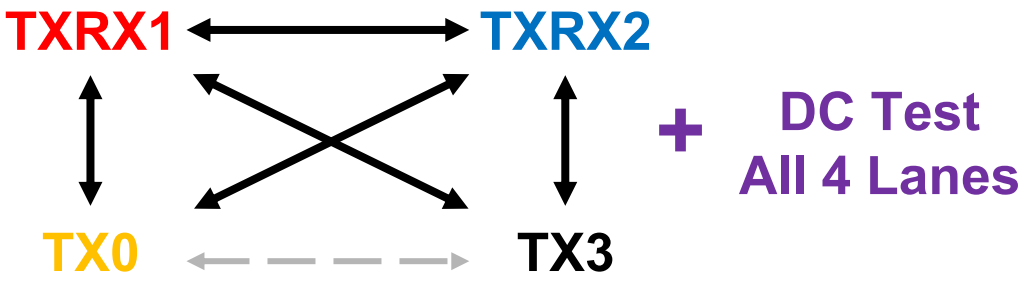
Truth table with 7 control lines

Case	Test Mode	HVG MS1	HVF HS1	HVE LS1	HVA Cap	HVB HS2	HVC LS2	HVD MS2
HS_1	HS2 to HS1(TX0 to RX0)	OFF	ON	OFF	ON	ON	OFF	OFF
HS_2	HS2 to MS1(TX0 to RX1)	ON	OFF	OFF	ON	ON	OFF	OFF
HS_3	MS2 to HS1(TX1 to RX0)	OFF	ON	OFF	ON	OFF	OFF	ON
HS_4	MS2 to MS1(TX1 to RX1)	ON	OFF	OFF	ON	OFF	OFF	ON
LS_1	HS2 to LS2(TX0 to LS2)	OFF	OFF	OFF	OFF	ON	ON	OFF
LS_2	MS2 to HS1(TX1 to LS2)	OFF	OFF	OFF	OFF	OFF	ON	ON
LS_3	HS1 to LS1 (RX0 to LS1)	OFF	ON	ON	OFF	OFF	OFF	OFF
LS_4	MS1 to LS1 (RX1 to LS1)	ON	OFF	ON	OFF	OFF	OFF	OFF

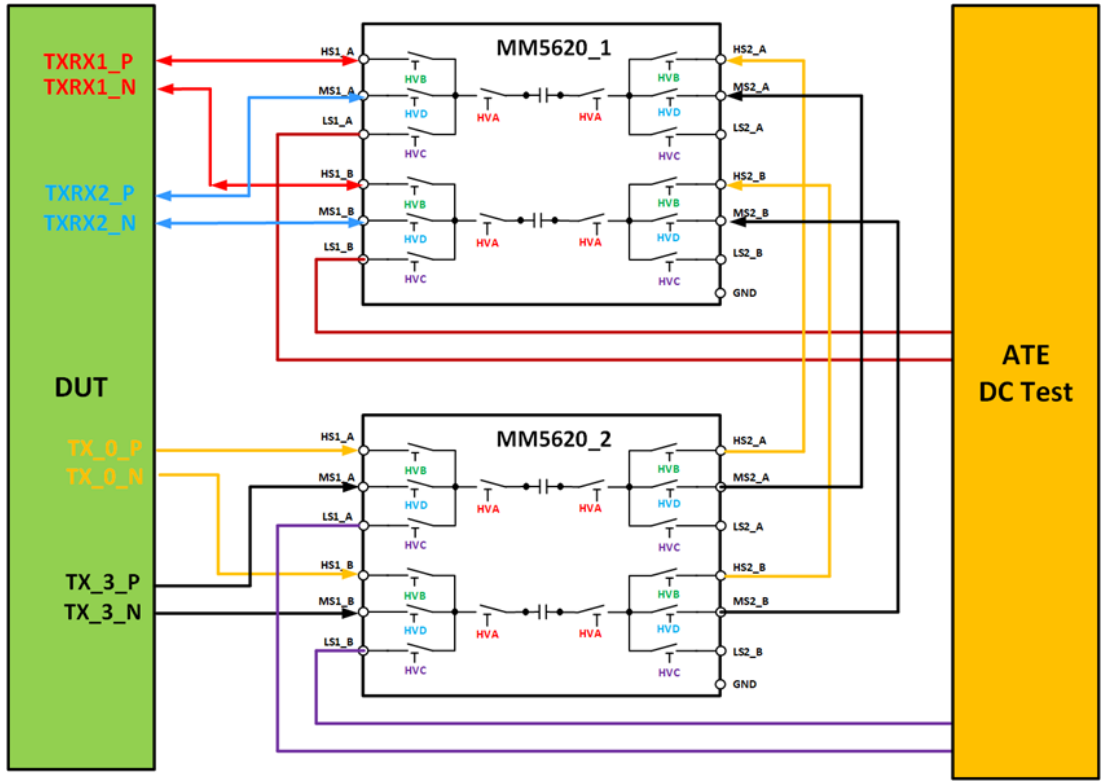
- Requirement/Use case:
  - TX diff signal (either TX0 or TX1) needs to be routed to two RX diff signals (RX0 and RX1)
  - Need to access all TX and RX pins through the LS paths for DC on/off test
- Solution: Add additional three gate control lines: *we can control each differential pair individually*

MM5625- Example Customer Use Case

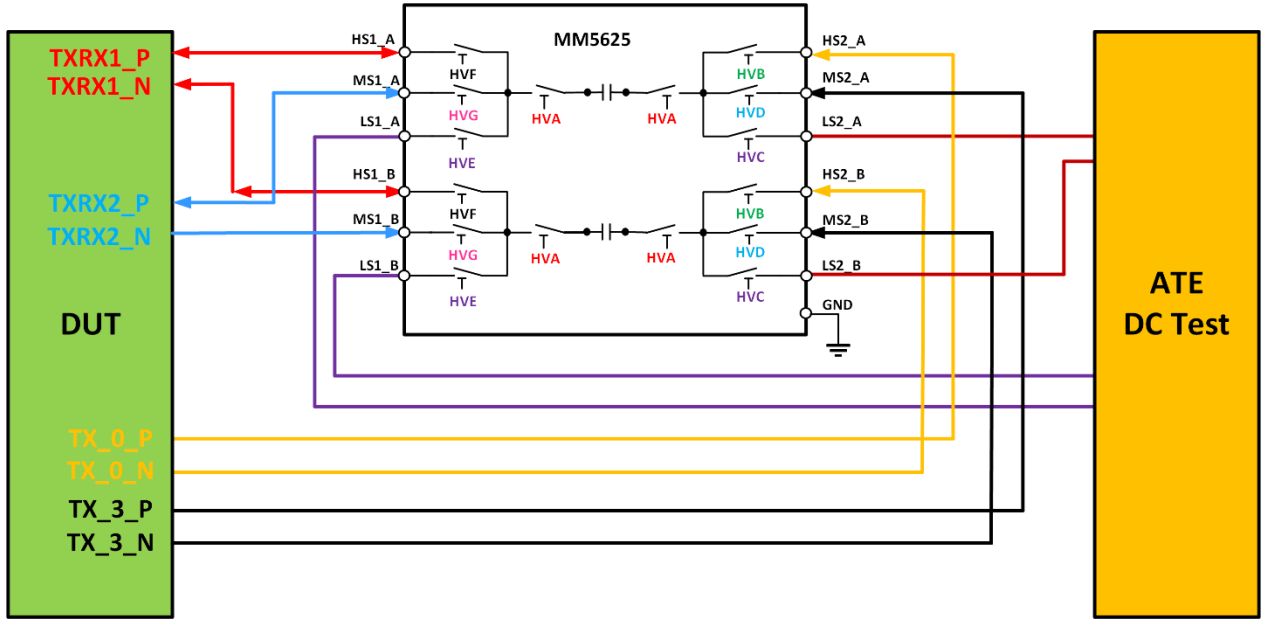
Single MM5625/27 device can support this more complex use case, with asymmetric TX/RX connections



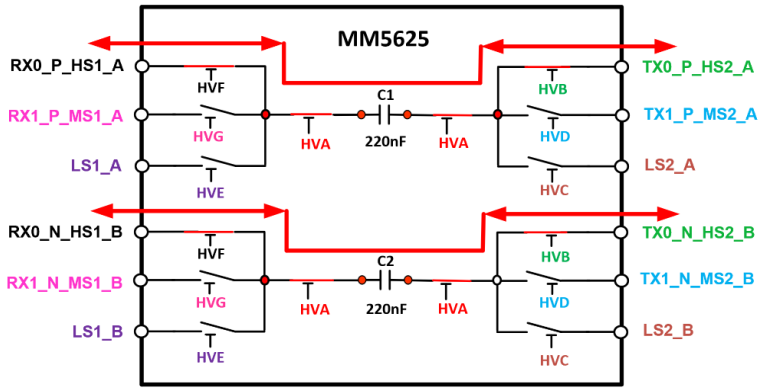
Currently needs (2) MM5620 devices



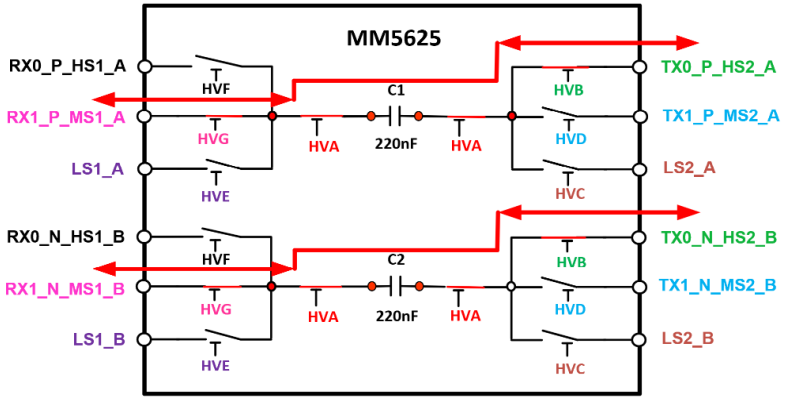
Will only need (1) MM5625 device



Signal Flow: New High-Speed connectivity scenarios (64Gbps)

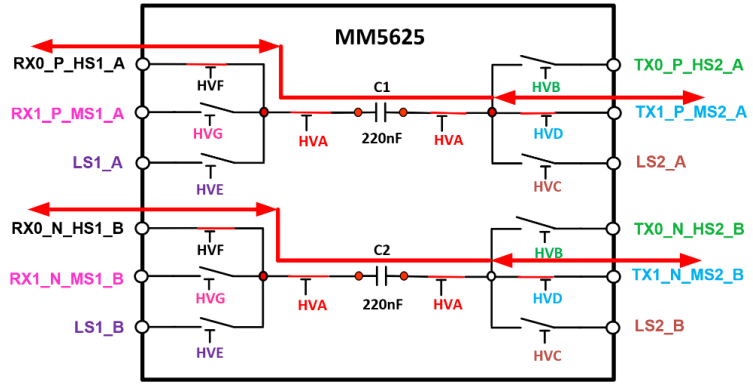


Case 1. TX0_P/N → RX0_P/N

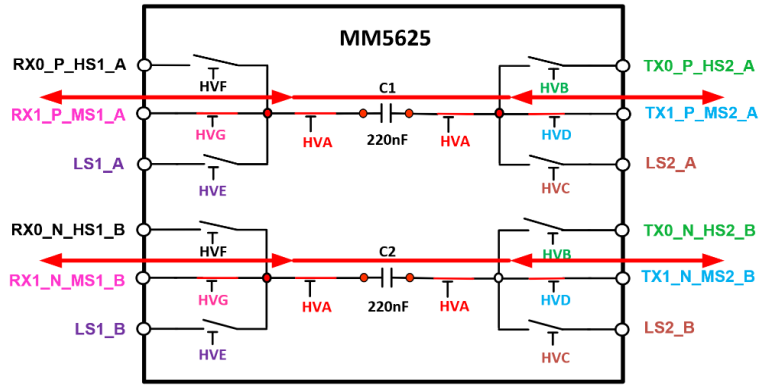


Case 2. TX0_P/N → RX1_P/N

New connection schemes enabled by MM5625

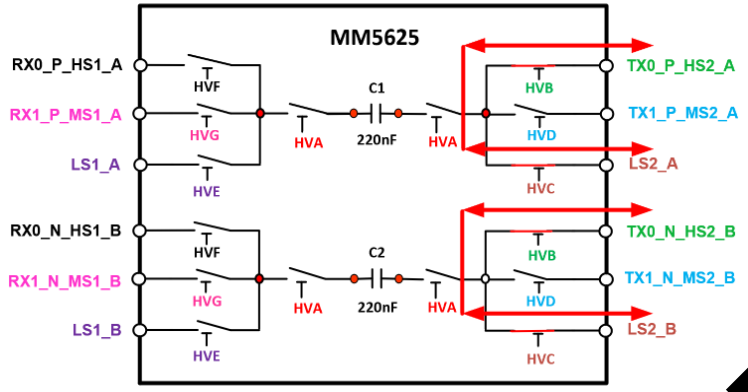


Case 3. TX1_P/N → RX0_P/N



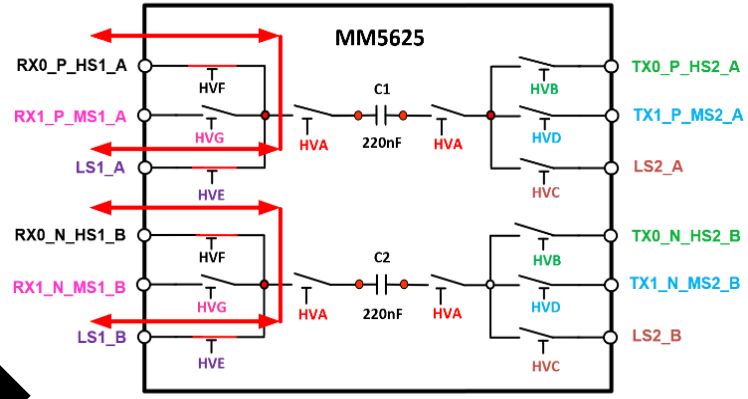
Case 4. TX1_P/N → RX1_P/N

Signal Flow: Low-Speed connectivity scenarios

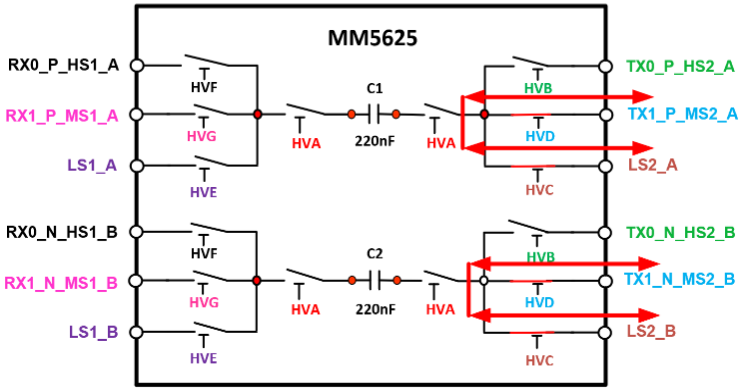


Case 1. TX0_P/N → LS2_A/B

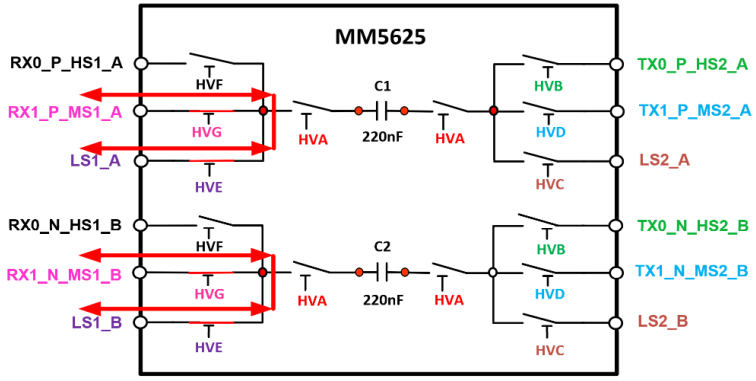
Now we have INDEPENDENT control between LS1 and LS2 paths



Case 3. RX0_P/N → LS1_A/B



Case 2. TX1_P/N → LS2_A/B

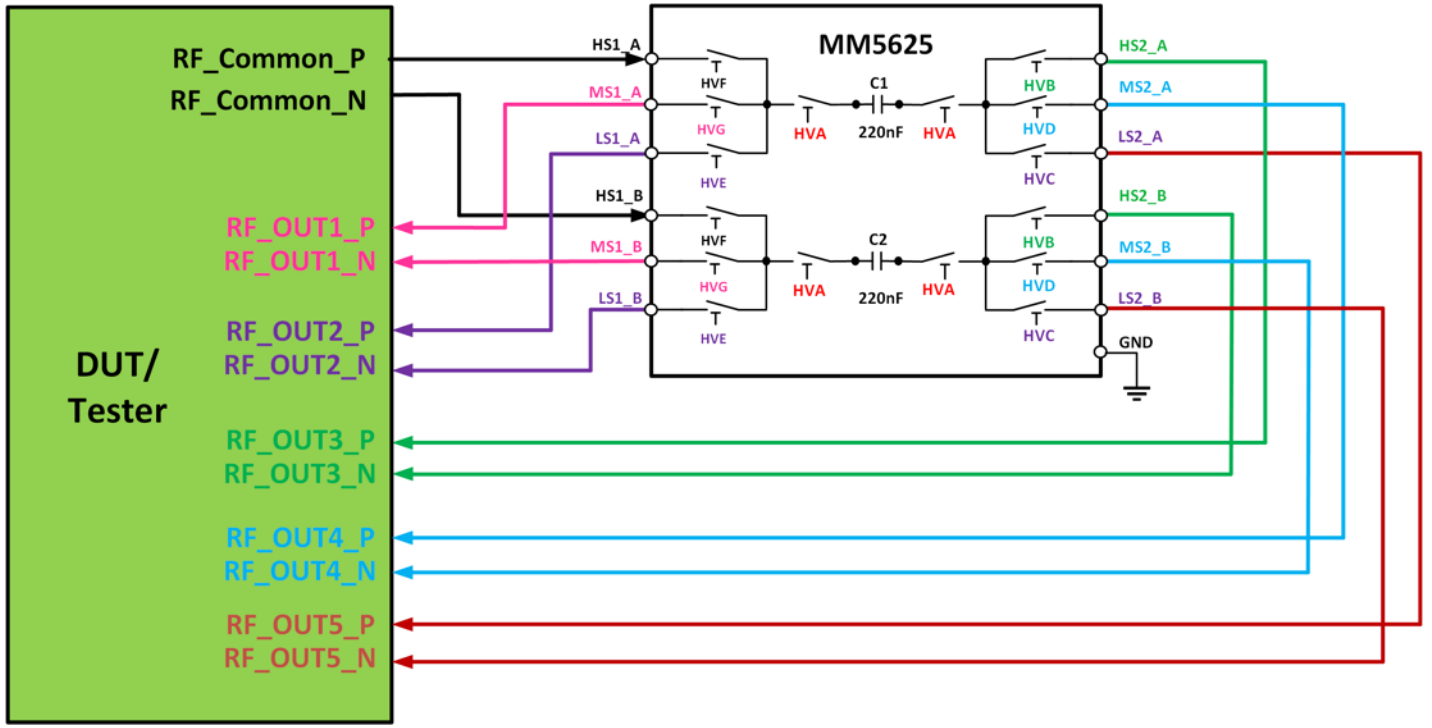


Case 4. RX1_P/N → LS1_A/B

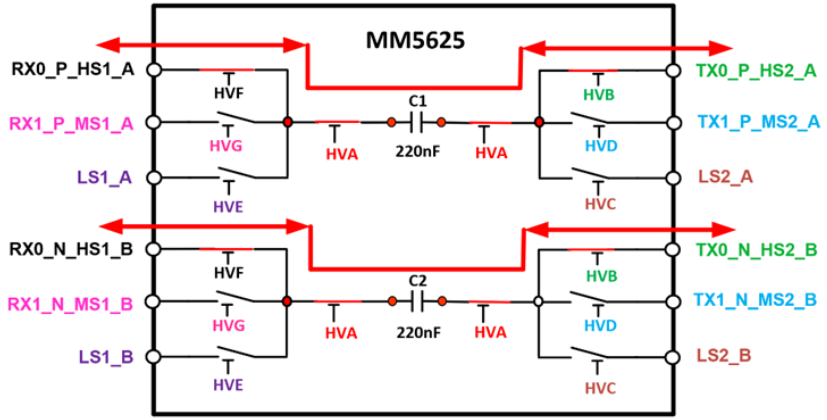
MM5625 Customer Use Case #3

7 control bits and 12 switches inside the MM5625 are going to create opportunities we haven't even thought of yet

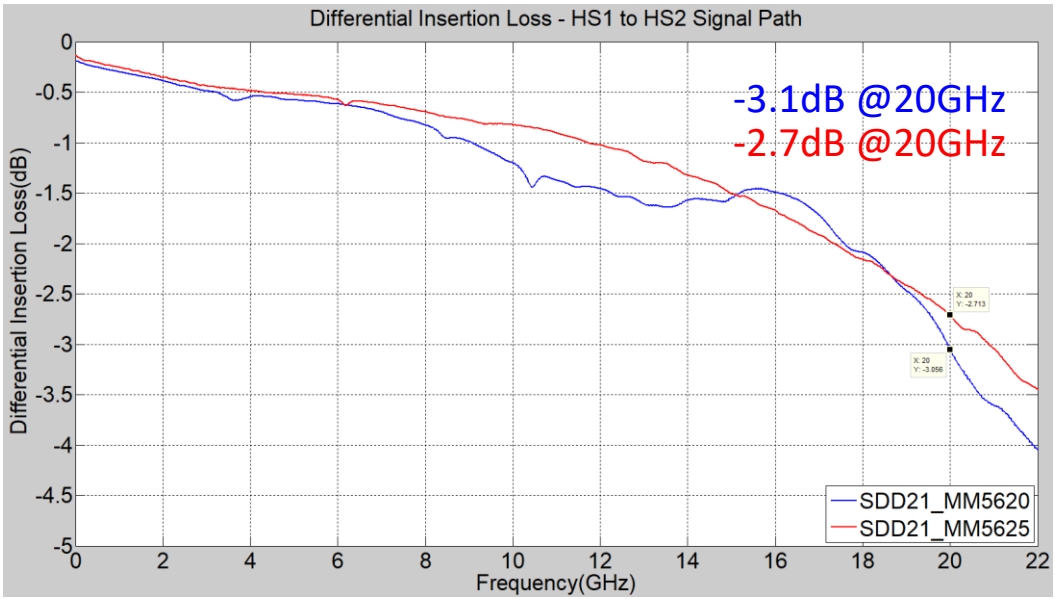
- Can you make a "Differential SP5T multiplexer" with MM5625?
- Sure, you can!
- 128 control states are supported and so creative engineers will find new applications for this very unique MM5625 product



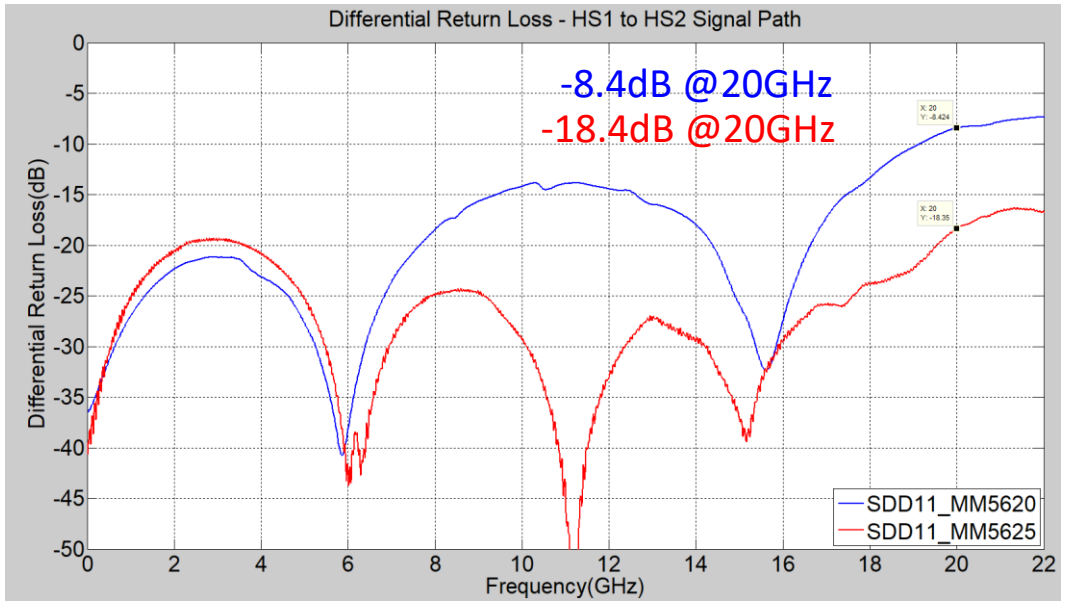
Measured Performance – MM5620 vs MM5625



MM5620
MM5625

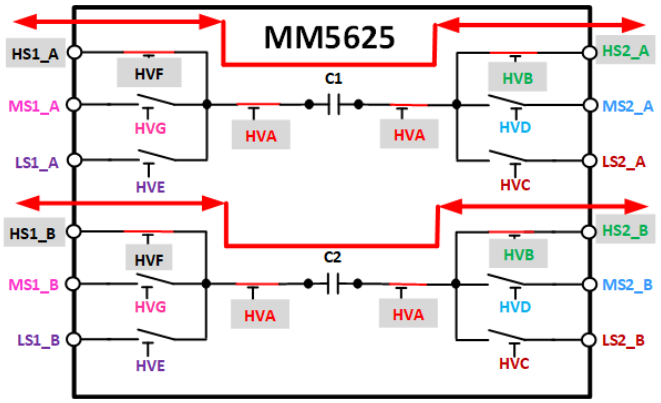


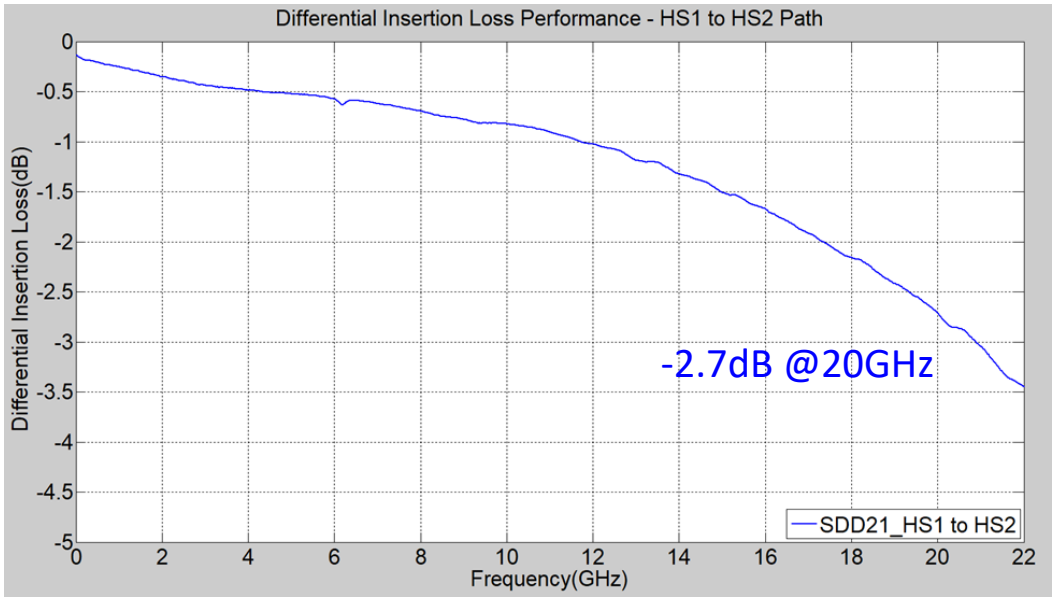
Differential Insertion Loss



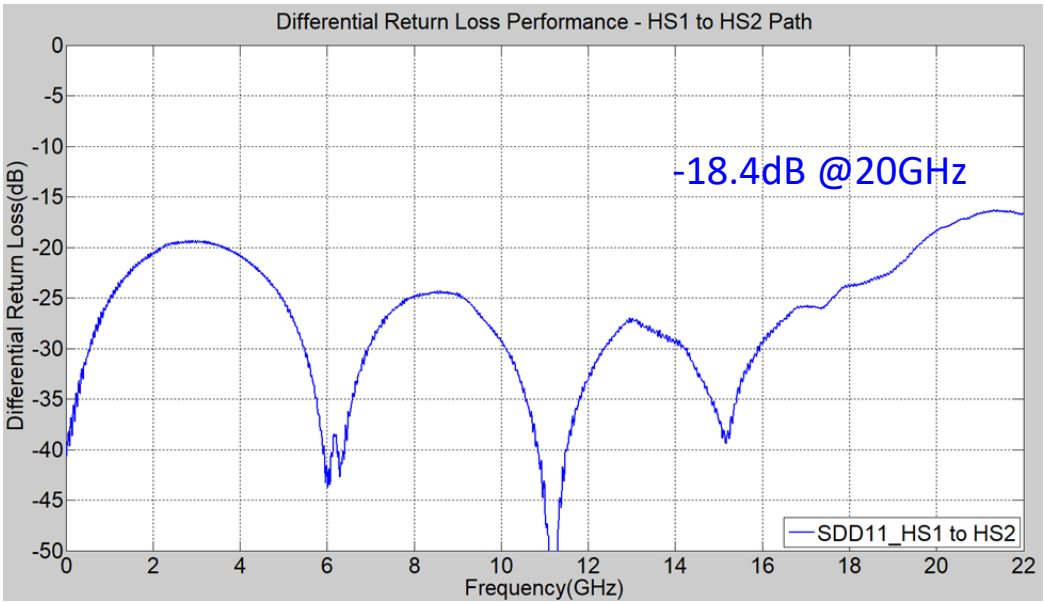
Differential Return Loss

MM5625 Measured Performance: HS1 to HS2 Signal Path



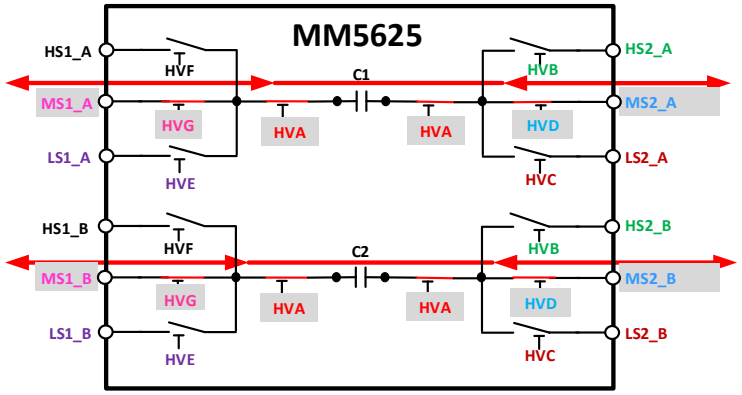


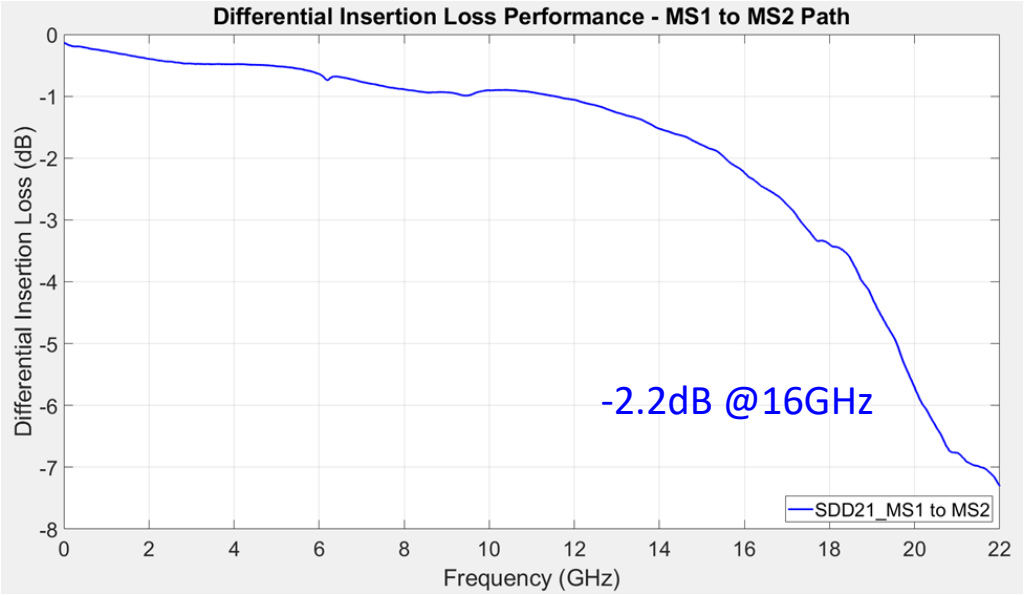
Differential Insertion Loss



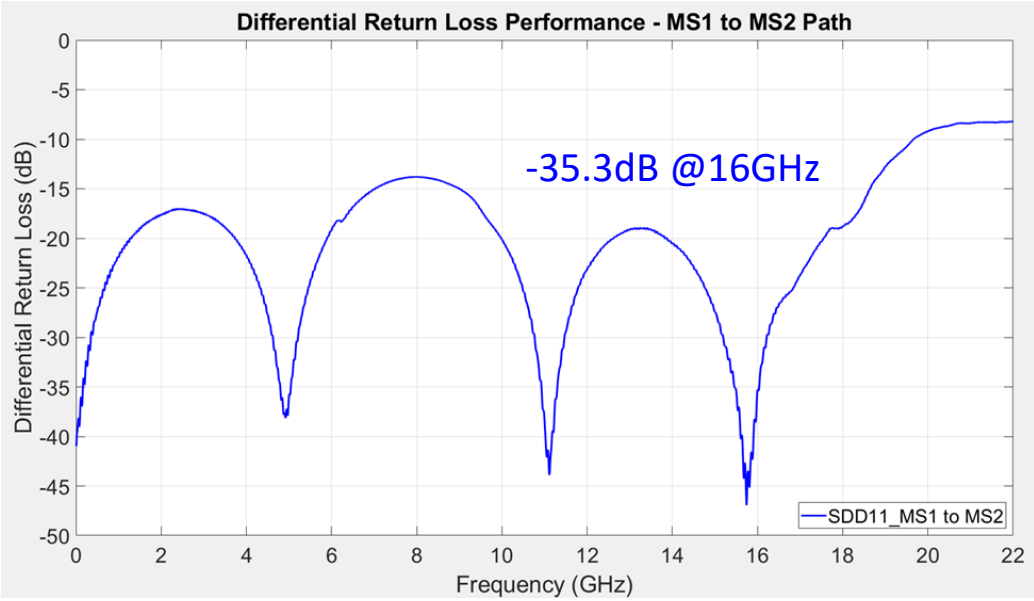
Differential Return Loss

MM5625 Measured Performance: MS1 to MS2 Signal Path



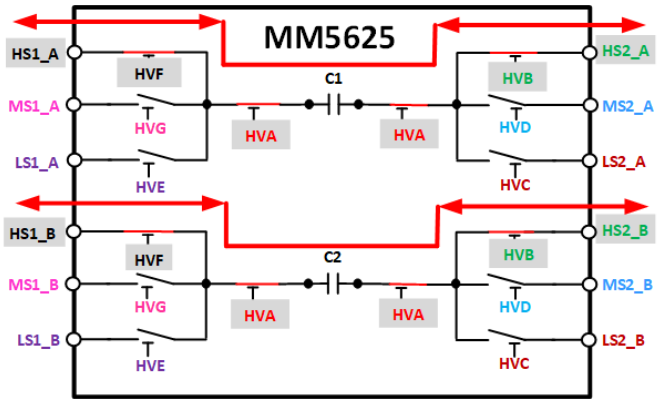


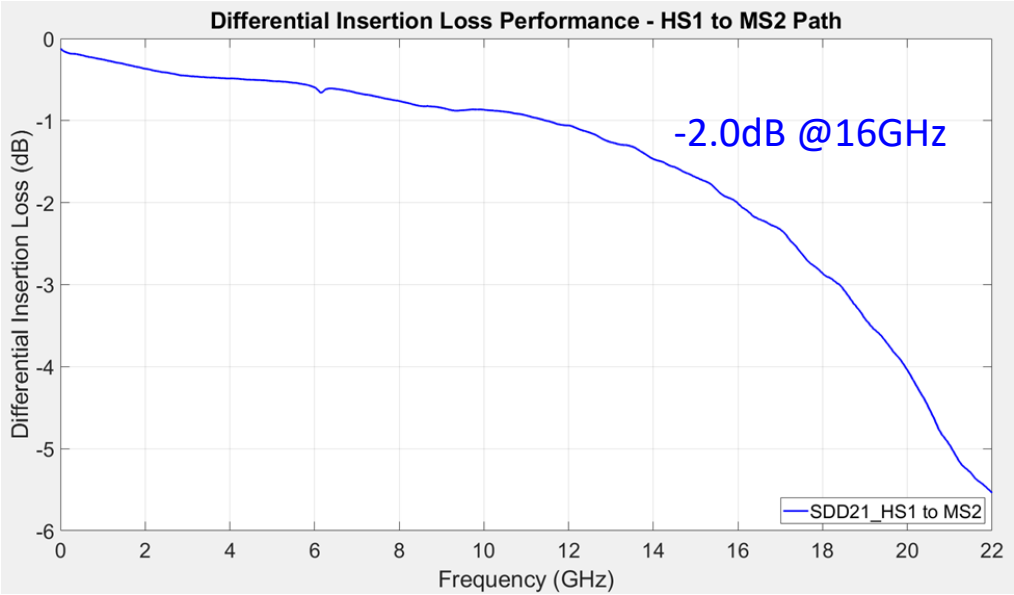
Differential Insertion Loss



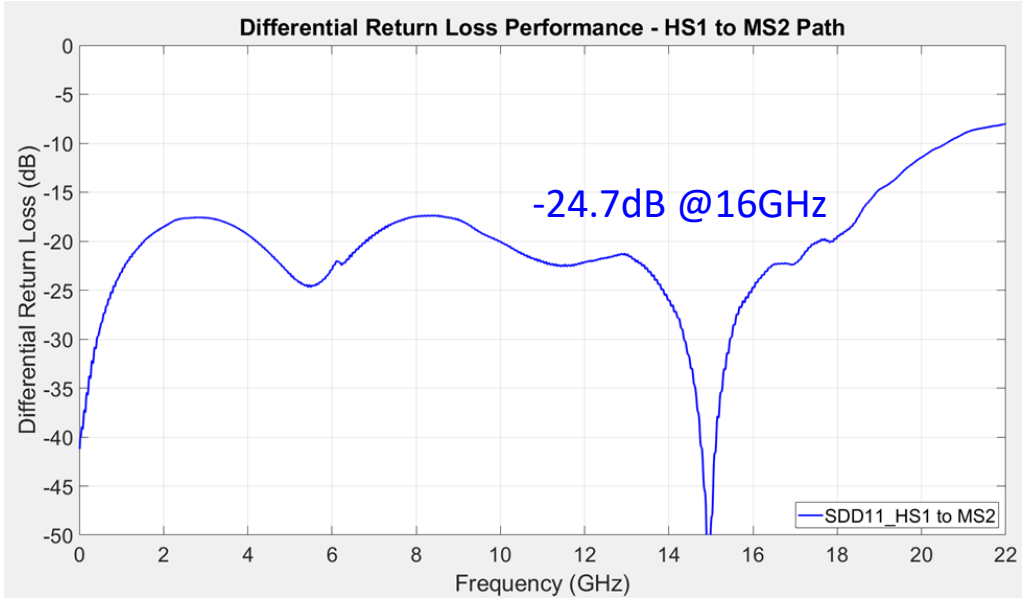
Differential Return Loss

MM5625 Measured Performance: HS1 to MS2 Signal Path



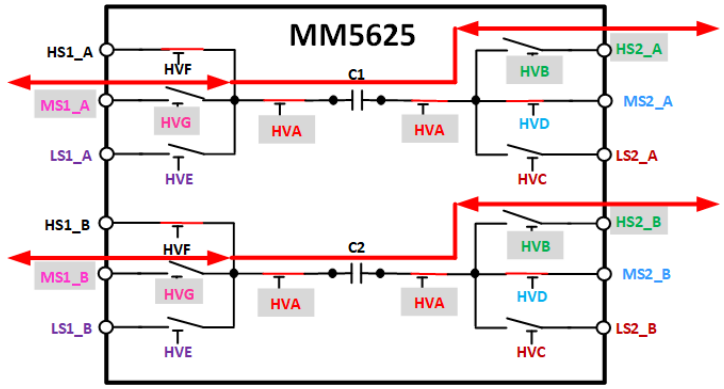


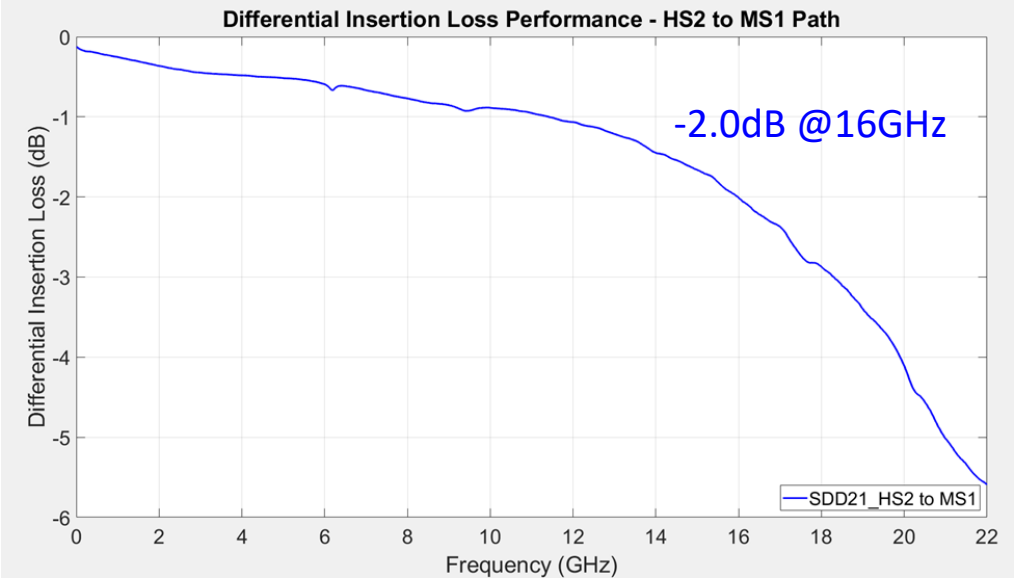
Differential Insertion Loss



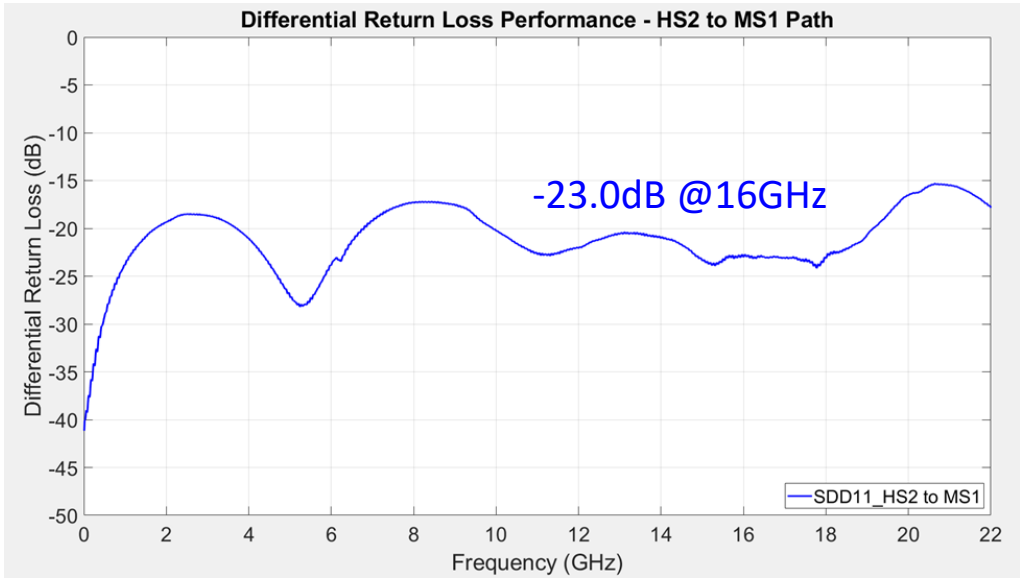
Differential Return Loss

MM5625 Measured Performance: MS1 to HS2 Signal Path





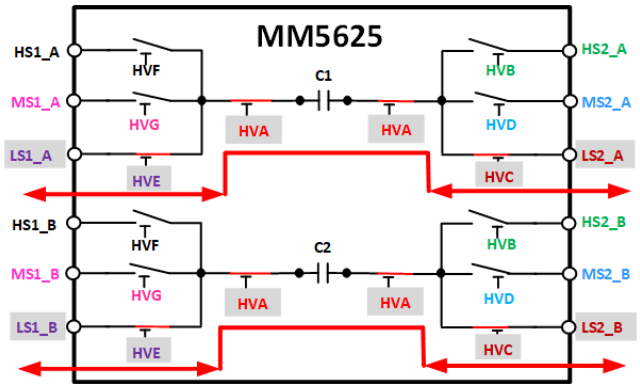
Differential Insertion Loss

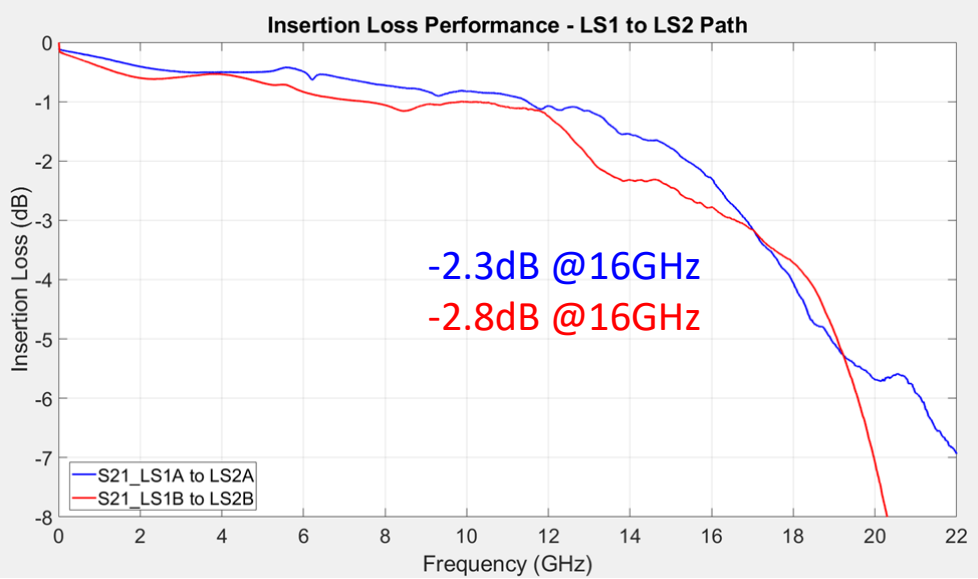


Differential Return Loss

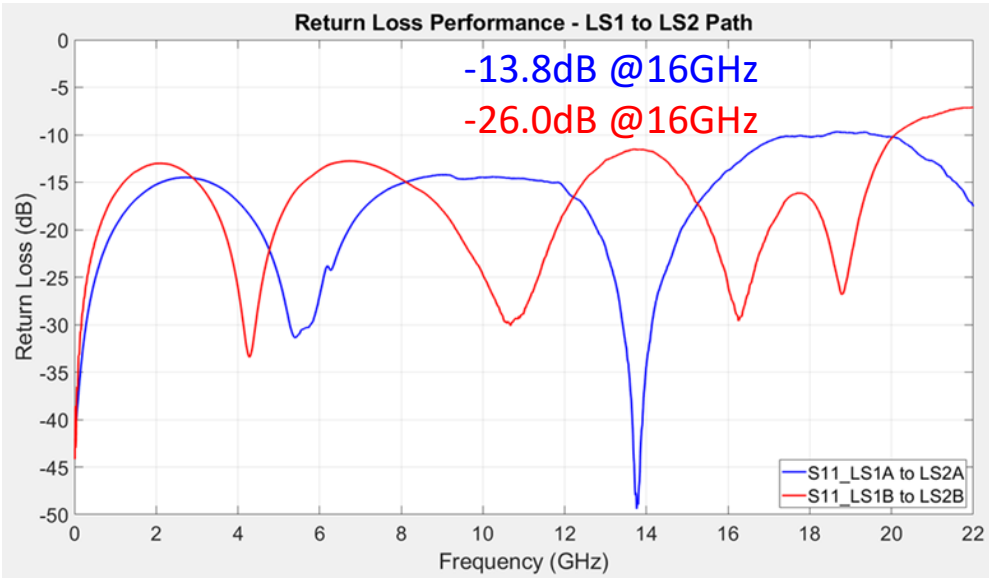
MM5625 Measured Performance: LS1 to LS2 Signal Path

LS1A to LS2A
LS1B to LS2B





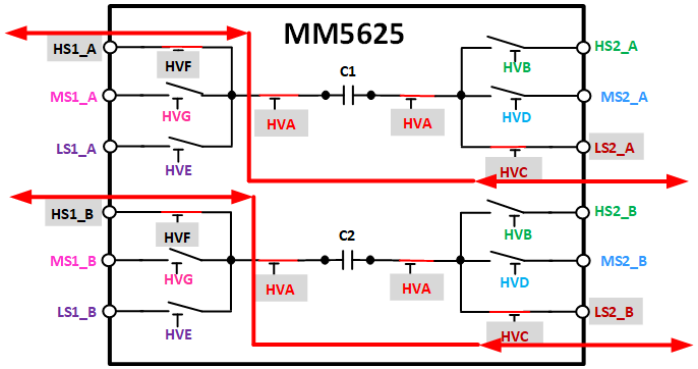
Single-ended Insertion Loss

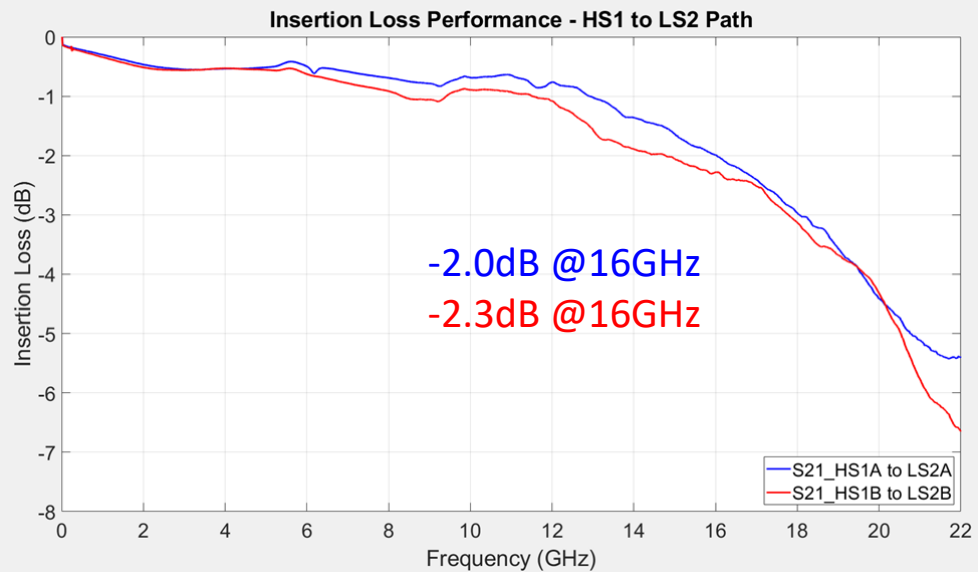


Single-ended Return Loss

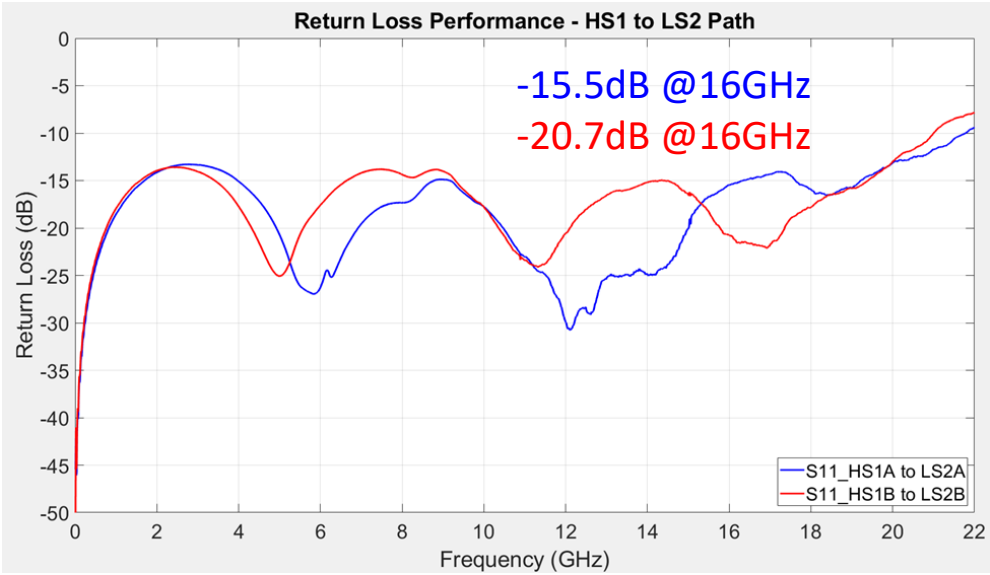
MM5625 Measured Performance: HS1 to LS2 Signal Path

LS1A to LS2A
LS1B to LS2B





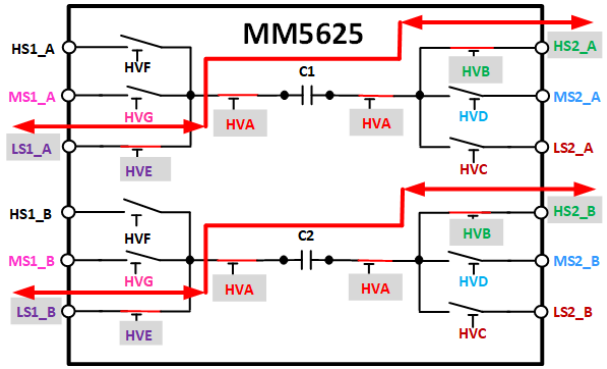
Single-ended Insertion Loss

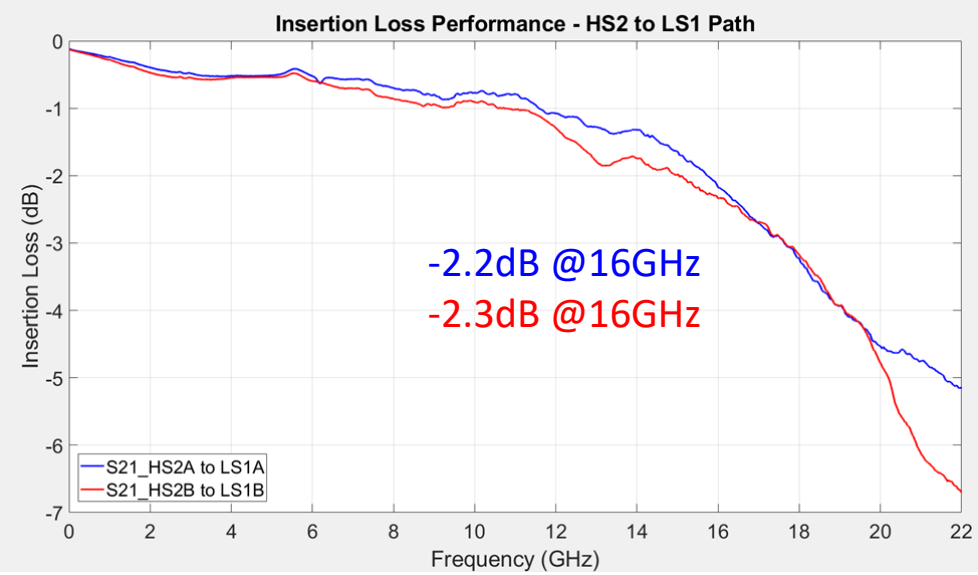


Single-ended Return Loss

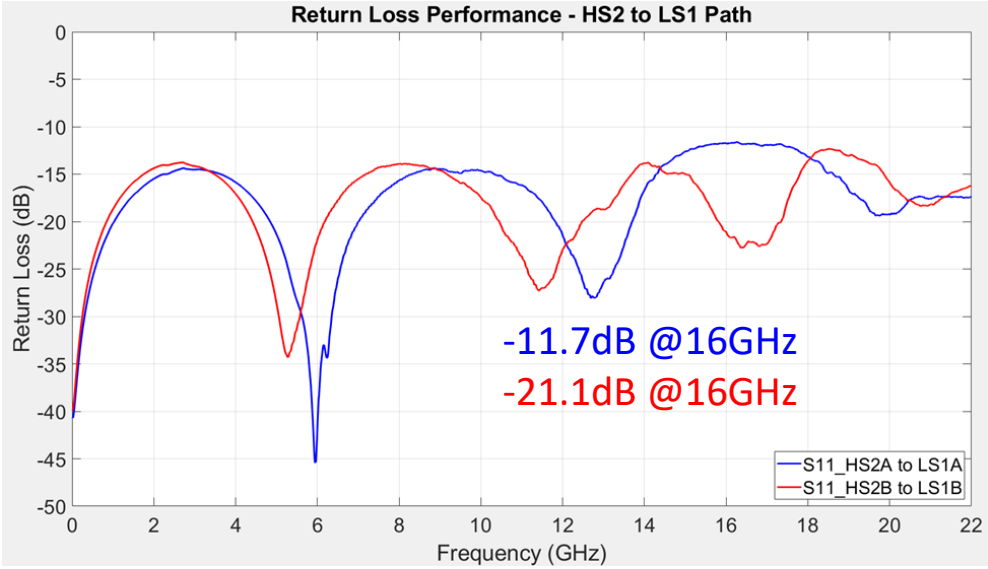
MM5625 Measured Performance: HS2 to LS1 Signal Path

LS1A to LS2A
LS1B to LS2B





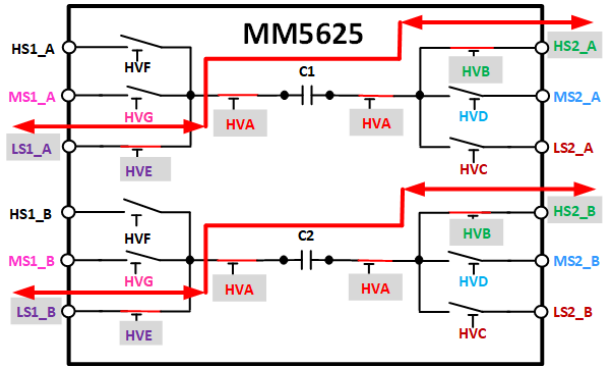
Single-ended Insertion Loss

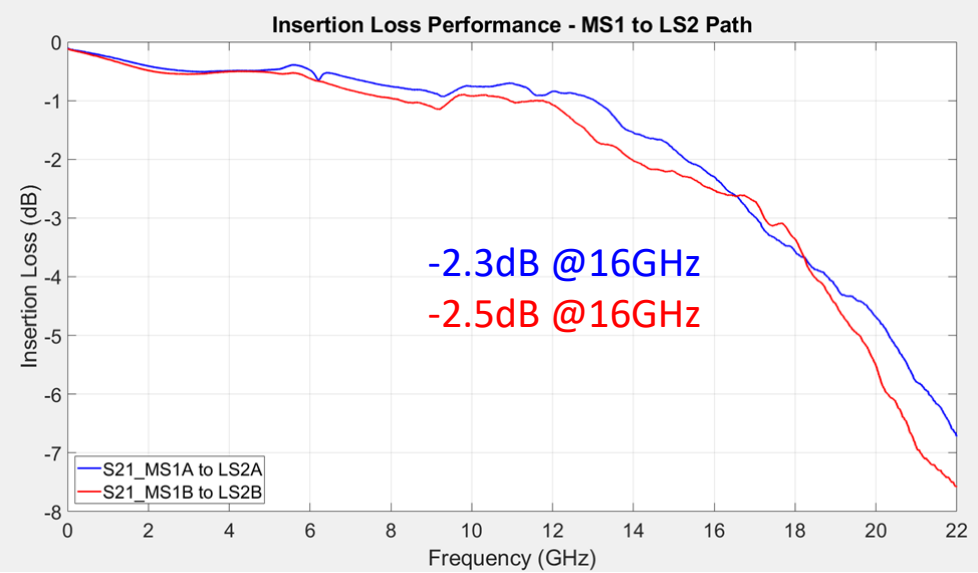


Single-ended Return Loss

MM5625 Measured Performance: MS1 to LS2 Signal Path

LS1A to LS2A
LS1B to LS2B



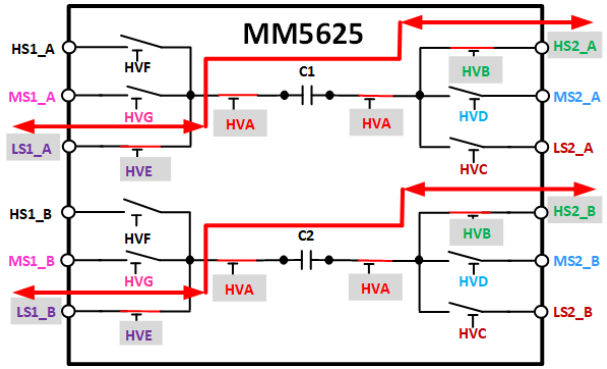


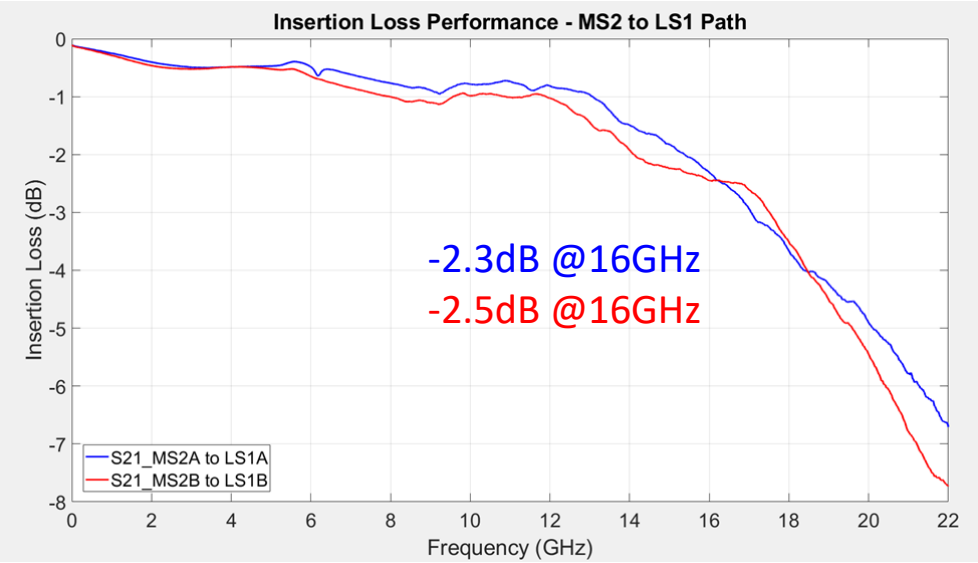
Single-ended Insertion Loss

Single-ended Return Loss

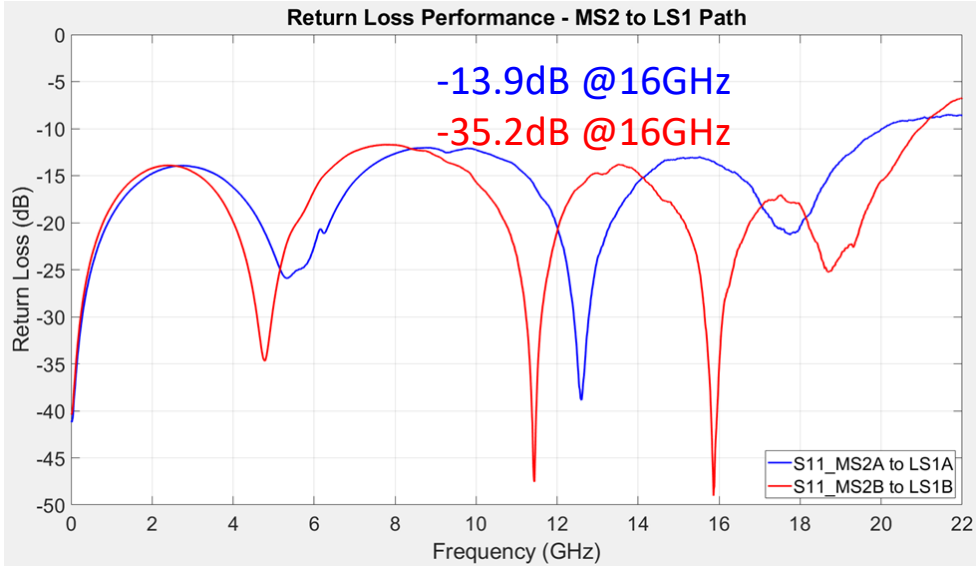
MM5625 Measured Performance: MS2 to LS1 Signal Path

LS1A to LS2A
LS1B to LS2B





Single-ended Insertion Loss

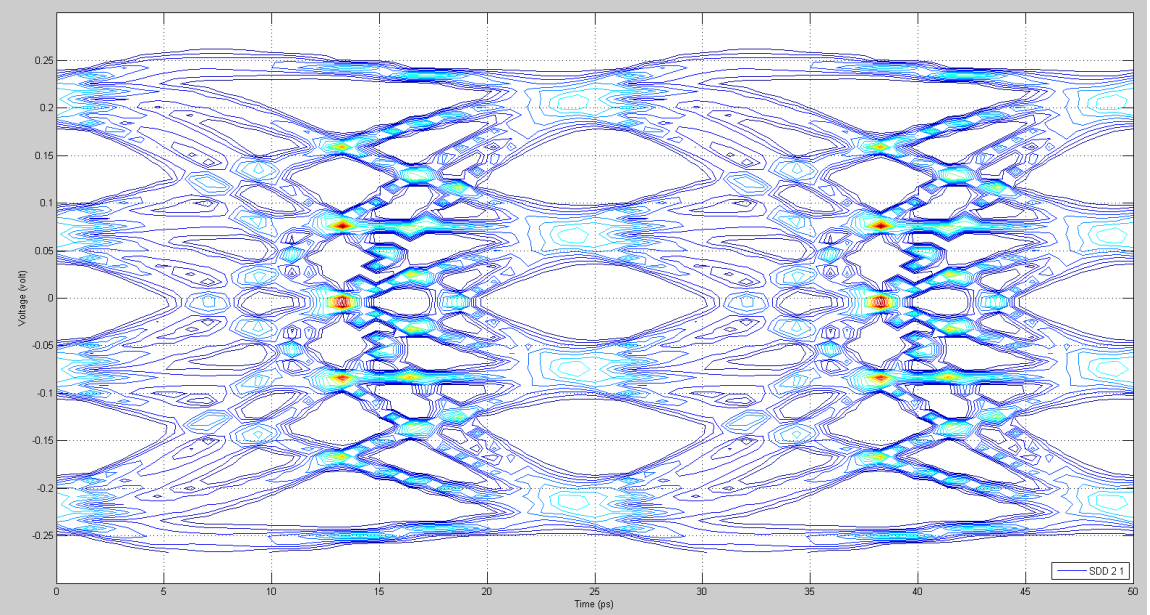


Single-ended Return Loss

Eye Performance Comparison – HS1 to HS2 Signal Path

Eye-Diagram Test Conditions

- Rise time 7.5ps (20 to 80%)
- PAM4, 40 Gbaud (80Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)

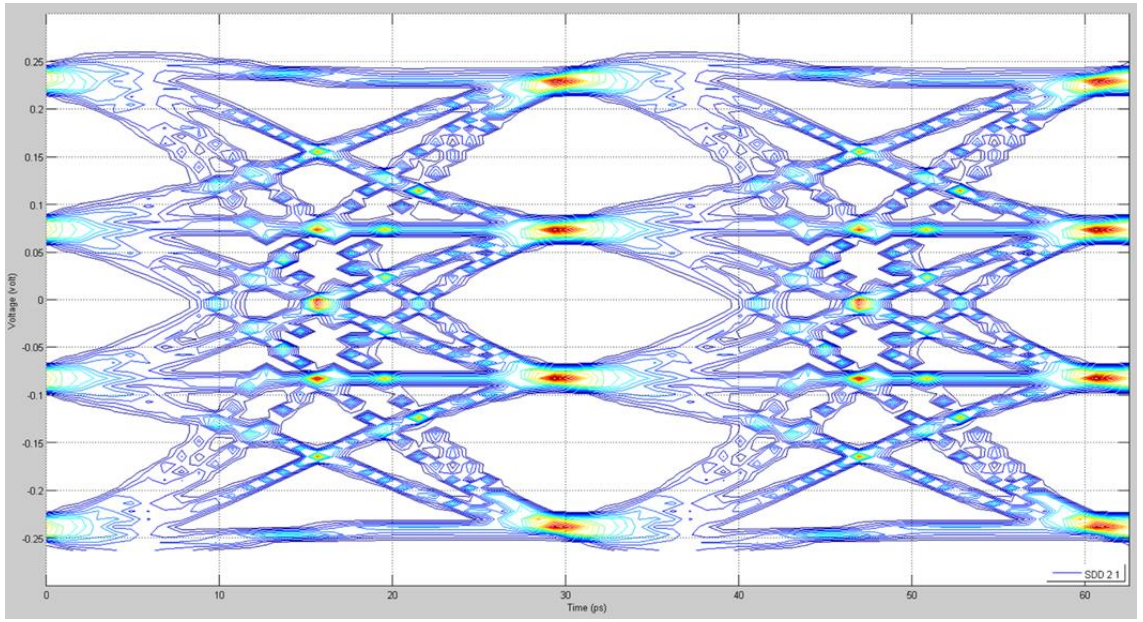


Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	80	79.74	10.54	7.23
1/2	80	80.58	11.03	6.99
2/3	80	79.74	10.28	7.36

Eye Performance Comparison – HS1 to HS2 Signal Path

Eye-Diagram Test Conditions

- Rise time 10ps (20 to 80%)
- PAM4, 32 Gbaud (64Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)

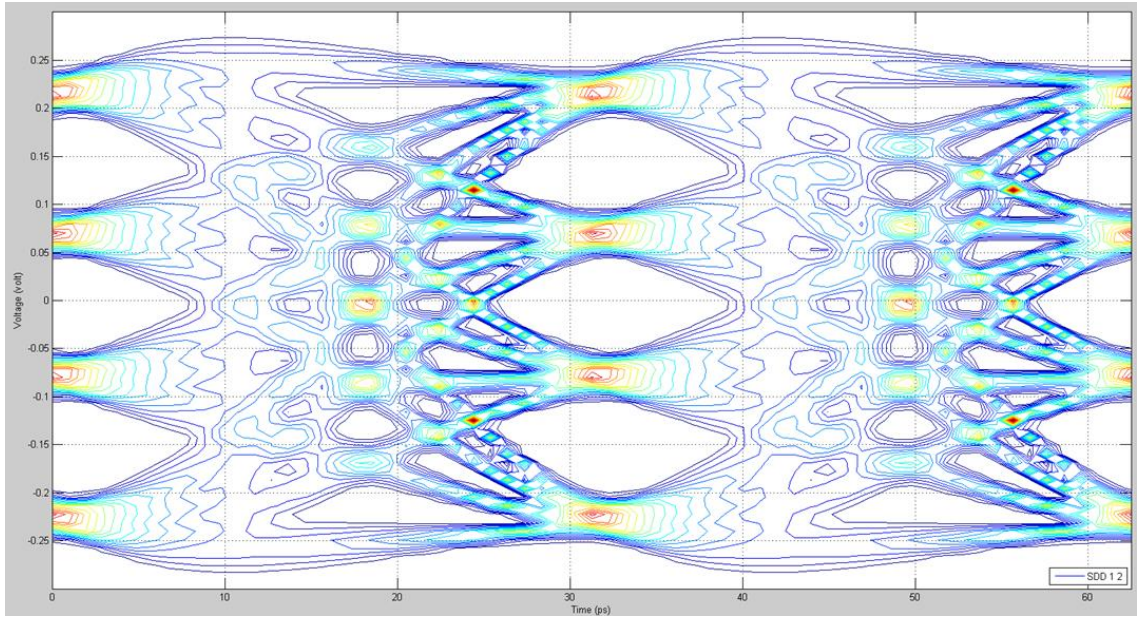


Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	64	134.09	17.56	6.85
1/2	64	134.08	18.32	6.47
2/3	64	134.42	18.04	6.61

Eye Performance Comparison – MS1 to MS2 Signal Path

Eye-Diagram Test Conditions

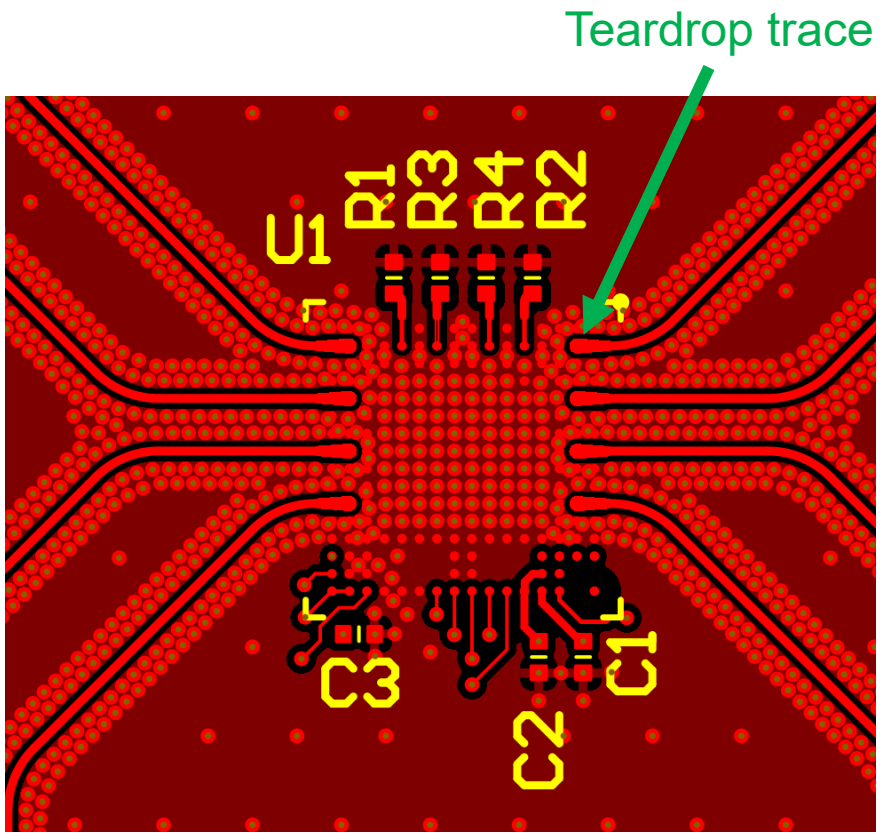
- Rise time 10ps (20 to 80%)
- PAM4, 32 Gbaud (64Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)



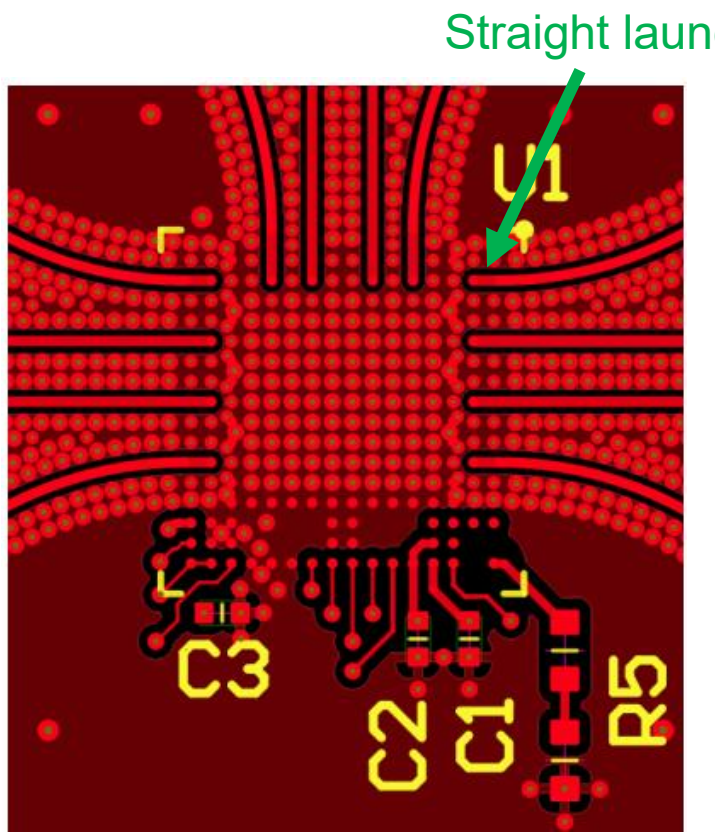
Eye	Bit Rate (Gbps)	Eye Height (mV)	Eye Width (ps)	Total Jitter (RMS, ps)
0/1	64	96.58	11.23	14.16
1/2	64	96.98	13.73	12.39
2/3	64	96.33	11.20	14.18

MM5625 – Customer Evaluation Board

- EVK performance is improved with optimized PCB launch



MM5620 EVK1 R4.0



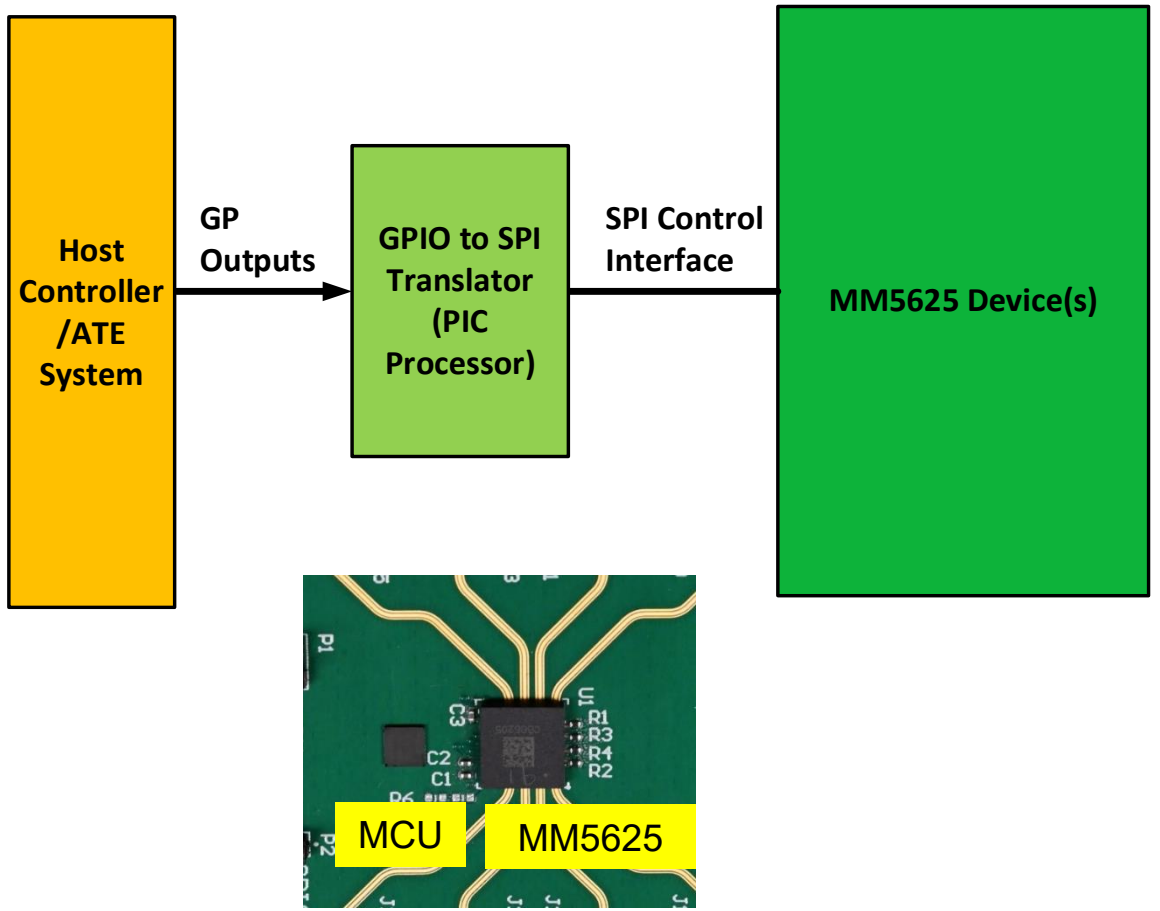
MM5625 EVK

MM5625 - GPIO to SPI Translator

Reduce any barriers to adoption due to SPI requirement – MAKE IT EASY TO ADOPT!

- MM5625 will support SPI control interface only
- For customers who are reluctant to use SPI:
  - Menlo will offer a reference circuit for programming multiple MM5625 via GPIO
  - PIC16 series MCU from Microchip
  - Allows programming of all MM5625 with general purpose +3.3V/+5V utility bits from testers
  - Adds $1.50 and 6x6mm of board area
  - Can be setup for serial, parallel as well as programming multiple MM5625
- Reference board and software available
- GPIO to SPI Translator Application Package:

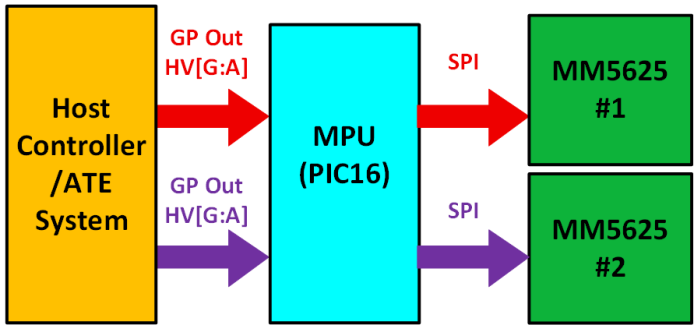
https://menlomicro.com/resources/download-log/2361



MM5625 - Applications circuits for multiple GPIO to SPI modes

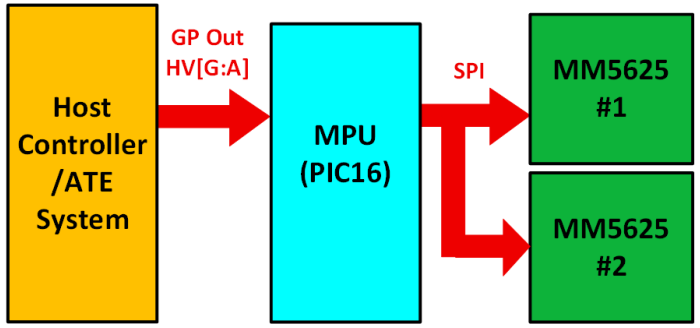
Reduce any barriers to adoption due to SPI requirement – MAKE IT EASY TO ADOPT!

Independent Control



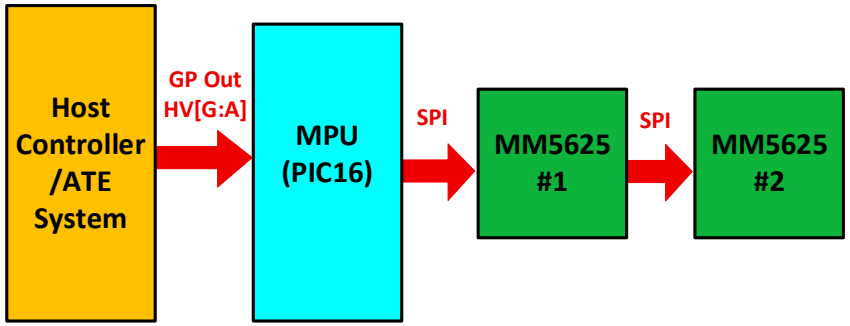
- Can control (1) or (2) MM5625 with independent GPIO control lines
- Required I/O Pins: 20

Parallel Control



- Can control (1) to (n) MM5625 with independent GPIO control lines
- Required I/O Pins: 10

Series Control



- Can control (1) to (n) MM5625 with daisy-chained control lines
- Required I/O Pins: 10

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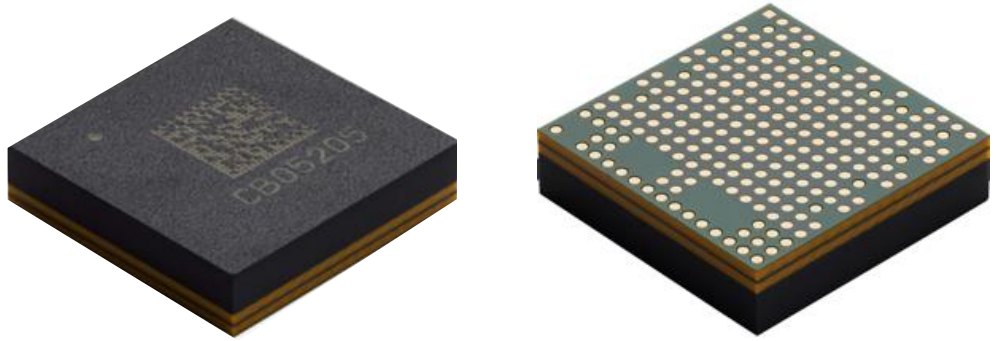
MM562x SPI Control

Daisy Chain Control Example



Control Register Definition

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit 15							bit 8

1 0 0 1 0 0 1 0

Bit 15: WR_EN
“1” :Write Control
“0” : Read Control

Bit 13: SLEEP
“1” : Enabled
“0” : Disabled

Bit 13:
“1” : VPP under-voltage comparator is disabled
“0” : VPP under-voltage comparator is enabled

Bit 14: FSTAT
“1” : Faulted
“0” : Not faulted

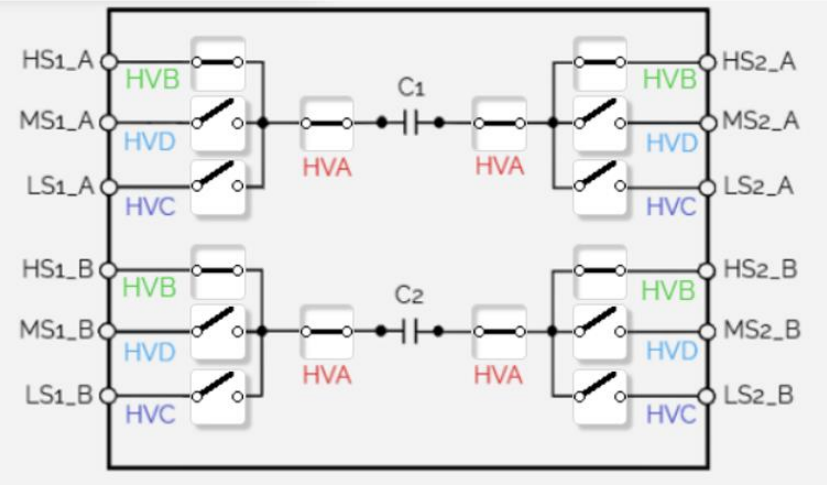
Bit 12: FLTMODE
“1” : Fault Detection Disabled
“0” : Fault Detection Enabled

Bit 9: CPEN
“1” : Charge Pump Enabled
“0” : Charge Pump Disabled

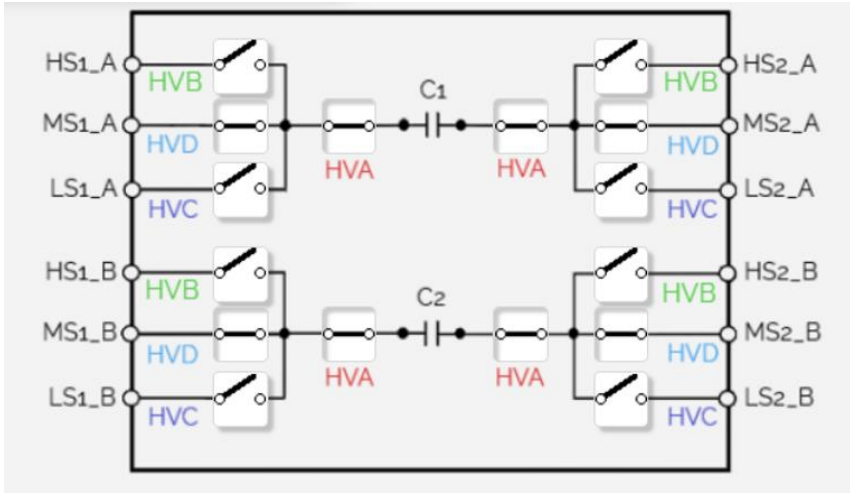
Control Register Definition

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	0	0	HVD	HVC	HVB	HVA
bit7							bit 0
0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	1



HS1 to HS2 Path: HVA and HVB ON(0x03)

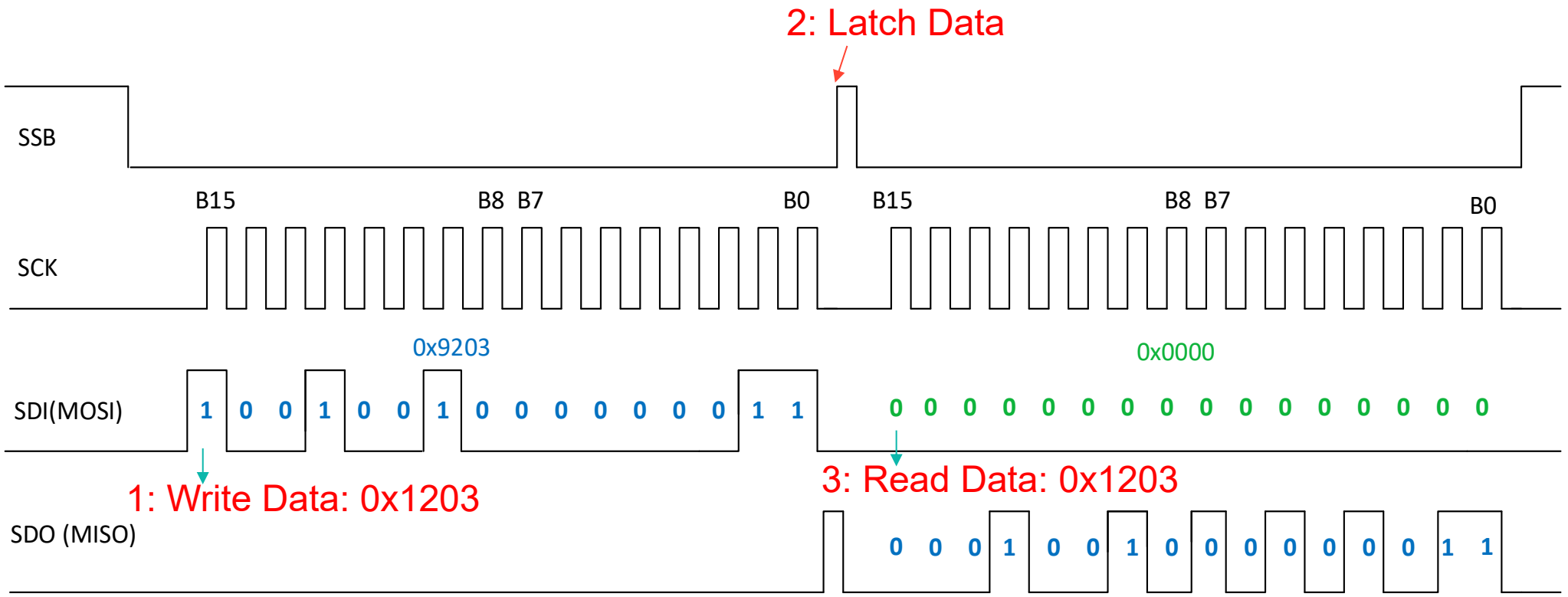


MS1 to MS2 Path : HVA and HVD ON (0x09)

Control Patterns

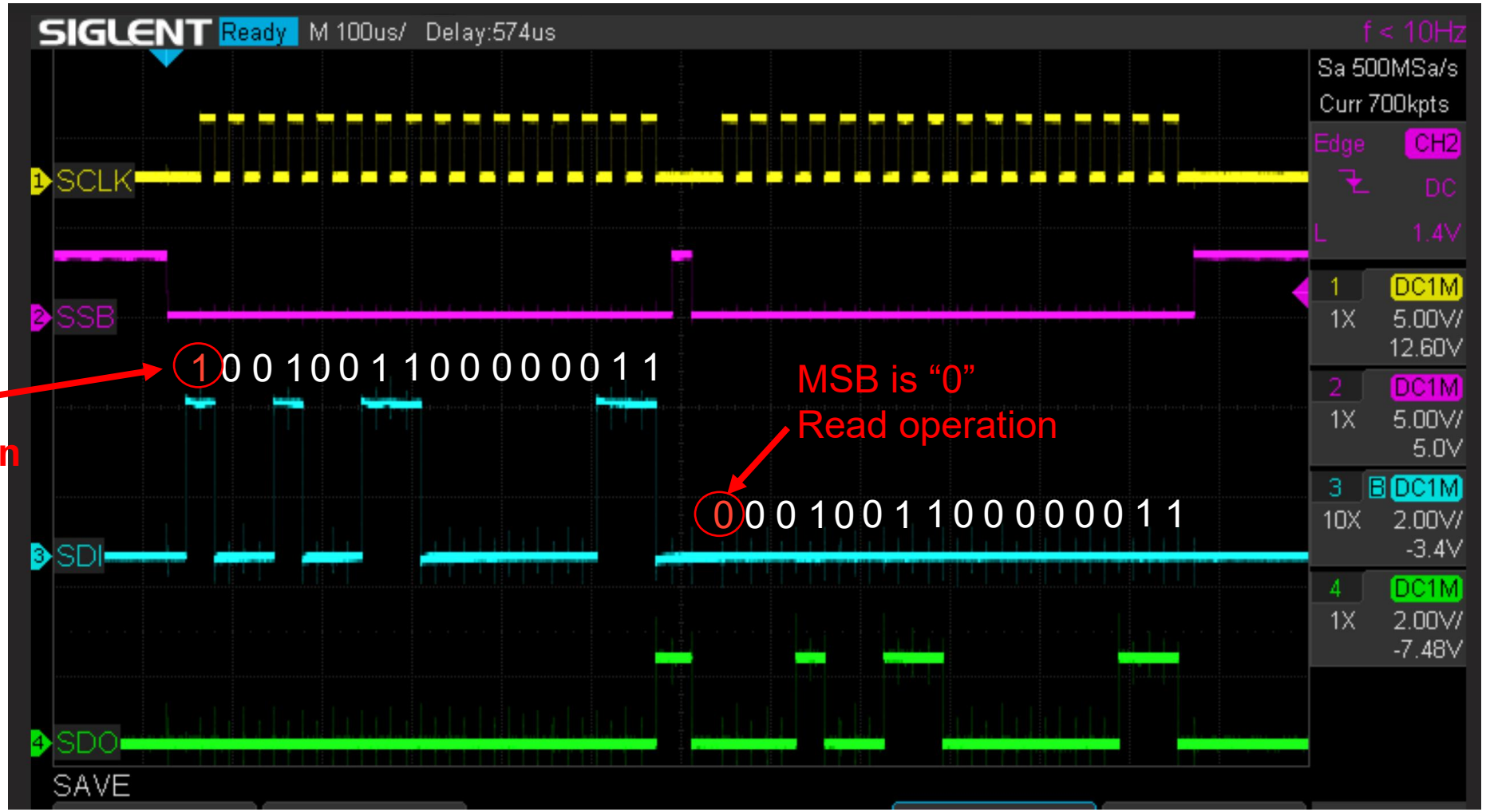
Control Example (one 16-bit word)	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0x00 00 – READ DATA	0				0				0				0			
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x92 00 – Charge Pump ON, Fault Mode DISABLE, ALL OFF (OPEN)	9				2				0				0			
	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
0x92 03 – Charge Pump ON, Fault Mode DISABLE, HS1 – HS2	9				2				0				3			
	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1
0x92 05 – Charge Pump ON, Fault Mode DISABLE, LS1 – LS2	9				2				0				5			
	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1
0x92 06 – Charge Pump ON, Fault Mode DISABLE, HS1 – LS1 and HS2 – LS2	9				2				0				6			
	1	0	0	1	0	0	1	0	0	0	0	0	0	1	1	0
0x92 09 – Charge Pump ON, Fault Mode DISABLE, MS1 – MS2	9				2				0				9			
	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1
0x92 0a – Charge Pump ON, Fault Mode DISABLE, HS1 – MS1 and HS2 – MS2	9				2				0				a			
	1	0	0	1	0	0	1	0	0	0	0	0	1	0	1	0
0x92 0c – Charge Pump ON, Fault Mode DISABLE, MS1 – LS1 and MS2 – LS2	9				2				0				c			
	1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0

One Device Control



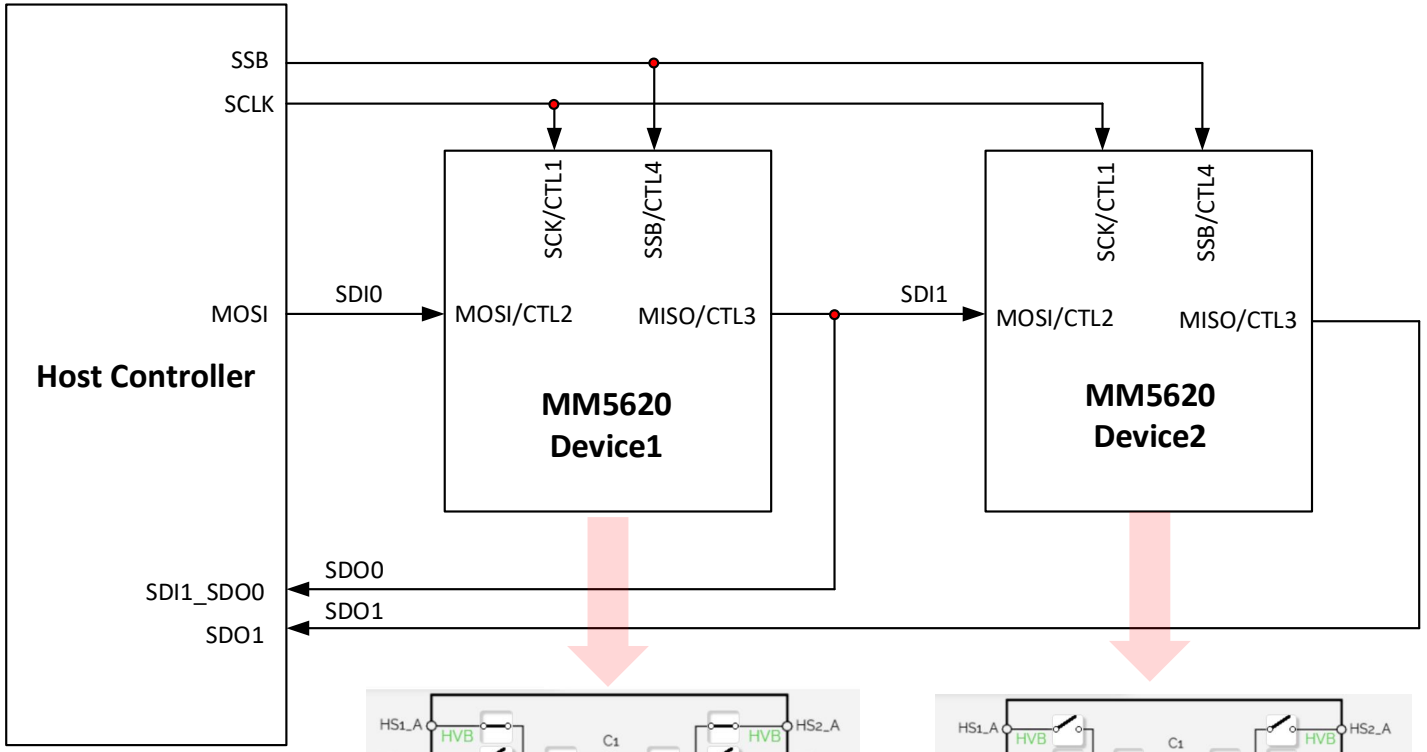
Write data 0x1203 (SDI) followed by read data to verify latched data 0x1203(SDO)

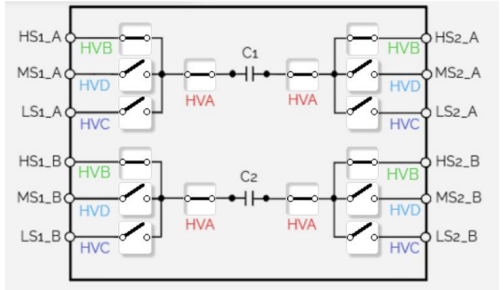
One Device Control Write

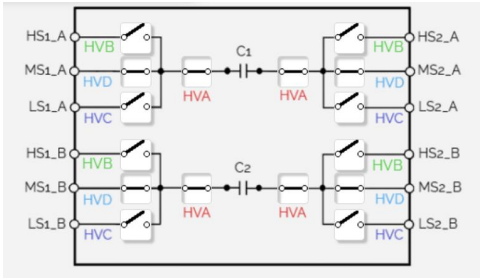


Write 1 word(SDI) and Read it back (SDO)

MM5620 Daisy Chain Example: 2 Devices







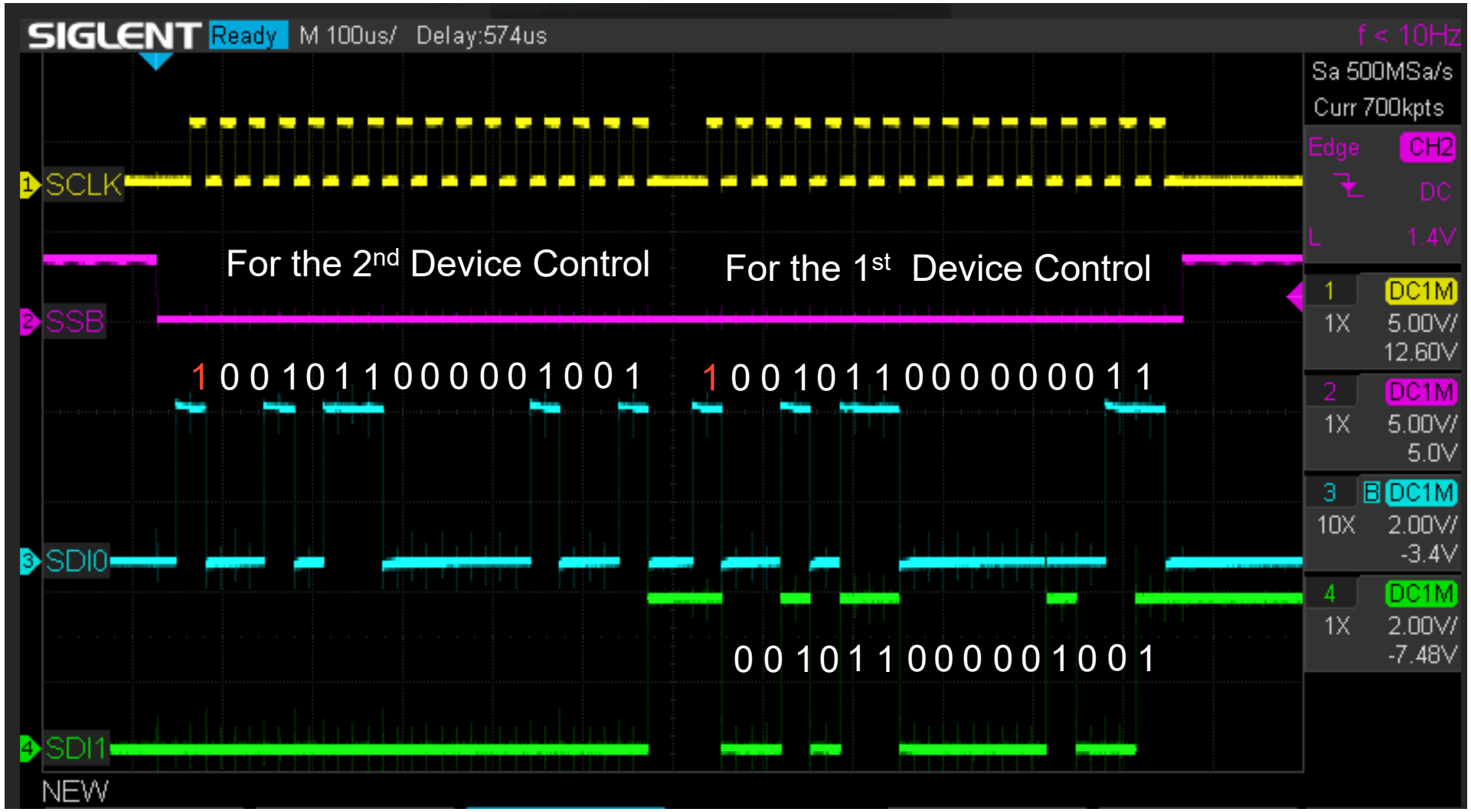
Status Register				Switch State
Bit3	Bit2	Bit1	Bit 0	
HVD	HVC	HVB	HVA	
0	0	0	0	ALL OFF (OPEN)
0	0	1	1	HS1 – HS2
0	1	0	1	LS1 – LS2
0	1	1	0	HS1 – LS1 and HS2 – LS2
1	0	0	1	MS1 – MS2
1	0	1	0	HS1 – MS1 and HS2 – MS2
1	1	0	0	MS1 – LS1 and MS2 – LS2
1	1	1	1	ALL ON (CLOSED)

Status Register (Lower 4 bits)

Device 1:
HVA and HVB ON(HS1 – HS2 ON)

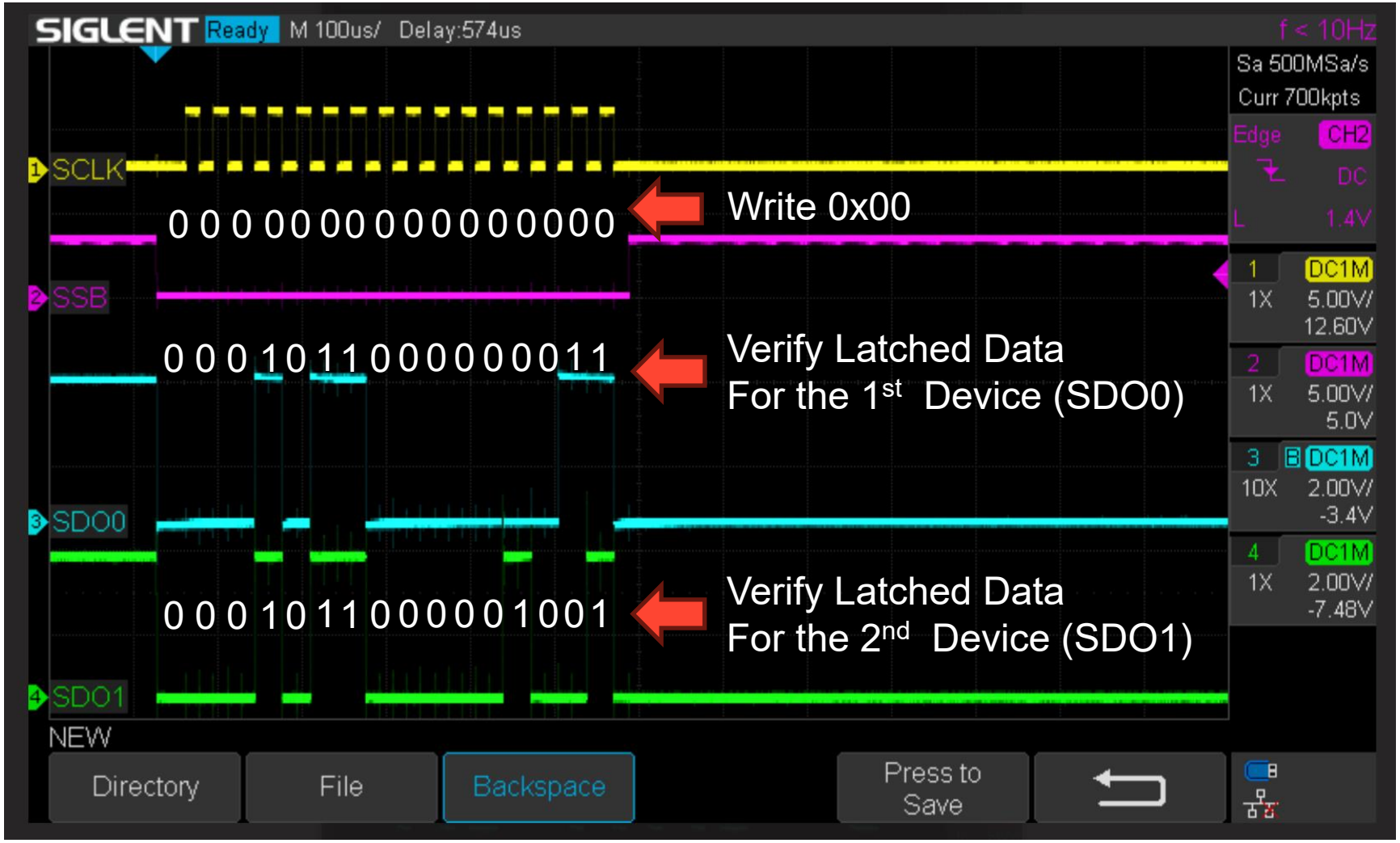
Device 2:
HVA and HVD ON (MS1 – MS2 ON)

MM5620 Daisy Chain Example: 2 Devices



Write 2 words (SDI0) and Monitor SDI1(SDO0)

MM5620 Daisy Chain Example: 2 Devices (continued)



Write 0x00 to read latched data and Verify SDO0 and SDO1

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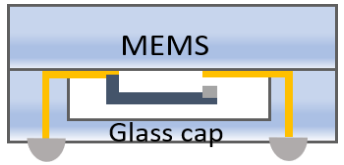
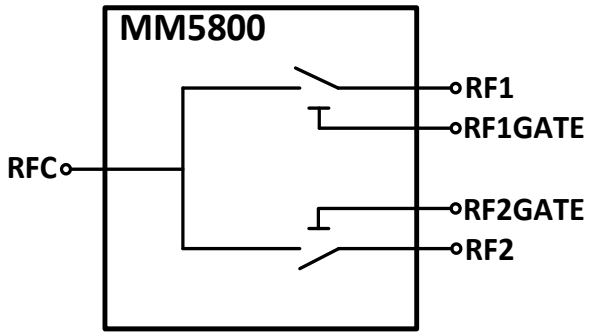
MM5800
DC – 70 GHz
SPDT Switch

Product Roadmap – MM5800 DC to 70 GHz SPDT Switch

New Die for mmWave Applications

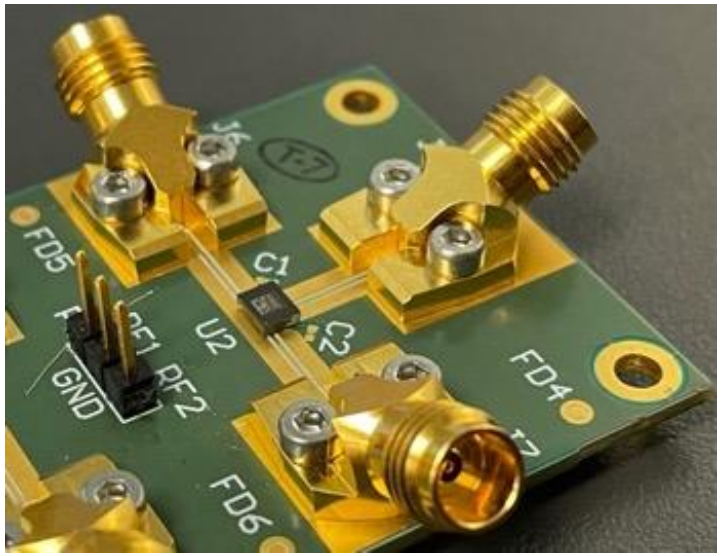
- Single SPDT
- Low Loss: 0.4 dB @ 40 GHz
- High Power: 2 W (CW), 20 W (pulsed)
- High Linearity: 95 dBm (IP3)
- High Isolation: 30 dB @ 40 GHz
- Fast Switching Speed: 8 µs
- High Reliability: >3 B switch cycles
- WL-CSP easy to assemble package





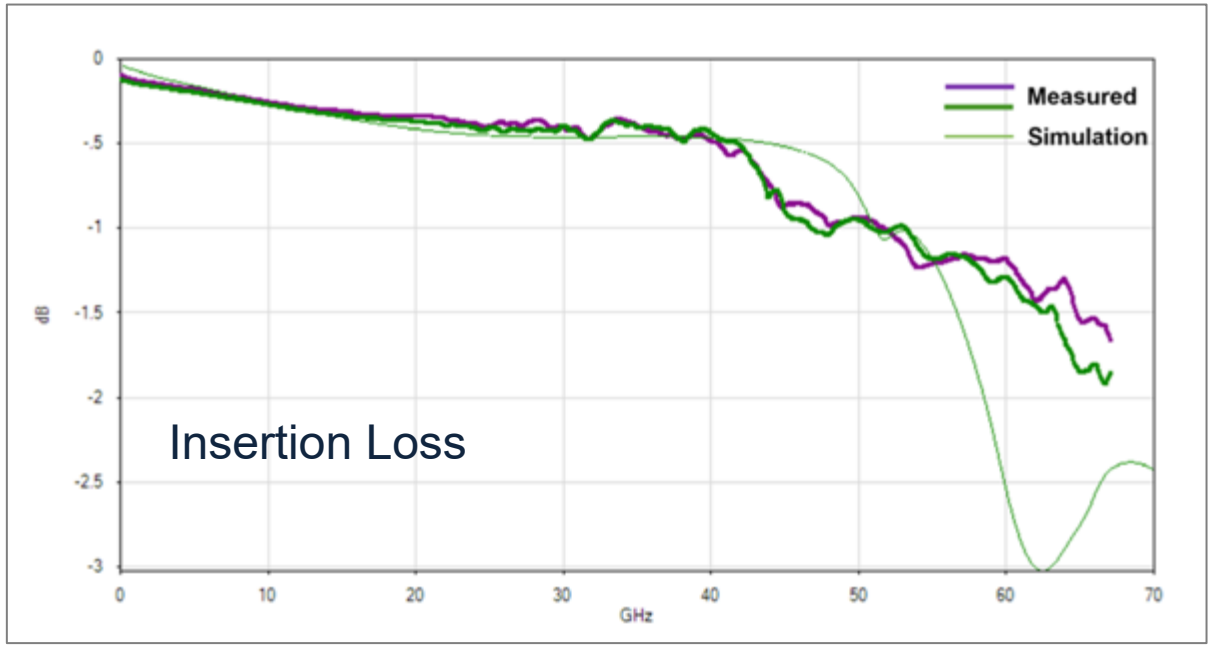
3.4mm x 2.7mm WL-CSP

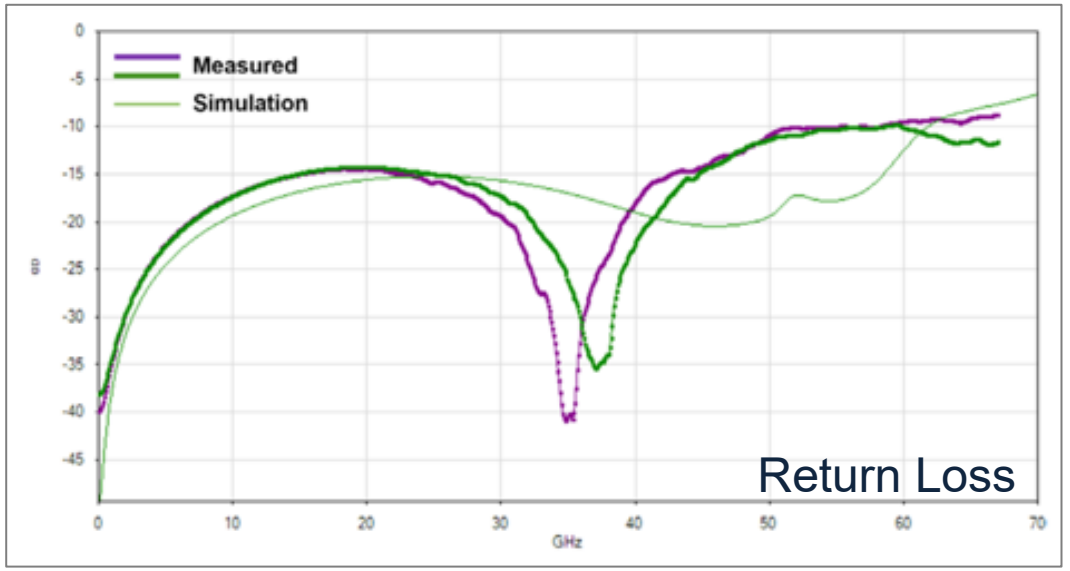
MM5800 EVK

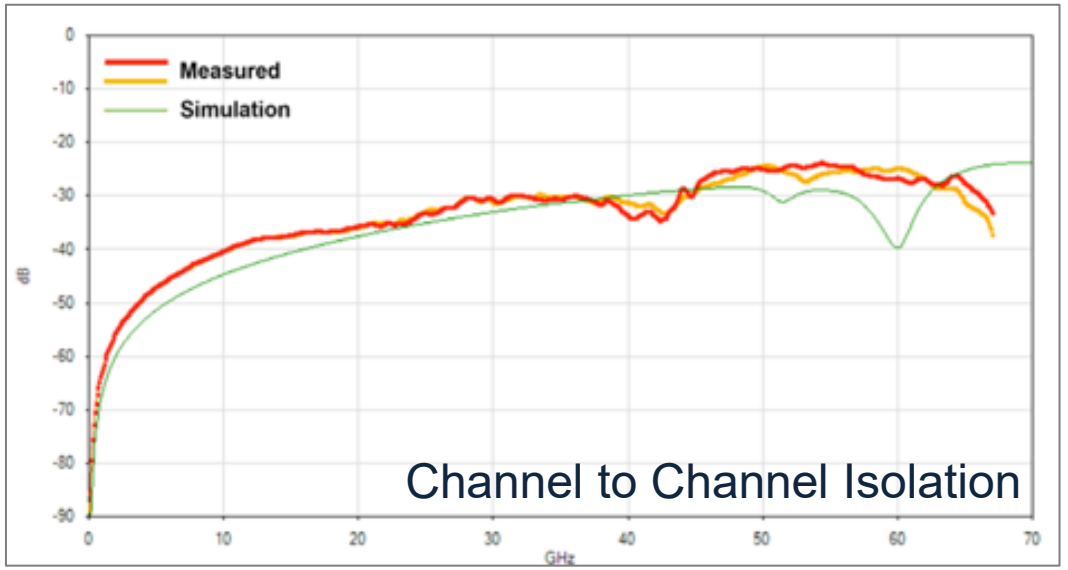


MM5800 – SPDT Target Specifications

- Initial wafer probe test results show SPDT passband performance to 70GHz (< 2dB IL)

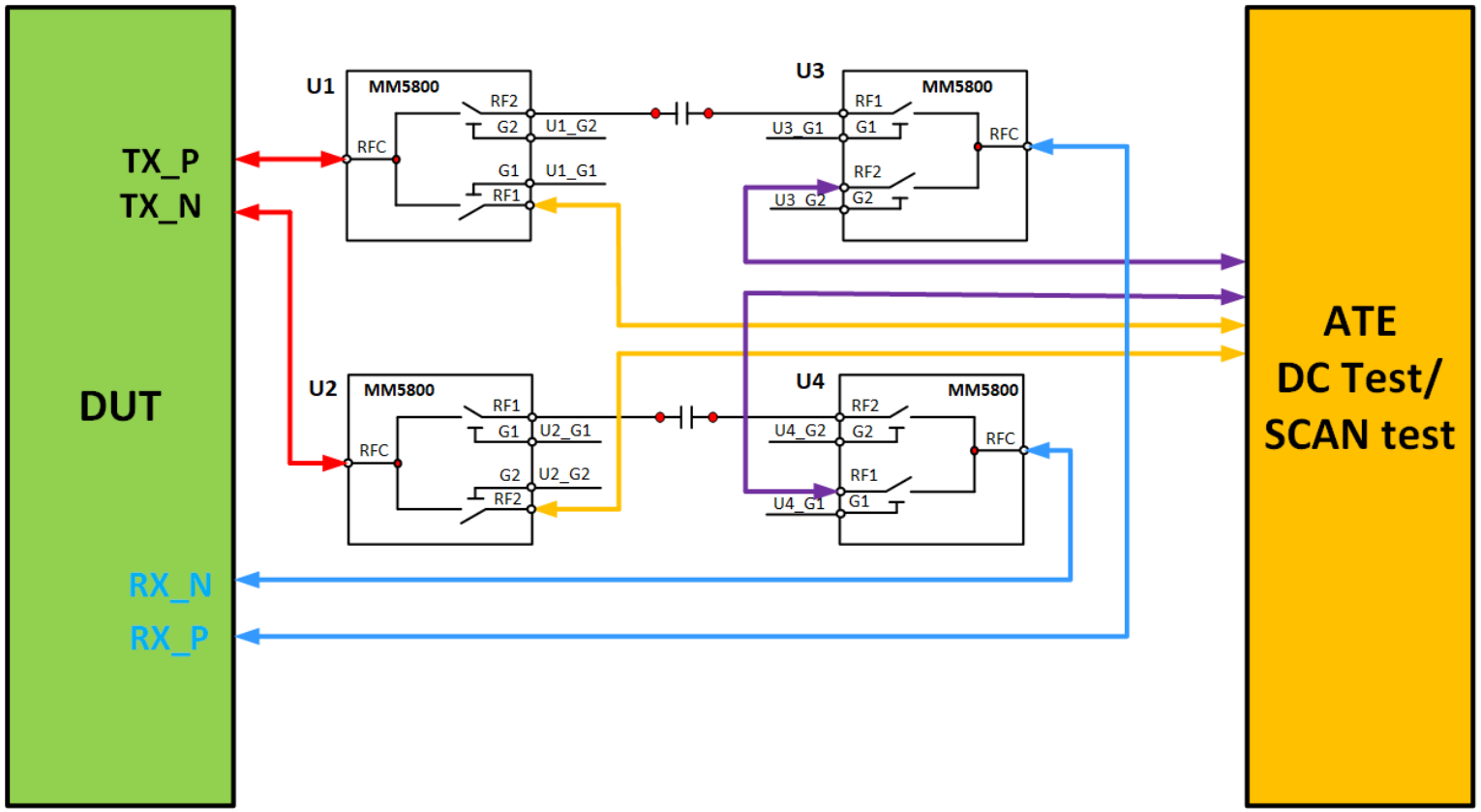




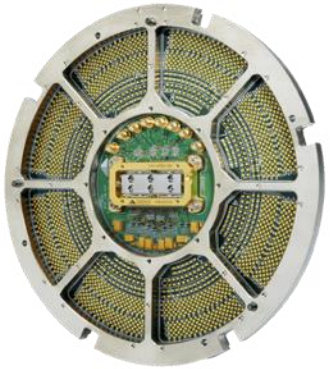


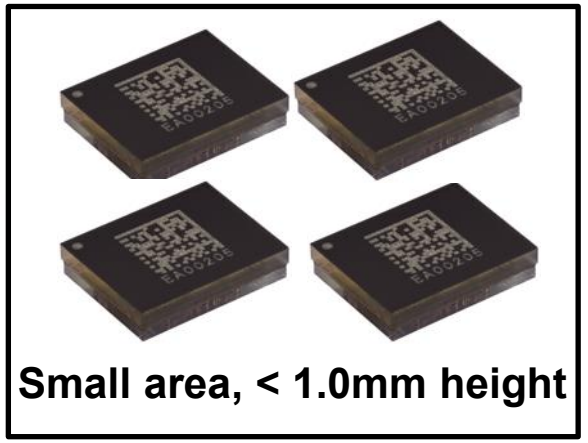
MM5800 – 224 Gbps Loopback Application (AC Coupled)

Initial wafer probe test results show SPDT passband performance to 70GHz (< 2dB IL)



High-speed (224Gbps) loopback at probe

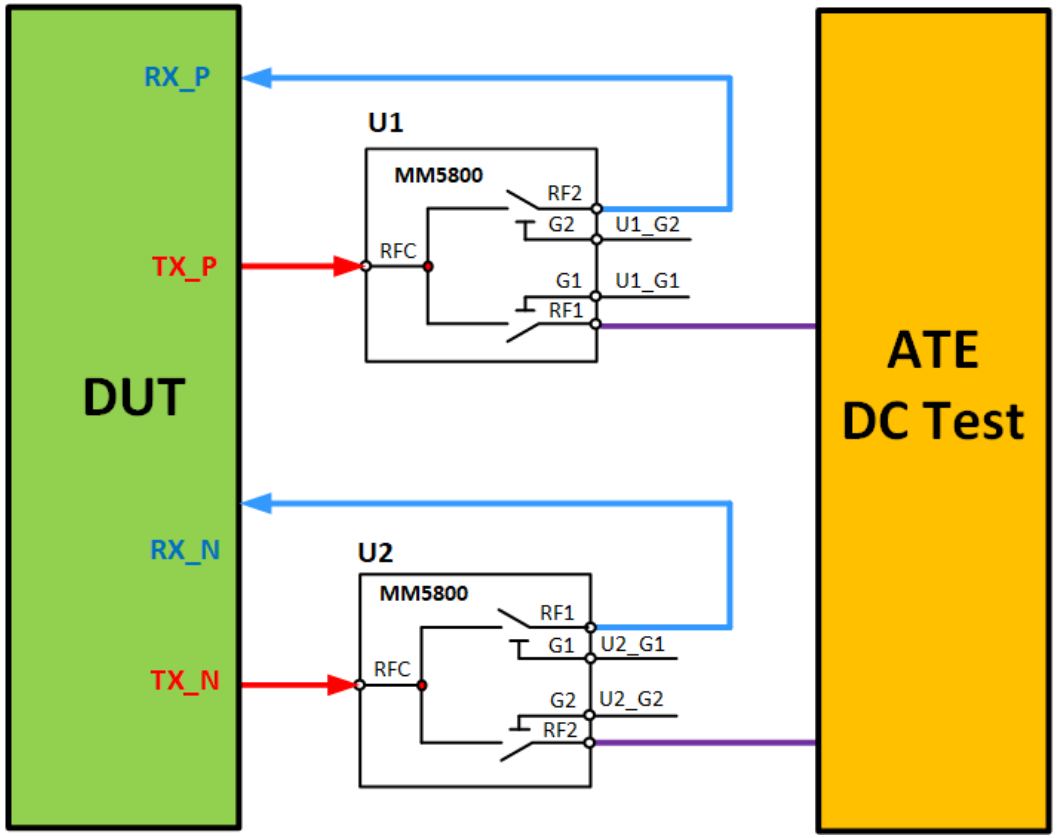




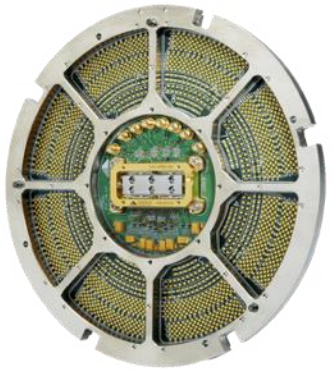
Small area, < 1.0mm height

MM5800 – 224 Gbps Loopback Application (DC Coupled)

Initial wafer probe test results show SPDT passband performance to 70GHz (< 2dB IL)



High-speed (224Gbps) loopback at probe



Small area, < 1.0mm height

Thank you.